ADVANCED DIGITAL DATA ACQUISITION SYSTEM

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ABSTRACT

An ARINC 429 data acquisition system has been developed by Flight Test Engineering for the Boeing Commercial Airplane Group. Traditionally, acquired ARINC 429 data is stored in the acquisition system and periodically sampled for recording. This paper describes a system which acquires data from many different ARINC 429 digital data buses and records that data as soon as it is has been transmitted on the bus.

INTRODUCTION

Boeing developed the Advanced Digital Data Acquisition System (ADDAS) two years ago in support of testing the model 747-400 airplane. The ADDAS is capable of selectively acquiring every label from up to 30 ARINC 429 buses and recording the data on a single track of an analog tape recorder. The system makes the data available for recording as soon as it has received a complete word and also time tags each data word, for time correlating data.

Prior to the development of the ADDAS, digital data was acquired with the use of small bus interface cards controlled by a Remote Multiplexer / Demultiplexer Unit (RMDU). Each card was programmed with an Erasable Programmable Read Only Memory (EPROM) and could store data from up to 64 labels per bus. Using an actual certification program involving 56 ARINC buses for comparison, the RMDU approach required 131 bus interface cards and 40 enclosures consuming 175.5 inches of rack space. Additionally, it took two months of preparation time to format the EPROMs, design the rack layouts and draw the cable diagrams. The same program could have been done with two ADDAS enclosures consuming 17.5 inches of rack space and requiring less then one day of preparation. In addition, on the old system, since the data being recorded on tape was periodically sampled by the RMDU after it had been transmitted on the bus, very limited time correlation could be performed between data on different buses or even different labels on the same bus.

RECORDED DATA FORMAT

Data is output in a Pulse Code Modulated (PCM) stream to a constant bit rate analog recorder. The operator-programmable bit rates are: 64KBS, 128KBS, 256KBS, 512KBS and 1024KBS. Data is output in major frames that are 64 words long and contain a 24 bit frame synchronizing pattern as illustrated in Figure 1. The data is written in a message sensitive format and is not position dependent. Each word in the frame is 48 bits wide and contains a six bit binary bus identification number which determines the contents of the rest of the word. Currently, the system only uses 32 of the possible 64 bus identification numbers with the rest reserved for expansion.

A bus identification number of zero indicates a major time word. Major time words are output 10 times per second and contain hours, minutes, seconds, tenths of seconds, hundredths of seconds and test number. All information in the major time word is in Binary Coded Decimal (BCD) except for the test number which is in a binary format.

A bus identification number between 1 and 30 indicates a valid data word consisting of the full ARINC 429 word[l] and a 10 bit binary minor time tag. The minor time tag has a resolution of 100 microseconds and can be added to the major time word to compute the actual time that the data word was received.

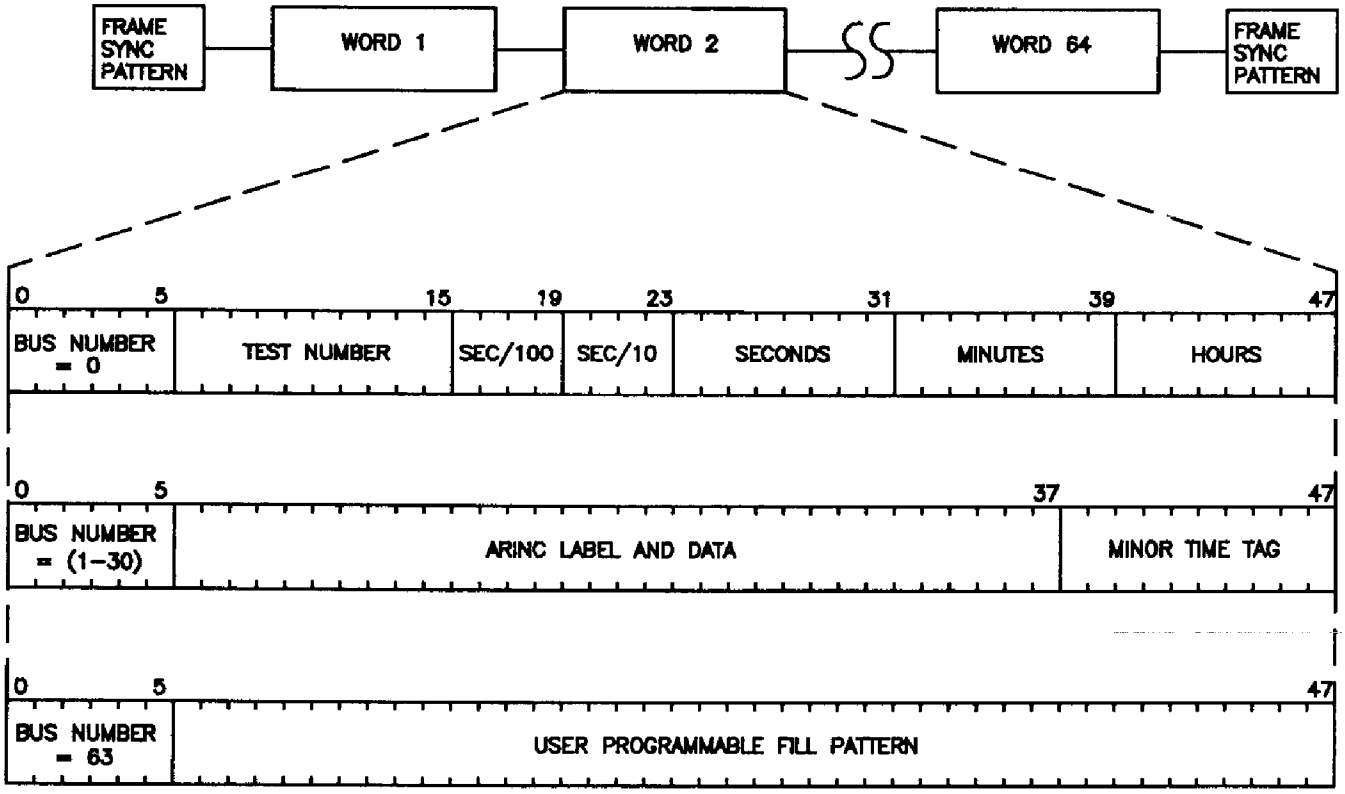

Figure 1 Recorded Data Format

A bus identification number equaling 63 indicates fill data to keep the output data rate constant.

SYSTEM ARCHITECTURE

The entire system is contained in an 8-3/4 inch high rack mount enclosure. The enclosure has 24 card slots, of which 20 are utilized, and is powered from a 48 Volt DC external uninterruptable power supply. Each card is a five inch by seven inch multi-layered printed circuit board which plugs into a Boeing proprietary bus. All cards are accessible from the front of the enclosure via a hinged panel, and all electrical connectors are on the back panel.

The system is designed with a dual bus / dual mode architecture. Figure 2 is a block diagram showing the buses, modes and the cards contained in the system. Every card in the system is connected to both a setup bus and an acquisition bus, however, each card can only operate in the data source mode or the data sink mode. If a card places data onto the acquisition bus it is defined as a data source card while any card that gets data from the acquisition bus is defined as a data sink card. The setup bus is used for system initialization and contains eight data bits, sixteen address bits and some control bits. The acquisition bus is designed to transfer data from multiple data sources to multiple data sinks and contains 48 bits of data and some control bits. The physical location of a card within the enclosure determines whether it is a data source or a data sink.

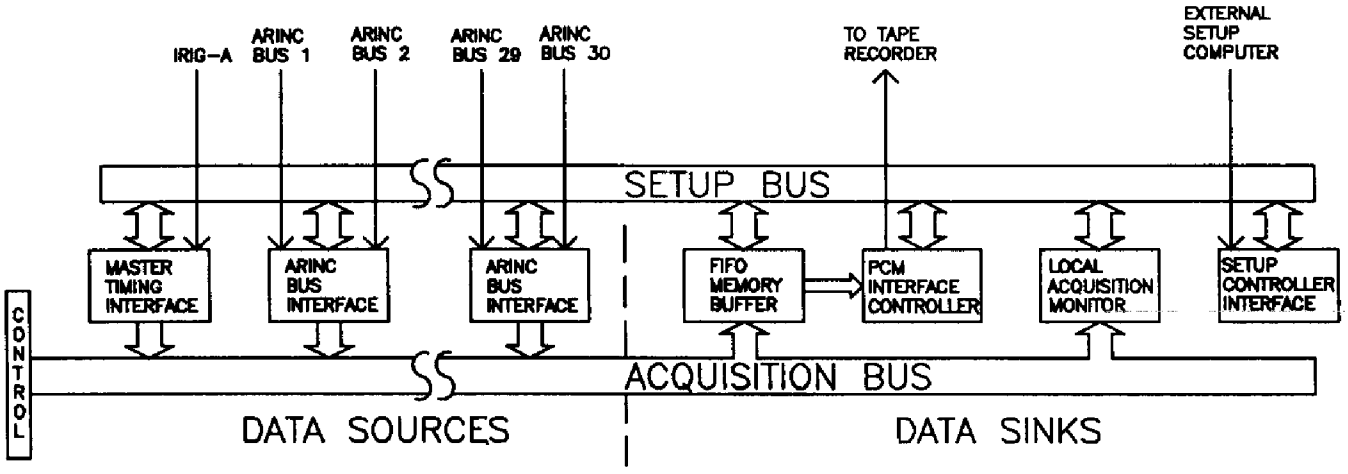

Figure 2 ADDAS Block Diagram

Control of the acquisition bus is handled by a printed circuit board which also contains all card connectors. This controller has a 16 input priority encoder and is responsible for determining which data source card can place data on the acquisition bus. When a data source card has data for recording, it asserts its REQUEST line. The controller

responds with a GATE signal and places the most significant bits of the bus identification number onto the acquisition bus. The requesting card will put its data onto the bus along with the least significant bit of the bus identification number. At the same time, the controller asserts a XFER line to signal all data sink cards that data is available on the bus. Each of the sixteen data source cards has its own unique REQUEST and GATE lines but, there is only one XFER line. In the event that multiple source cards simultaneously assert their REQUEST lines, the controller will grant the bus to the card with the highest priority. The highest priority belongs to the Time Interface Card with priorities decreasing as the bus identification number increases.

An external setup computer is responsible for maintaining a database of programming information. This database contains information on the output bit rate and what buses and labels should be recorded. The setup computer will program the system by transmitting and then verifying this information. Once the system is programmed, it requires no further operator intervention, and it contains non-volatile memory in order to retain its format during power outages.

ARINC BUS INTERFACE CARD

The ARINC Bus Interface Card contains circuitry to interface with two ARINC 429 digital data buses. Each bus interface is identical and completely separate up to the acquisition bus interface logic. The cards are designed to operate with buses that are considerably out of electrical / timing specification[l]. The input impedance of the card is much higher than specification and the card will operate at input voltage levels that are much lower. This design guarantees the ability of the system to gather data under the worst of conditions. The card has special logic to be able to automatically operate with either a high or low Speed bus. The card can be programmed to look at labels with or without Source / Destination Index (SDI) bits for data selection. The data selection logic centers around non-volatile memory, in order to retain formatting information during power outages. The card contains two light emitting diodes that indicate the presence of data activity on the bus, which is invaluable during check out of the system.

MASTER TIMING INTERFACE CARD

The Master Timing Interface Card accepts IRIG-A[2] and outputs a major time word for recording 10 times per second. If the card is not outputting a major time word, it gates the 10 bit minor time tag on the acquisition bus. The minor time tag has a resolution of 100 microseconds, and with a 10 bit value, the minor time will repeat once every 100 milliseconds; therefore the major time word must be output 10 times

per second. Additionally, the card can accept an IRIG-G[2] input signal. If IRIG-G is used, system timing is increased by a factor of ten. When this happens, the minor time tag has a resolution of 10 microseconds, and a major time word will be output 100 times per second. This mode will also activate the hundredths of seconds field in the Major Time Word.

FIFO BUFFER MEMORY CARD

The First In First Out (FIFO) Buffer Memory Card is used to synchronize the incoming data to the fixed rate output stream. The card contains a 4096 deep FIFO memory that is 48 bits wide. The card will place any data transmitted on the acquisition bus into the FIFO Memory and make that data available to the PCM Output Card. Data is transmitted to the PCM Output Card via a ribbon cable located on the front edge of the card. If the FIFO Memory is empty when the PCM Output card wants data, the FIFO Memory Buffer Card asserts an EMPTY signal. If the FIFO Memory is full and the XFER line is asserted, the card will generate an OVERFLOW signal which is used to alert the operator of a problem.

PCM OUTPUT CARD

The PCM Output Card gets data from the FIFO Memory Buffer Card and sends the data to a tape recorder. It also generates the output data stream and inserts the Frame Synchronizing Pattern at the appropriate time. It will output data from the FIFO Memory Buffer Card, and if that card has no data, the PCM card will record a user programmable fill word. The PCM Output Card serializes the data and outputs Non Return to Zero, Bi-Phase and Delay Modulation-Mark codes for recording.

LOCAL ACQUISITION MONITOR CARD

The Local Acquisition Monitor Card provides diagnostic data to the system operator. The card contains logic to selectively capture any data which is being recorded by the system. It can also calculate the data rate for any parameter being processed in the system. In addition, the card can calculate the number of Fill words being recorded. This information is transmitted to an operator via the Setup Controller Interface and is not used in normal operation.

SETUP CONTROLLER INTERFACE CARD

The Setup Controller Interface Card is used for communication with an external setup computer and to initialize and program the system. The Setup Controller is based around an Intel Corporation 8085 microprocessor operating at a clock rate of 4.096

MHZ. This clock is used by the PCM Output Card to generate the output bit clock. With the exception of this clock signal, the entire Setup Controller Interface Card could be removed, and the system would still acquire and record data. The card contains 8 KB of program EPROM, 16 KB of EEPROM for setup database storage, 1KB of volatile memory, reset logic, a watchdog timer, two serial interfaces and an interrupt controller.

Upon command from the external setup computer, the Setup Controller Interface Card will use the data in its setup database to program the system. This process is rather analogous to compiling source code into executable modules. The system was designed this way to isolate the external setup computer from the internal workings of the ADDAS.

DATA INTEGRITY FEATURES

The prime objective of the ADDAS is to reliably acquire and record data. With this in mind, several features were designed into the system to preclude accidental data loss. The enclosure and the ARINC Bus Interface cards are designed so that no single point failure can cause a bus fault. Each enclosure has a unit identification switch mounted on the front panel. Every message transmitted from the external Setup Computer to the system contains this identification number, or the system will ignore that message. The front panel also has a guarded SETUP ENABLE switch. Any accidental or intentional modification of the non-volatile system memory when the SETUP ENABLE switch is not enabled is prohibited by logic contained in the Setup Computer Interface Card. Since the SETUP ENABLE switch should be enabled only when the system format is being modified, the PCM Output Card stops outputting data but continues to output a Frame Synchronization Pattern and FILL Words when the SETUP ENABLE switch is enabled.

FUTURE ENHANCEMENTS

A new card to allow the recording of ARINC 629 data is currently under development. This card will be used for some initial test processing of ARINC 629 data and is not intended for long term use. The card decodes ARINC 629 data and processes it just as it would process ARINC 429 data. It is programmed exactly as an ARINC 429 bus interface card would be. When a word string is received, logic in the card decides whether or not to record the data. If the word string is to be recorded, each sixteen bit word in the string is processed as an ARINC 429 data word. This format contains an inordinately high amount of overhead since every sixteen bit word in the string is recorded with its sixteen bit label, as well as a 10 bit time tag and six unused bits. The time tag is completely redundant, since once the time of an ARINC 629 label is

known, the time for every word in the string is also known. The unused bits are left over since an ARINC 429 word may contain up to 22 bits of data.

CONCLUSIONS

The ADDAS has been used for over two years and has considerably improved the ability of Flight Test to record and analyze ARINC 429 data. The computerized setup allows formats to be modified in minutes as compared to hours with the older system. Additionally, since all data is time tagged, accurate time correlation between buses is greatly enhanced. This is of considerable importance due to the increasing complexity of avionics on today's modern aircraft.

ACKNOWLEDGEMENTS

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REFERENCES

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[2.] Telemetry Group Range Commanders Council, IRIG Standard 104, Range Commanders Council, U. S. Army White Sands Missile Range, New Mexico.

NOMENCLATURE

ADDAS	Advanced Digital Data Acquisition System
ARINC	Aeronautical Radio, INC.
BCD	Binary Coded Decimal
EPROM	Erasable Programmable Read Only Memory
EEPROM	Electrically Erasable Programmable Read Only Memory
FIFO	First In First Out
KBS	KiloBytes per Second
IRIG	Inter-Range Instrumentation Group
PCM	Pulse Code Modulation
SDI	Source / Destination Index
RMDU	Remote Multiplexer / Demultiplexer Unit