WIDEBAND MODEM CHARACTERIZATION TESTING

Gerald T. Finn
Satellite Control Division
The Aerospace Corporation
Sunnyvale, California 94086

ABSTRACT

As part of an investigation into the causes for random, unexplained data “dropouts” on a Defense Satellite Communication link between the Air Force Satellite Control Facility, Sunnyvale, California and the Indian Ocean Remote Tracking Station, a number of tests were conducted to characterize the performance parameters of the wideband modems used on the link.

These tests were used to measure the loop parameters of the modem Carrier and Timing Recovery Loops and to determine the modem sensitivity to RF phase disturbances, data rate variations and various repetitive bit patterns.

This paper describes the test techniques used and the results obtained.

INTRODUCTION

In early 1979, a wideband satellite communications link was established between the Air Force Satellite Control Facility (AFSCF), Sunnyvale, California and a remote tracking station in the Indian Ocean, referred to as IOS. This link, utilizing the Defense Communications Agency (DCA) communications network and the AFSCF interface equipment, is called DSIS, DCA-SCF Interface System. Figure 1 is a simplified diagram of the system.

Since the start of operations, this link has been experiencing large numbers of random data dropouts. An intensive Air Force, Aerospace and Ford Aerospace Communications Corporation test effort was established in late 1980 to review the previous efforts to correct the link problems and to further isolate and correct the causes for the communications dropouts.

The primary emphasis of this test effort was to characterize the performance limitations of the individual components in the system. Of particular interest were the wideband modems used on the link.

The symptoms of the data dropouts pointed to a possible loss of Bit Count Integrity (BCI) in the modems which in turn caused a loss of synchronization in the DSIS Demultiplexer.

These modems use staggered (or offset) Quadriphase Shift Keying, SQPSK (or OQPSK), to modulate a 70 MHz IF carrier with the digital baseband information. Rate ½, constraint length 7, Convolutional Encoding and Viterbi Decoding are used with the modems to provide a Forward Error Correction capability. The digital data rates used on the system are 192, 384, 768, 1536, and 3072 kbps.

Two types of modem are used on the AFSCF-IOS communications links: Stanford Telecommunications Inc., STI 6144 modems at the SCF and IOS terminals and Harris MD-1002 modems at the Fort Detrick, MD nodal point.

MODEM TEST PROGRAM

Since the data dropouts on the link appeared to be related to a loss of Bit Count Integrity (BCI) in the modems the test program centered around the performance characteristics of the Carrier Recovery Loop (CRL) and Timing Recovery Loop (TRL) in the demodulators (See Figure 2). The test sequence followed was:

a. Standard Bit Error Rate (BER) vs E_b / N_o tests to verify proper modem alignment.

b. Carrier Recovery Loop Bandwidth measurements.

c. Timing Recovery Loop Bandwidth measurements.

d. Bit Pattern Sensitivity Tests.

e. Bit Rate Sensitivity Tests.

f. RF Phase Error Sensitivity Tests.

BIT ERROR RATE TESTS

The Bit Error Rate Test setup used was the standard configuration depicted in Figure 3. A Psuedo-random bit pattern (2047 bits long) is used to modulate the 70 MHz IF, a measured level of white, Gaussian noise is added to the IF signal and the result is fed to

the demodulator input. The bit error rate test set detects the number of bit errors in the received 2047 bit sequence.

This test enables the measurement of two important modem parameters; the E_b /N_o threshold at which the demodulator loses (or acquires) carrier phase lock and the conformance of the BER vs E_b /N_o curve with the theoretical performance curve over the operational range for E_b /N_o. A typical result from this test is shown in Figure 4.

This particular test has proven to be extremely useful in determining the overall condition of the modems used in the system. The problems uncovered by this test included demodulator misalignment (resulting in 3 db degradation of BER performance), excessive noise in the CRL Voltage Controlled Oscillator, VCO, (resulting in 3 - 4 db degradation in lock threshold) and misaligned TRL VCOs (resulting in 3 - 4 db degradation in lock threshold).

As a result of these initial test findings, new procedures have been prepared requiring that all of the SCF modems be subjected to Bit Error Rate tests every three (3) months as a minimum.

CARRIER RECOVERY LOOP PARAMETER TESTS

The STI 6144 modem uses a x4 multiplier loop (See Figure 2) to recover a carrier reference for the demodulator. The x4 circuitry essentially provides a 280 MHz single phase reference signal from the 70 MHz Quadriphase IF signal. The phase lock loop is locked to the 280 MHz reference and provides a 70 MHz reference to the demodulators. Since the performance of the Carrier Recovery Loop determines the demodulators ability to track a signal in noise and to maintain an accurate demodulation reference during signal disturbances, the characteristics of the loop are of prime concern. Figures 5 and 6 show two methods used to measure the performance of the Carrier Recovery Loop.

The first method, Figure 5, substitutes an FM signal generator, with a center frequency of 70 MHz, for the modulator's 70 MHz crystal oscillator. The deviation of the demodulators VCO as a result of the FM on the Modulator's carrier is detected by the FM discriminator and measured using a MINCOM Flutter Meter. The deviation of he VCO is compared to the deviation of the carrier at various FM modulation frequencies to determine the Phase Lock Loop's frequency response.

Because of the poor noise characteristics of the FM discriminator used in the initial tests, the second test method, Figure 6, was developed. The primary difference between the two techniques is that with the second method the deviation of the VCO control voltage is measured rather than the actual VCO deviation. For small deviations, the relationship

between the VCO control voltage and the VCO output is linear. Using a low frequency (<20 Hz) modulation of the FM generator, a 0 db reference level of the VCO control voltage is established. Then by maintaining the FM generator's deviation constant, the modulation frequency is increased incrementally and the response of the VCO control voltage is measured.

The two test techniques provided equivalent results, with the second method proving to be easier to implement.

A third technique which has recently been used successfully, is similar to the arrangement in Figure 6 but an HP8660 Frequency Synthesizer with an 86634A Phase Modulation plug-in is used to replace the Modems' 70 MHz crystal oscillator.

The results of the tests agreed with the design criteria used for the Harris and STI modems. Figure 7 shows the data collected.

The 3 db bandwidth of the STI modem's CRL was determined to be about 300 Hz for data rates below 768 kbps and 2000 Hz for data rates of 768 kbps and above. The Harris modem CRL was found to have a 3 db bandwidth of about 140 Hz at 192 kbps. This difference in CRL bandwidth was found to be significant during one instance on the operational link.

A power supply problem in the transmit section of the SCT-21 at IOS (refer to Figure 1) induced phase modulation at harmonics of 60 Hz on the transmitted signal. The Harris demodulator at Fort Detrick, Maryland failed to track this phase modulation and as a result, the data was unusable. Bypassing the Harris modems at Fort Detrick with a 70 MHz Amplifier provided a temporary fix to the link since the STI Demodulator at the STC, operating with a CRL loop bandwidth of 2000 Hz, was capable of tracking the phase "noise" and maintain acceptable data quality.

The design of the Carrier Recovery Loop involves tradeoffs in which the characteristics of the link on which it is used must be considered. A narrow CRL bandwidth will permit the loop to maintain synchronization with a carrier under high Gaussian noise conditions. The long time constant associated with a narrow loop bandwidth will also permit the CRL to maintain synchronization during short fades or carrier dropouts. Therefore, where C/KT is marginal a narrow CRL Loop Bandwidth is desirable.

However, a narrow bandwidth limits the loops ability to track phase noise or phase perturbations in the RF system. Sources for these perturbations include the local oscillators in the up- and down-converters and the AM/PM conversion effects of high power amplifiers operating near saturation.

TIMING RECOVERY LOOP (TRL) MEASUREMENTS

The Timing Recovery Loop in the demodulator derives a clock synchronized to the detected data stream (See Figure 2). This clock is used to determine timing for the Integrate and Dump circuitry and to the other baseband circuits in the demodulator, ultimately providing the demodulators output clock.

The test method used to determine the Timing Recovery Loop performance parameters is similar to that described for the Carrier Recovery Loop, except that the transmit baseband data (and clock) stream is FM modulated and the response of the TRL output clock is measured. Figure 8 shows the typical test configuration. Figure 9 shows the results of these tests.

Our primary concern, at the time these tests were conducted, was the ability of the modems TRL to maintain synchronization during transitionless data sequences. The narrow loop bandwidths measured by the test indicate the TRL time constant is relatively long (estimated to be about 14 milliseconds). As a result, the duration of signal dropout (i.e., transitionless data pattern) that the TRL will “ride” through was estimated to be about 3000 bits (at 192 kbps). Later tests with specific data patterns confirmed this conclusion.

BIT PATTERN SENSITIVITY TESTING

Early in the investigation of the anomalies on the DSIS link between the STC and IOS, a concern that sequences of transitionless data, prevalent in the data stream, would cause the Timing Recovery Loop to lose lock and drift, with a consequent loss in bit count integrity. Other data sequences, which could cause a reduction in the recovered carrier reference signal, were also of concern since these sequences could potentially cause the Carrier Recovery Loop to cycle slip, leading to a loss of bit count integrity.

As a result of these concerns, a series of tests were conducted to determine the sensitivity of the modems to various bit patterns. The general test configuration used is shown in Figure 10.

The first tests were designed to stress the Timing Recovery Loop. Since the demodulator recovers a timing reference from only one channel (either the I or Q depending on the phase of the Carrier Recovery Loop lock), bit patterns which result in transitionless sequences on either or both the I and Q channels, after differential and convolutional encoding, were tested.

The test configuration permitted the synchronous insertion of various repetitive test bit patterns into a PN data stream. The duration of the test pattern could be varied. The demodulators output clock was compared to the modulators input clock and the amount of jitter was measured. The duration of the test pattern was increased to the point where the Timing Recovery Loop would cycle slip, resulting in a loss of Bit Count Integrity.

It was found that relatively long transitionless data patterns were required before the Timing Recovery Loop started to cycle slip. The chart in Figure 11 shows that the residual jitter did not start to increase until the data sequences exceeded about 800 bits (4 ms duration). Cycle slipping did not occur until the test patterns exceeded about 3600 bits (20 ms).

The maximum transitionless sequence that can occur on the operational link in question is about 230 bits, due to the multiplexers framing method. As a result of these tests, it was concluded that, while specific data patterns could permit the Timing Recovery Loop to cycle slip, sufficient margin existed on the operational system to indicate that this was not a probable cause for the problems experienced.

It should be noted that the introduction of thermal noise in the link will degrade the modem performance with the transitionless data patterns. However, even with the E_b / N_o set below the normal range of 8 - 12 db, transitionless sequences on the order of 400 - 500 bits were required to cause cycle slipping.

The second series of pattern sensitivity tests involved data sequences which would reduce the level of the recovered carrier reference in the demodulators Carrier Recovery Loop. These sequences would increase the probability of the CRL cycle slipping and consequently could result in a loss of Bit Count Integrity.

Data sequences resulting in “1010...” patterns on both the I and Q lines of the modulator produce a spectrum containing most of the signal energy in the 3rd and 5th harmonics of the data rate. These harmonics are severly attenuated by filtering used to conserve satellite bandwidth. As a result, the reference signal produced by the x4 multiplier in the Carrier Recovery Loop is 3 - 4 db lower than that produced by an essentially random data stream. The net effect is that the modems’ lock threshold is degraded by some 3 - 4 db. With a marginal link C/KT, cycle slipping of the CRL may result.

With a continuous data pattern resulting in “1010...” sequence on both the I and Q channels the particular modem under test lost lock at an E_b / N_o of about 6.4 db. (This same modem maintained lock at an E_b / N_o of 2.4 db when the data stream consisted of a PN sequence.) Other tests involving short sequences of this data pattern (approximately 300 bits) imbedded in a PN sequence did not result in the modem losing synchronization until

the E_b / N_o was reduced to below 4.0 db. This indicates that the CRL time constant was sufficiently long to permit short sequences of these particular data patterns to occur without impacting the operational link performance, provided adequate C/KT is maintained.

BIT RATE SENSITIVITY (TRACKING RANGE) TESTS

The purpose of these tests was to determine the capability of the modems to lock on and track data rates that vary from the nominal data rate setting of the modem. The general test configuration is indicated in Figure 12.

The test consists of varying the input data rate about the nominal setting of the modem and measuring the phase differential between the input clock and output clocks.

As seen in Figure 13, the STI 6144 Modem acquires and tracks data rates approximately ±1.5% about the nominal data rate.

The Harris MD-1002 Modem, however, exhibits a nonlinearity when the data rate varies more than about ± 0.1%, and loses lock at ± 0.3% of the nominal data rate. This narrow tracking range is probably due to the use of VCXOs in the Harris Timing Recovery Loop (the STI Modem uses an RC tuned VCO). While this narrow range may be of concern when used with some data sources, the crystal controlled multiplexer data output was found to be well within the ± 0.1% range of the Harris Modem.

RF PHASE ERROR SENSITIVITY TESTING

Concern that phase noise or phase perturbations on the RF link may be causing the modem Carrier Recovery Loop to cycle slip, led to the initiation of a series of tests to determine the sensitivity of the demodulators CRL to phase disturbances.

The test configuration shown in Figure 14 was used to introduce phase disturbances in the modulators 70 MHz carrier. The demodulators response to the disturbance was observed.

Various wave shapes were used to modulate the HP 8660's phase modulation section. As expected, the rate of change of the phase disturbance was found to be critical in the ability of the CRL to track the disturbance. Step changes in the carriers phase of 40° to 70° caused the Carrier Recovery Loop in the demodulator to cycle slip 90°. Since a 90° shift in the reconstructed carrier causes the I and Q data to exchange lines in the demodulator (Figure 2), the Timing Recovery Loops reference shifted 90° and the demodulator lost Bit Count Integrity. The Viterbi Decoder and the external BER Test Set Receiver lost data

synchronization. These symptoms are identical to those observed on the operational link during the data dropouts.

It was interesting to note, that phase disturbances of more than approximately 70° caused the Carrier Recovery Loop to cycle slip 180°. Since the I and Q data streams do not exchange under this condition (although one or the other data stream may be inverted), the Timing Recovery Circuit reference does not change and Bit Count Integrity is maintained. While some bit errors (10 - 40 errors) were observed, the Viterbi Decoder and the external BERTS receiver maintained synchronization.

The testing to date has been qualitative in nature and was conducted primarily to duplicate the symptoms observed on the operational links.

Additional tests to quantify the sensitivity of the CRL to various types (repetition rate, rate of change, amplitude) of phase disturbances are planned.

SUMMARY & CONCLUSIONS

The modem characterization testing described here represent only a part of an extensive investigation into the causes for loss of data synchronization on an operational link. As such, the test results provided a sound baseline for further system level (end-to-end) tests.

In addition to uncovering a number of maintenance deficiencies, the characterization tests defined the capabilities/limitations of the modems under a wide range of conditions. In particular the measurements of CRL and TRL bandwidths together with the pattern sensitivity testing indicated that pattern sensitivity was not a primary cause for the data dropouts. The tracking range tests indicated that while the Harris MD-1002 modem had a much narrower tracking capability than the STI 6144 modem, neither modem should have a problem with the crystal controlled multiplexer data source.

The RF phase perturbation tests conducted on the STI 6144 modem duplicated the symptoms observed on the operational system. While additional work is required in this area, the tests show that the modem is relatively insensitive to step changes in phase less than about 40°. This corresponds to the results obtained by Harris Corporation on the MD-1002 modem (Reference 1).

Sources for phase perturbations of this magnitude are currently under investigation. At this time, the most probable cause appears to be the Up- and Down-converters (and associated frequency synthesizers) used in the Ground Terminals. (See Figure 15.) The synthesizers used at some of the terminals have a history of excessive phase noise. These phase

perturbations when multiplied by the converters could be of sufficient magnitude to cause the modems Carrier Recovery Loop to cycle slip.

The tests conducted to date indicate that the primary cause of the data dropouts on the operational link is phase perturbations originating in the RF equipment. These phase perturbations are of sufficient magnitude to cause the Demodulator's Carrier Recovery Loop to cycle slip 90° and consequently to exchange the I and Q data streams in the demodulator. Since the I and Q data streams are staggered 90°, the reference signal for the Timing Recovery Loop in the modem will shift 90° under this condition, causing the loop to lose lock and Bit Count Integrity.

Analyses suggest that a QPSK system would be less sensitive to the catastrophic effects of the RF phase perturbations. While the CRL in the QPSK modem would still be susceptible to cycle slipping the exchange of the I and Q data lines in the demodulator would not disturb the Timing Recovery Loop since the I and Q data streams are in-phase. While bit errors will be induced under this condition, Bit Count Integrity would be maintained.

ACKNOWLEDGEMENT

The author would like to thank Dr. M. H. Nichols for his support and guidance in the course of these efforts.

REFERENCES

(1) "Final Technical Report Vol. 1 Earth Terminal Engineering Studies", Submitted by Harris Corporation Government Systems Group Communications System Under Contract S-200, Melbourne, Florida, May 80

(2) "IOS LINK ANALYSIS 1981 REPORT", TR6230, Submitted by Ford Aerospace & Communications Corporation under Contract F04690-82-C-0005, Sunnyvale, California, Jan 82

(3) "STI 6144 MODEM TEST SYSTEMS ENGINEERING SUPPORT", STI-TR-9067, Submitted by Stanford Telecommunications Inc. under Contract SC-720562-EY, Sunnyvale, California, Aug 81

(4) "LINK BIT-COUNT INTEGRITY", TOR-0081(6420-14)-l, Submitted by The Aerospace Corporation under Contract F04701-80-C-0081, Mar 81

(5) "DIAGNOSTIC AND AUXILIARY INSTRUMENTS FOR SATELLITE LINKS", TOR-0081(6420-14)-4, Submitted by The Aerospace Corporation under Contract F04701-80-C-0081, Mar 81

(6) Gardner, Floyd M., PHASELOCK TECHNIQUES, 2nd Edition, Wiley-Inscience, New York, New York, 1979

(7) Finn, G. T., "Preliminary Test Report, DSIS Modem Characterization Tests", Letter Report, The Aerospace Corporation, Feb 81

(8) Spilker, James J., DIGITAL COMMUNICATIONS BY SATELLITE, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1977

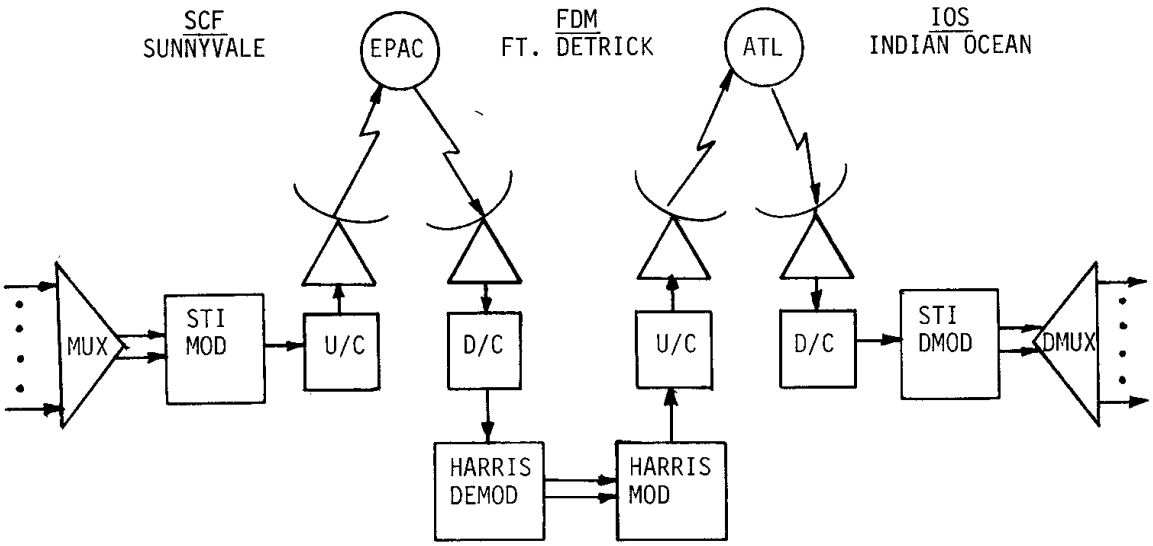

Figure 1. AFSCF-IOS Communication Link

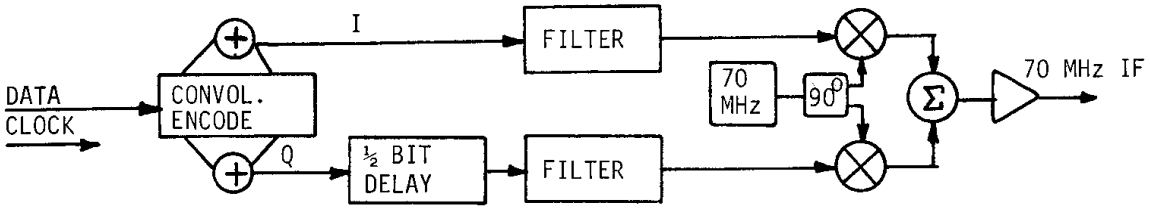

Figure 2a. SQPSK Modulator

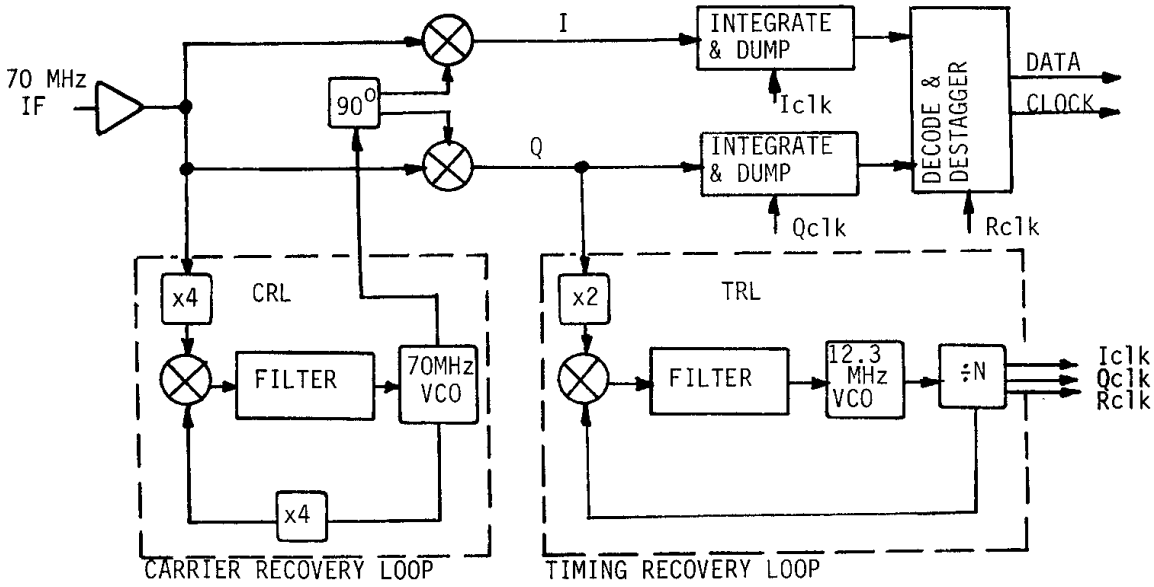

Figure 2b. SQPSK Demodulator

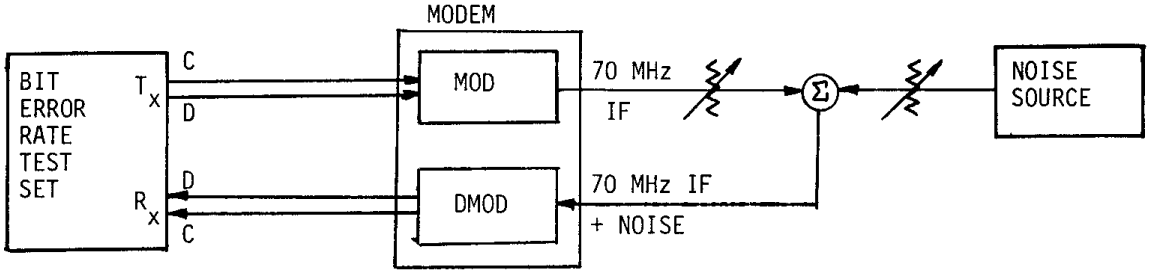

Figure 3. Bit Error Rate Test

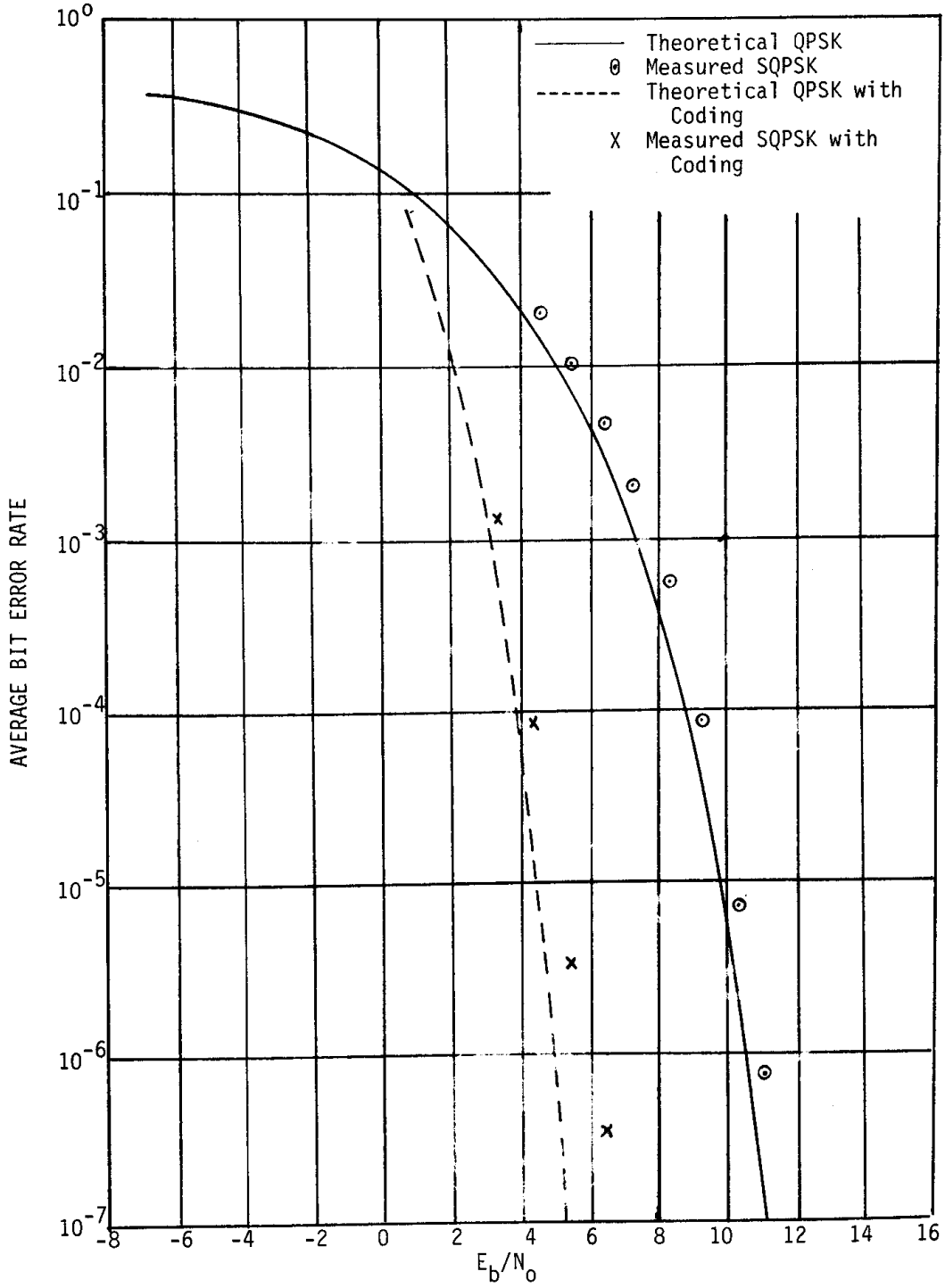

Figure 4. Bit Error Rate vs E_b/N_o

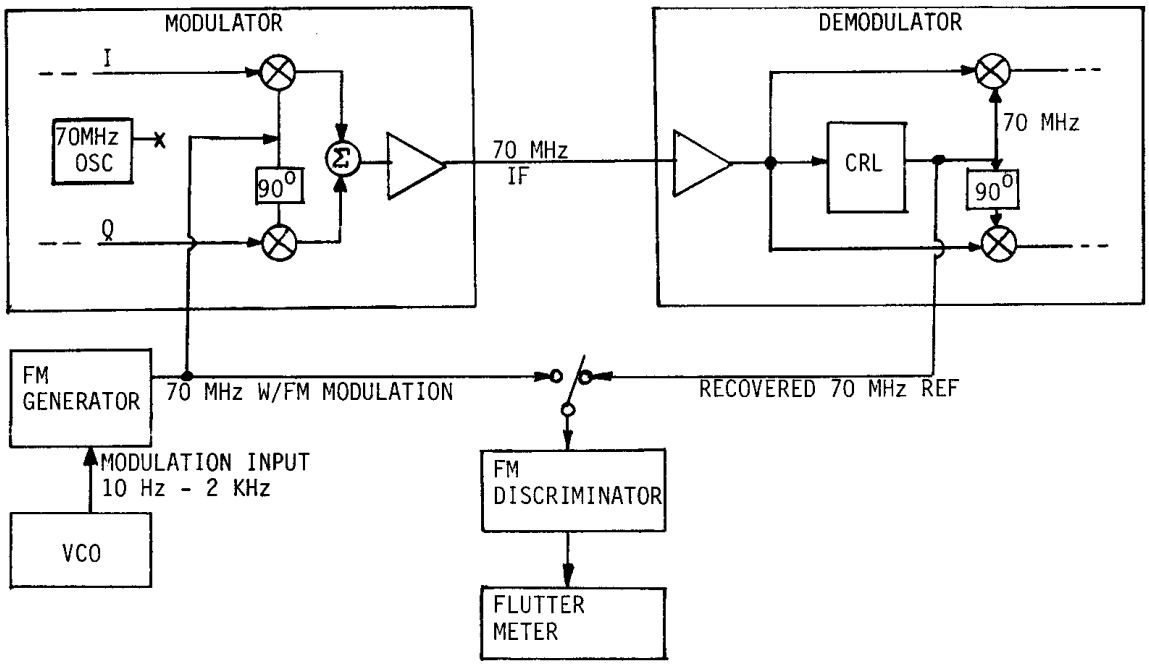

Figure 5. Carrier Recovery Loop Bandwidth Measurement (Method 1)

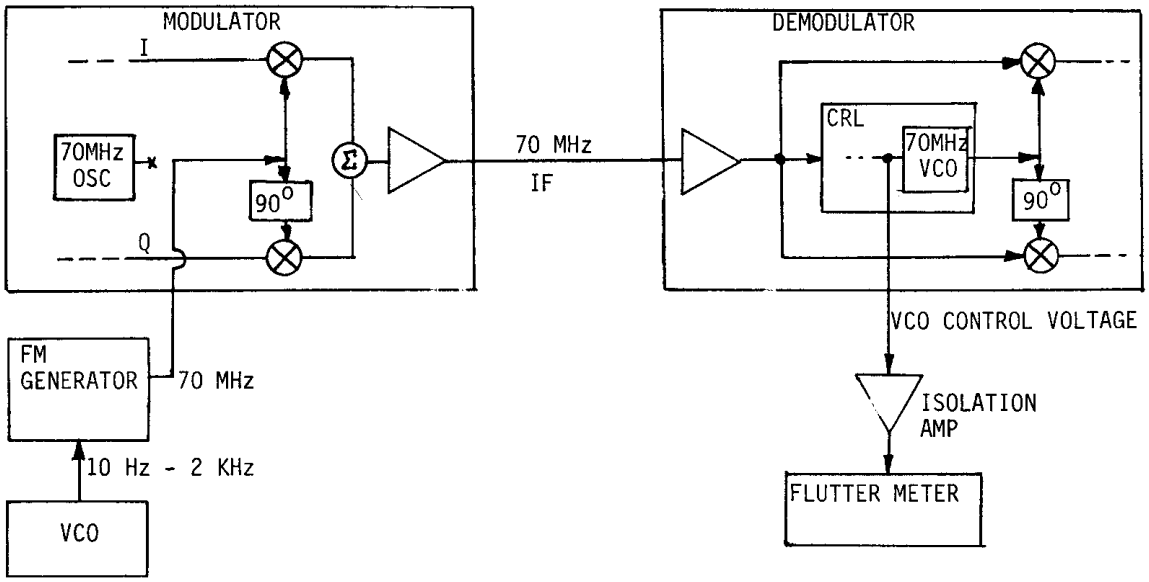

Figure 6. Carrier Recovery Loop Bandwidth Measurement (Method 2)

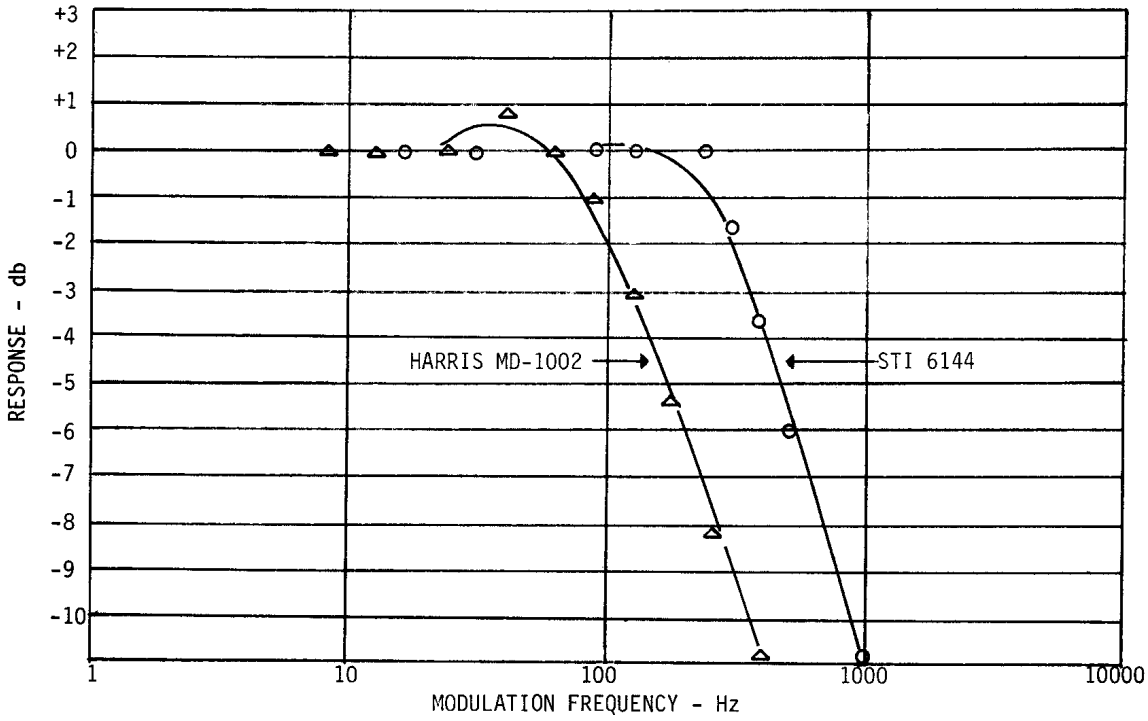

Figure 7. Carrier Recovery Loop Bandwidth Measurements

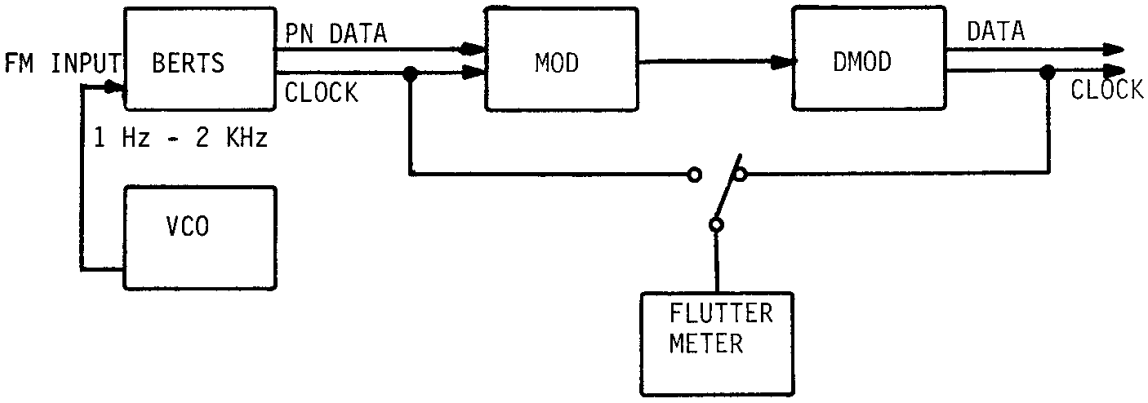

Figure 8. Timing Recovery Loop BW Test

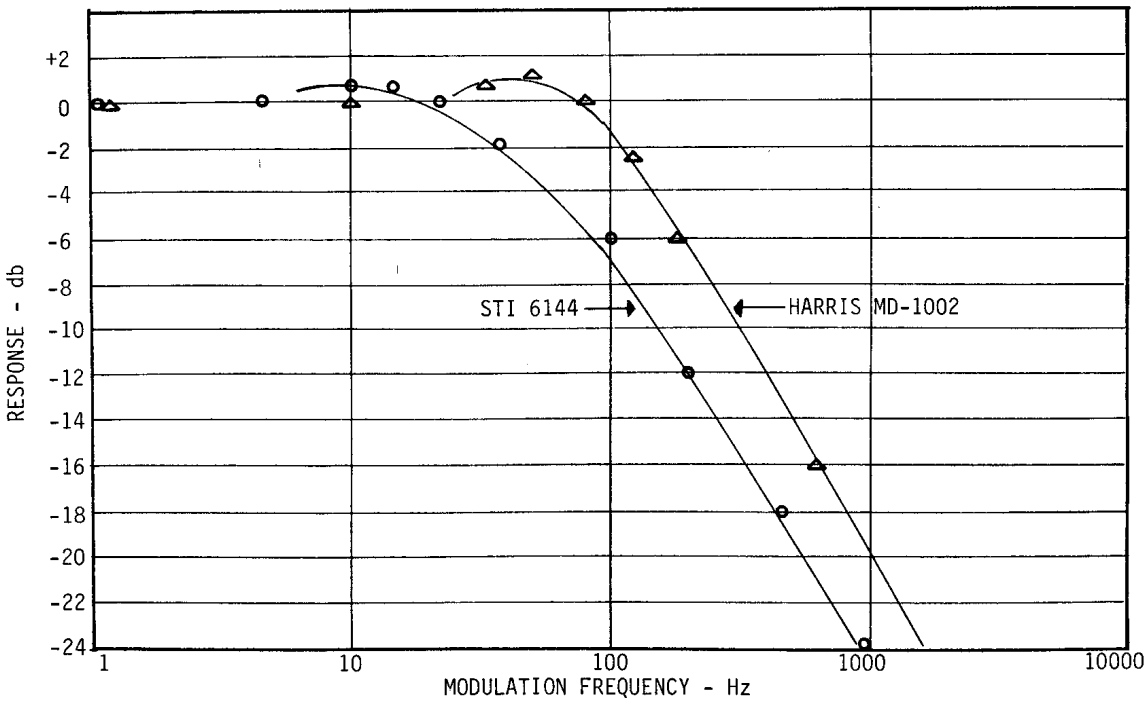

Figure 9. TRL Bandwidth Measurements (192 kbps, Uncoded)

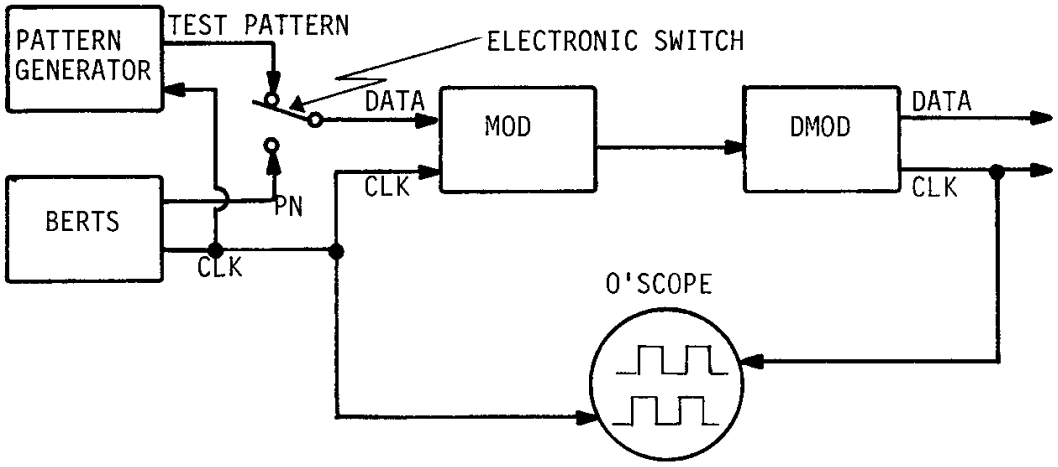

FIGURE 10. PATTERN SENSITIVITY TESTING

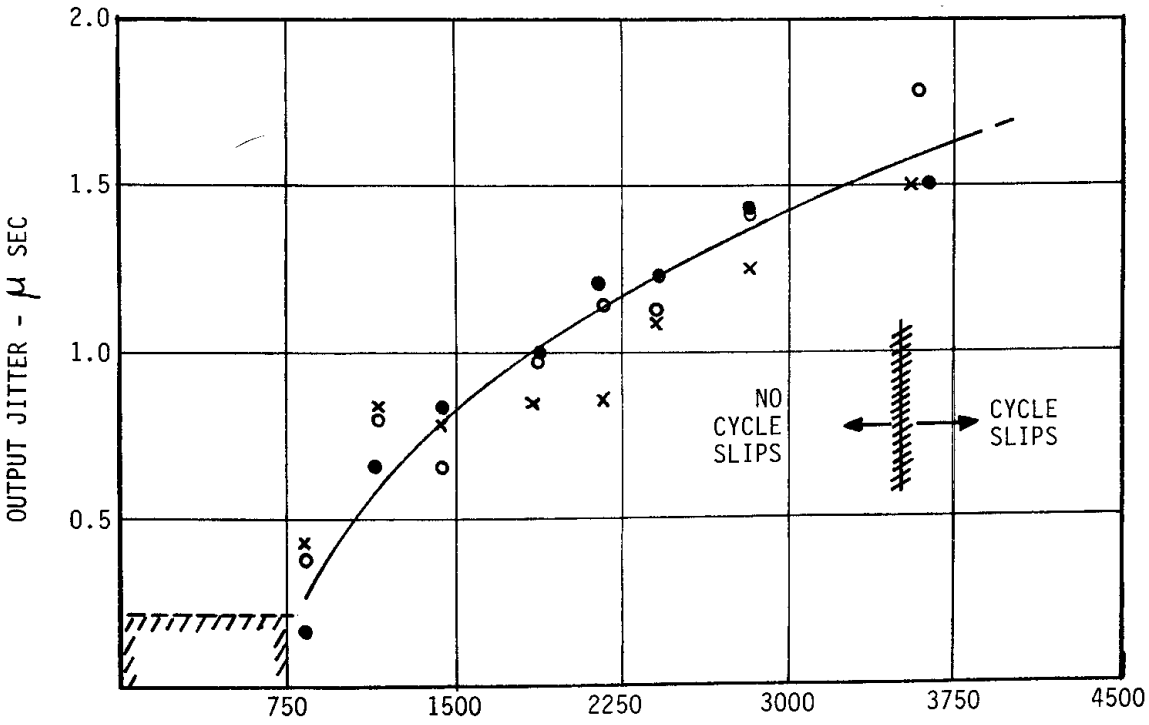

Figure 11. Length of Transitionless Sequence-Bits

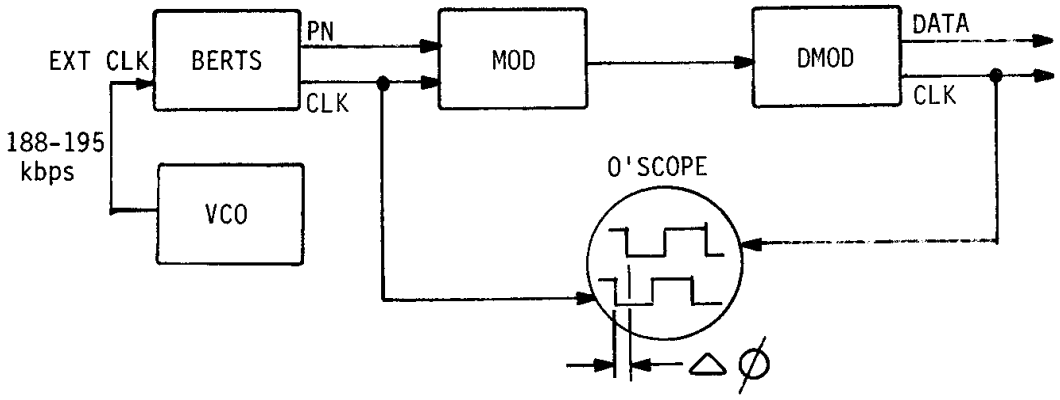

Figure 12. Data Rate Sensitivity Tests (Tracking Range)

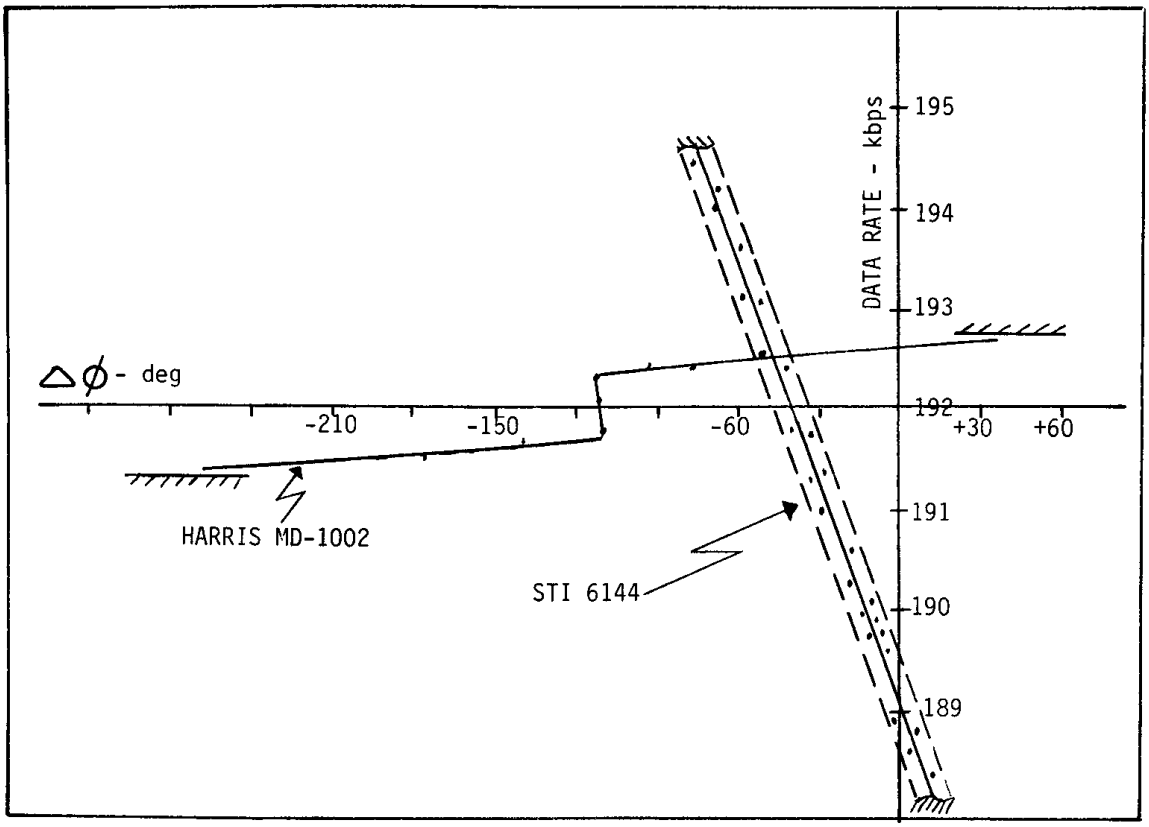

Figure 13. Modem Data Rate Tracking Range

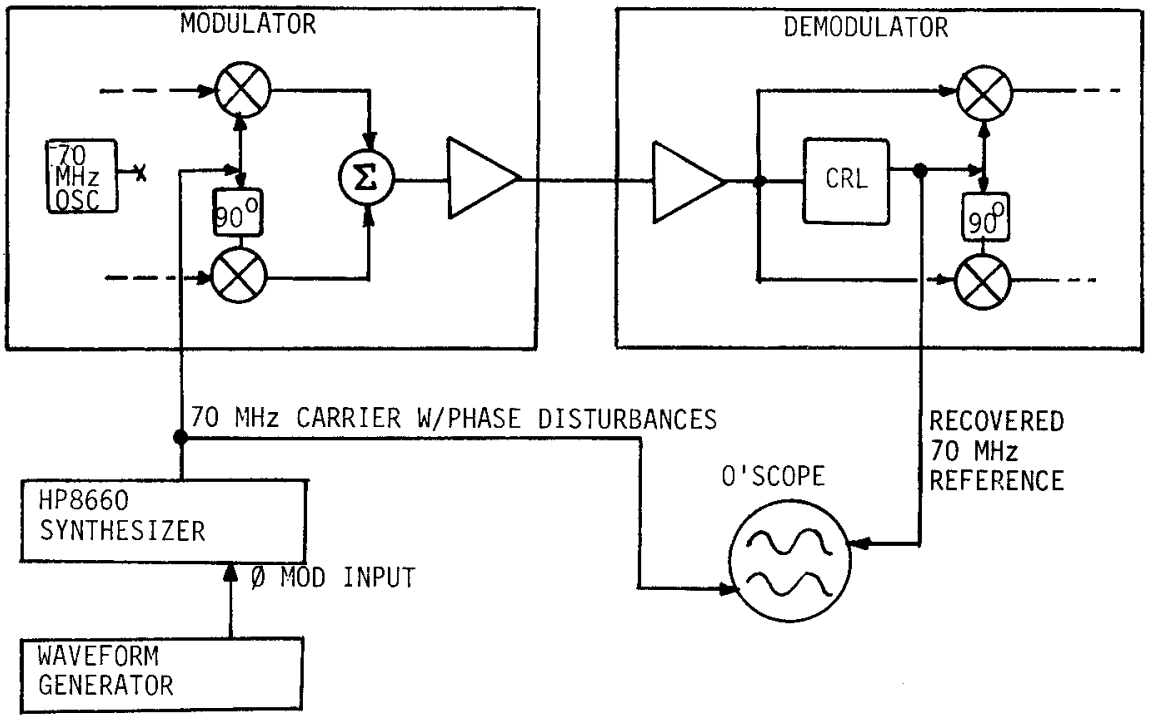

Figure 14. RF Phase Error Sensitivity Tests

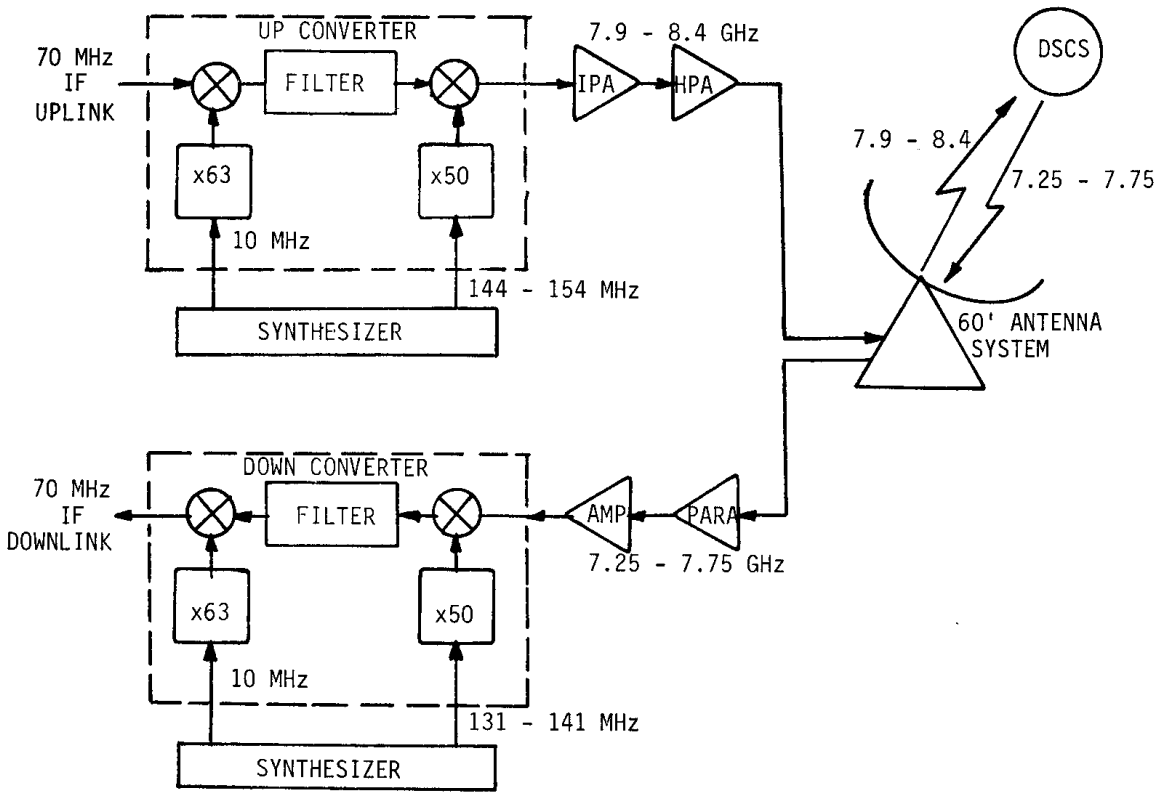

Figure 15. Typical DSCS Ground Terminal