NEXT GENERATION FUNCTIONAL COMPONENTS FOR SPACE TELEMETRY DATA PROCESSING

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ABSTRACT

Space telemetry data processing elements for flight and ground systems are currently developed using discrete components on a project-by-project basis. The adoption of various standards, such as those recommended by the Consultative Committee for Space Data Systems (CCSDS), brings commonality of requirements across future NASA communications elements and affords the opportunity to create standard components to meet these requirements.

Over the past five years, NASA's Goddard Space Flight Center (GSFC) has developed a series of high performance Very Large Scale Integration (VLSI) components for space data systems. These standard components have enabled the development of high performance data systems that are an order of magnitude more compact and cost effective than systems of the previous generation. Recent advances in design automation tools and integrated circuit densities have yielded the means to achieve yet another leap in the integration levels, performance and cost reduction of space data systems. Design automation tools can generate complex integrated circuit designs from high level technology independent functional descriptions. A single reusable functional description can be targeted to a variety of circuit technologies including CMOS, ECL and GaAs. With available densities of over 1 million integrated transistors in both CMOS and GaAs technologies, standard components integrating multiple processing elements are realizable for both flight and ground projects.

This paper describes the ongoing efforts of the Microelectronics Systems Branch at GSFC to create highly integrated components to meet functions outlined by the CCSDS using design automation techniques.

INTRODUCTION

In order to serve an expanding community of space data users in an era of tightening budgets, NASA space data transport and processing functions must become broadly available to users at low cost. Currently, most telemetry data processing systems for flight and ground elements are developed uniquely for each new project. Project resource limitations often constrain data systems to meet only the specific functional and performance requirements of their mission. These project oriented data systems lack the flexibility and generic capabilities for subsequent missions and, therefore, are very rarely reused. This mission-unique development cycle leads to very high costs for implementation and maintenance of telemetry data systems on a NASA-wide basis. As the number of space data users increases, the required functionality and bandwidth of data systems also increases which further drives up their cost. Under the current development cycle and budget constraints, telemetry data system costs will limit user access and, thereby, limit the full potential of future space missions.

The adoption of international space data transfer and processing standards, such as those outlined by the CCSDS, promises great potential for significant cost savings across all future NASA flight and ground acquisition and processing systems. Because the CCSDS recommendations provide a commonality of functional and performance requirements across future communications elements, an opportunity arises to meet NASA data system needs with fewer unique system designs. By partitioning and targeting CCSDS functionality into standard modular components, flexible data system architectures can be created that can be configured to meet a broad range of project requirements. The reuse of these genetic data system architectures will provide a significant savings in cost, time and manpower in the areas of design, integration and test of subsequent projects. Standard components implemented using VLSI technology will further reduce manufacturing and maintenance costs through economies of scale. Additionally, VLSI standard components will improve the performance and reliability of space data systems while reducing their size and power consumption. The current commercial electronics and computer industries offer ample evidence of the level of improvement possible in cost, performance, size and reliability when high integration and standardization are used.

The Microelectronics Systems Branch of the Data Systems Technology Division of NASA Goddard Space Flight Center (GSFC) has been developing low cost data systems from generic standard components for a number of years. This approach, referred to as the "Functional Components Approach", has produced front-end ground telemetry data systems for such NASA projects as the Topographical Explorer (TOPEX), Small Explorer (SMEX) and the Deep Space Network (DSN). The backbone of this approach is a set of more than a dozen VLSI Application Specific

Integrated Circuits (ASICs). These VLSI ASICs are integrated into larger standard functional (board-level) components to create a library of generic reusable processing elements. The current library contains some fourteen different standard components which implement such functions as frame synchronization, Reed-Solomon decoding and packet processing. By selecting the appropriate standard hardware components and configuring them with modular software components in an open bus system environment, low cost "mission specific" ground telemetry systems can be created.

Within the Microelectronics Systems Branch, new integrated circuit design methodologies are being adopted that foster design reuse and increase designer productivity. The new methodologies, based upon Hardware Description Languages (HDLs) and automated logic synthesis, are being used to create a new series of very high density ASICs. The very high density ASICs will serve as a basis for the next generation of functional components which will further integrate space data processing functions into smaller and less expensive functional units. The creation of these next generation functional components and the techniques used to create them are the subject of this paper. First, we start with the motivation to move to a new design methodology and a description of the HDL-based design methodology adopted by the Microelectronics Systems Branch at GSFC within the context of a current ASIC design. We then describe ongoing development to create the first in a series of next generation functional components. Finally, we comment on plans for other next generation components and plans to reuse HDL designs in subsequent generations of components with successively higher integration levels.

A NEW DESIGN PARADIGM

Since the advent of integrated circuit technology in the late 1950s, the number of transistors on a chip has doubled approximately every two years. Today, individual chips can contain millions of transistors. In order to understand the operation of a complex chip, it is imperative to view the chip design at the proper level of abstraction. Otherwise, it is easy to get lost in an overwhelming amount of detail. In the same light, the timely and cost effective design of complex chips requires working at the proper level of abstraction. Through the years, integrated circuit design methodologies have followed the trend of moving design to higher levels of abstraction through software automation. The graph contained in Figure 1 illustrates this point.

As fabrication technology has evolved to allow greater chip complexity, the development of Computer Aided Design (CAD) software has allowed designers to economically design more complex chips. In the 1960s, integrated circuits were

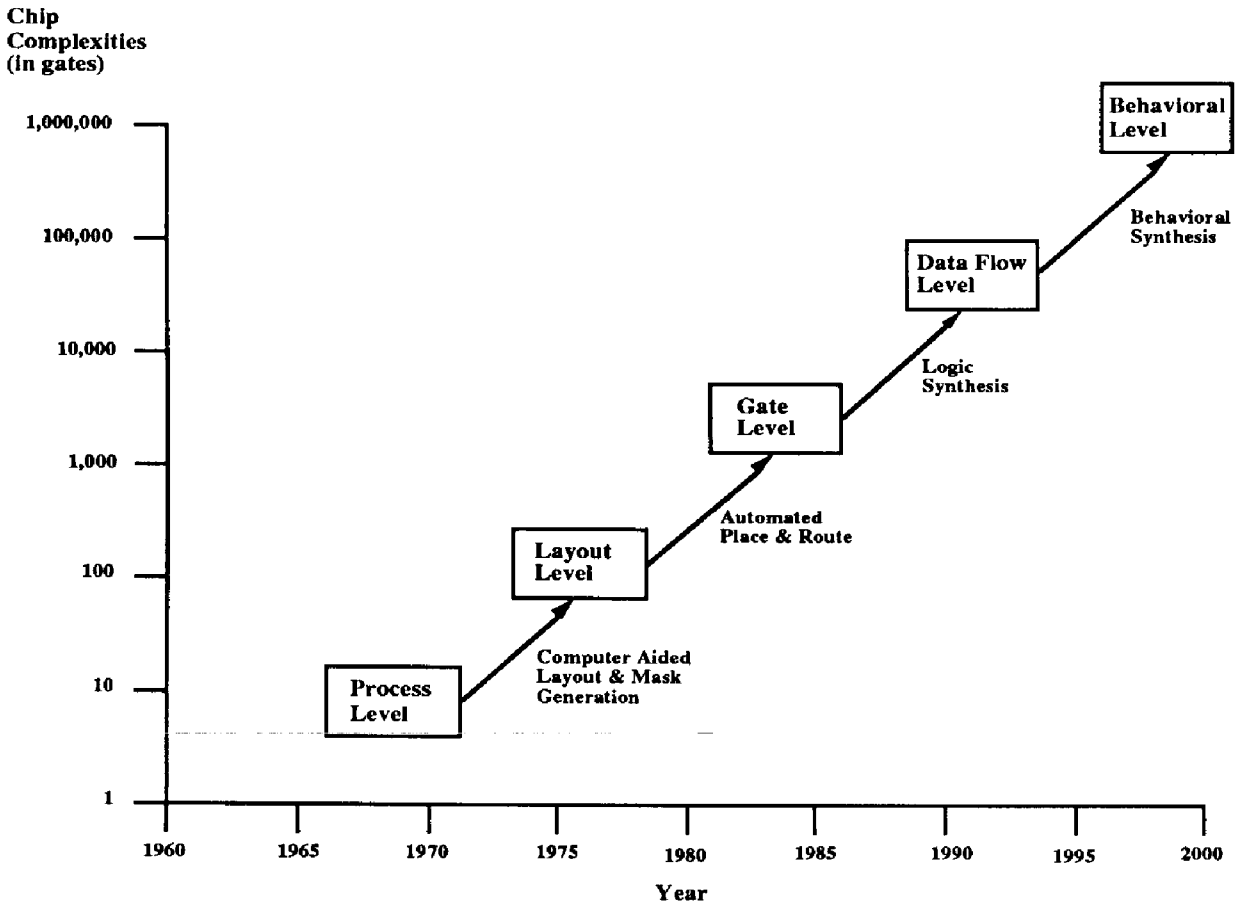

Figure 1. The Impact of Software Automation on Integrated Circuit Design

fabricated from hand generated artwork used to create process mask layers. In the 1970s, CAD software automated the representation and manipulation of geometric objects and provided computer-aided chip layout. In the 1980s, gate-level schematic capture and automated component place and route software brought the abstraction of chip design to VLSI levels. While schematic capture is now commonly used to design integrated circuits with complexities up to 20,000 gates, the capability of fabrication technology has extended well beyond 100,000 gates. Using a schematic capture approach, the design costs of creating chips at current fabrication levels can quickly overwhelm most organizations.

A methodology that couples HDL design with synthesis, referred to as HDL synthesis, can provide the further abstraction and automation required to economically design and manage circuits of this complexity. HDLs are text-based languages that provide designers with the ability to describe and validate a hardware element's architectural and functional characteristics in an abstract technology independent format. Logic synthesis tools provide an automated mechanism of transforming HDL code into an optimized gate-level representation targeted for a specific circuit technology.

Not only does this type of automation increase a designer's productivity, but it also promotes design reuse. Because computer software can quickly perform the technology mapping and optimization, a design can be automatically retargeted to a variety of circuit technologies or reused in subsequent designs at higher levels of integration. Synthesis libraries are now available for a number of commercial and radiation hardened (rad hard) processes in both Silicon and Gallium Arsenide (GaAs) technologies. At modest additional cost, flight qualifiable ASICs can be created that are functionally identical to ground processing components.

The Microelectronics Systems Branch has elected to use a synthesis approach based upon the VHSIC Hardware Description Language (VHDL). While there are many HDLs in existence today, VHDL was selected because it is an industry standard and is the most widely supported hardware description language. Our design approach, which is typical of HDL synthesis methodologies in general, is depicted in Figure 2. It is shown in the context of a single chip generic frame synchronizer planned for use in the first next generation of functional component. The frame synchronizer chip, when combined with a compact CPU module and memory elements, is intended to replace a current card-level component.

The design process starts with a general functional and performance requirements specification. In the case of the frame synchronizer, we require generic functionality at a full spectrum of operating rates. By targeting this frame synchronizer to two different fabrication technologies, we can supply system developers with a choice of performance and cost solutions. Since the goal is a single chip implementation, fabrication processes are selected that support very high integration levels. For low cost frame synchronization at rates less than 50 Mbps, a chip will be fabricated using a 0.7 micron silicon Complementary Metal Oxide Semiconductor (CMOS) process. For rates greater than 50 Mbps, we will use a 0.6 micron GaAs Metal Semiconductor Field Effect Transistor (MESFET) process. The same functional design will yield two parts in only a little more time than it takes to design one.

From the requirements, a top level design hierarchy containing the major functional modules of the design is created. A preliminary block floorplan often helps to efficiently partition a design. The next step is to write VHDL code for each individual module. This VHDL code is written at a data-flow level of abstraction, known as the Register Transfer Level (RTL). RTL code has a definite, implied architecture. Although VHDL can be used to describe designs behaviorally with no implied architecture, current synthesis tools cannot automatically translate behavioral descriptions.

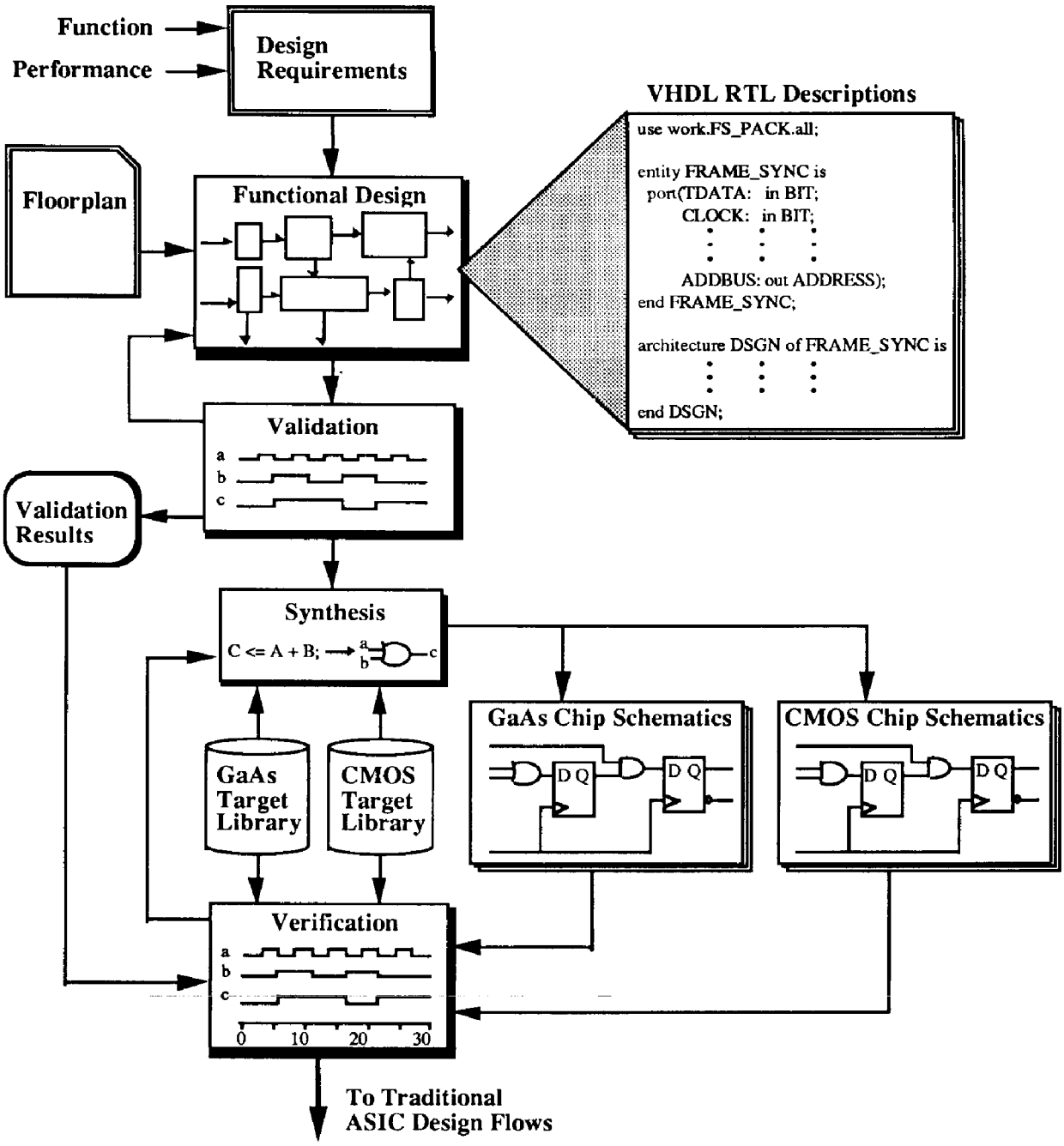

Figure 2. VHDL Synthesis ASIC Design Flow

After an RTL description has been entered, functional validation is performed using simulation. Typically, validation proceeds in a bottom-up manner with each module being "unit" tested to ensure desired operation. After all the functional modules have been validated, they are assembled for a full validation of the design.

Once an RTL design is validated, then it is ready for the synthesis phase of the design cycle. Synthesis translates the RTL VHDL code into a gate level representation.

Synthesis also performs optimization on the design with respect to a particular set of performance goals and the target technology library. Test synthesis tools can also be used to automatically insert test structures into the design and generate high coverage fault vectors. In the case of the frame synchronizer, we are actually translating and optimizing the design twice; once for a CMOS chip and again for a GaAs chip. Prior to verification, chip-specific features such as I/O buffers are manually added to the design.

Verification is an automated process that performs gate-level simulation and compares the simulations with the validation results. It also performs timing analysis including critical path analysis. Its primary purpose is to ensure that functionality is achieved and performance goals are met. If chip specifications are not met, then the design is either reoptimized or the RTL architecture is modified to meet design goals. For the frame synchronizer parts, each chip will have its own verification phase. Verification is where HDL synthesis methodologies coincide with traditional design approaches. After verification, the two chip designs continue to flow through traditional design processes prior to fabrication. These processes include layout, post-layout verification and mask generation.

In the future, the same Frame Synchronizer VHDL functional design may also be targeted to a rad hard flight qualifiable CMOS fabrication process. Several rad hard processes are presently available that can integrate over 50,000 gates on a single device. The availability of integrated flight components will allow flight system developers to take advantage of the same performance gains and cost reduction gained in ground data systems.

A NEXT GENERATION FUNCTIONAL COMPONENT

An effort is currently under way to develop the first next generation functional component, a single card CCSDS return-link telemetry processor. This next generation component integrates the functionality of three current generation components into a single 9 U VME bus card. A high level functional block diagram of the CCSDS return-link card is shown below in Figure 3.

The card is functionally separated into the Channel Controller CPU (CCC), Telemetry Simulator module and a pipeline of telemetry processing modules. The telemetry processing modules consist of the Frame Synchronizer, Reed-Solomon Decoder and Packet Processor modules. In order to achieve the integration levels for a single card implementation, the modules will be created using very high density HDL-designed ASICs, compact CPUs and memory elements. Current effort is centered on the development of these ASIC components; one of which is the Frame Synchronizer chip mentioned in the previous section.

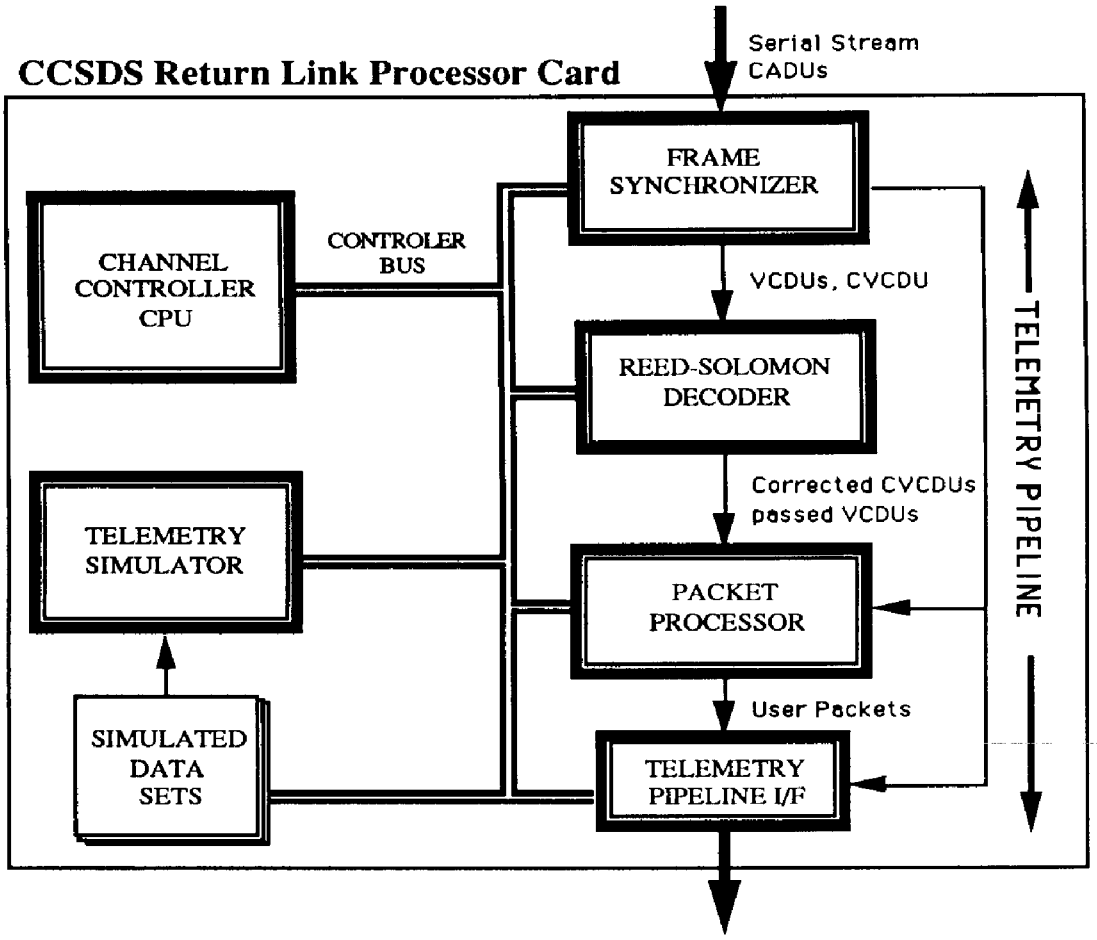

Figure 3 - Return Link Processor Functional Diagram

The card is planned to function in the following manner. Upon bootup, the CCC performs a diagnostic self-test on the card. The CCC sets up each module and issues instructions to the Telemetry Simulator to perform testing. The Telemetry Simulator tests each module using a variety of simulated telemetry data. To determine proper functioning, a module's output data and status are compared against expected results. After successful unit testing, different segments of the processing pipeline are tested in a similar fashion.

Prior to accepting telemetry data, the CCC downloads a session setup catalog to each module. Setup data consists of hardware parameters and software executable code required to process data for a specific mission or session. For example on the Frame Synchronizer module, some of the downloadable hardware parameters include the sync pattern, sync acquisition strategy, error tolerances and Cyclic Redundancy Check decoding algorithms.

After setup, each module is ready to process data. The Frame Synchronizer delimits an incoming stream of data into framed units based upon a setup acquisition strategy.

It also performs a number of other functions including bit transition density decoding, data inversion and reversal correction. Frame data and status are then passed through a First-In-First-Out (FIFO) buffer to either the Reed-Solomon Decoder or the Packet Processing module.

Upon receiving data, the Reed-Solomon Decoder determines which type of frame it is processing (encoded or unencoded). It then performs any necessary frame and header error correction including deinterleaving and delivers corrected data and status to the Packet Processor module.

The Packet Processor module is actually a general-purpose protocol convener. When configured for CCSDS data processing, the Packet Processor first extracts frame and packet headers from received data. It then validates the header IDs, checks data integrity and reassembles users packets. User packets including an optional routing header are delivered to the output of the card.

Each of the modules also supplies the CCC with cumulative quality monitoring. The CCC accesses this information through a dual port memory located in each module. The CCC formats the status and passes it to the next higher system controller.

Besides the Return-Link Processor card, there are plans to create a number of other next generation components. Single card functional components for forward-link processing, data take processing and catalogue / database processing are being contemplated. These highly integrated generic components will offer the functionality and performance needed to support the requirements of a number of present and future missions. The low cost of these components will make ground data handling systems readily available to most organizations.

THE EVOLUTION OF TELEMETRY SYSTEMS

Past methods for providing telemetry processing functions involved the use of medium scale integration subsystems consuming multiple cards and racks of equipment. The current generation of functional components has integrated subsystems into single standard bus cards through VLSI technology. The next generation of functional components will continue the evolution of integrating larger system elements into smaller, less costly functional units. Eventually, these components will be replaced by higher performance systems that are even smaller and cost less. This progression to higher levels of integration is a natural evolution of electronic systems. Figure 4 demonstrates this evolution and its potential impact on future telemetry data systems.

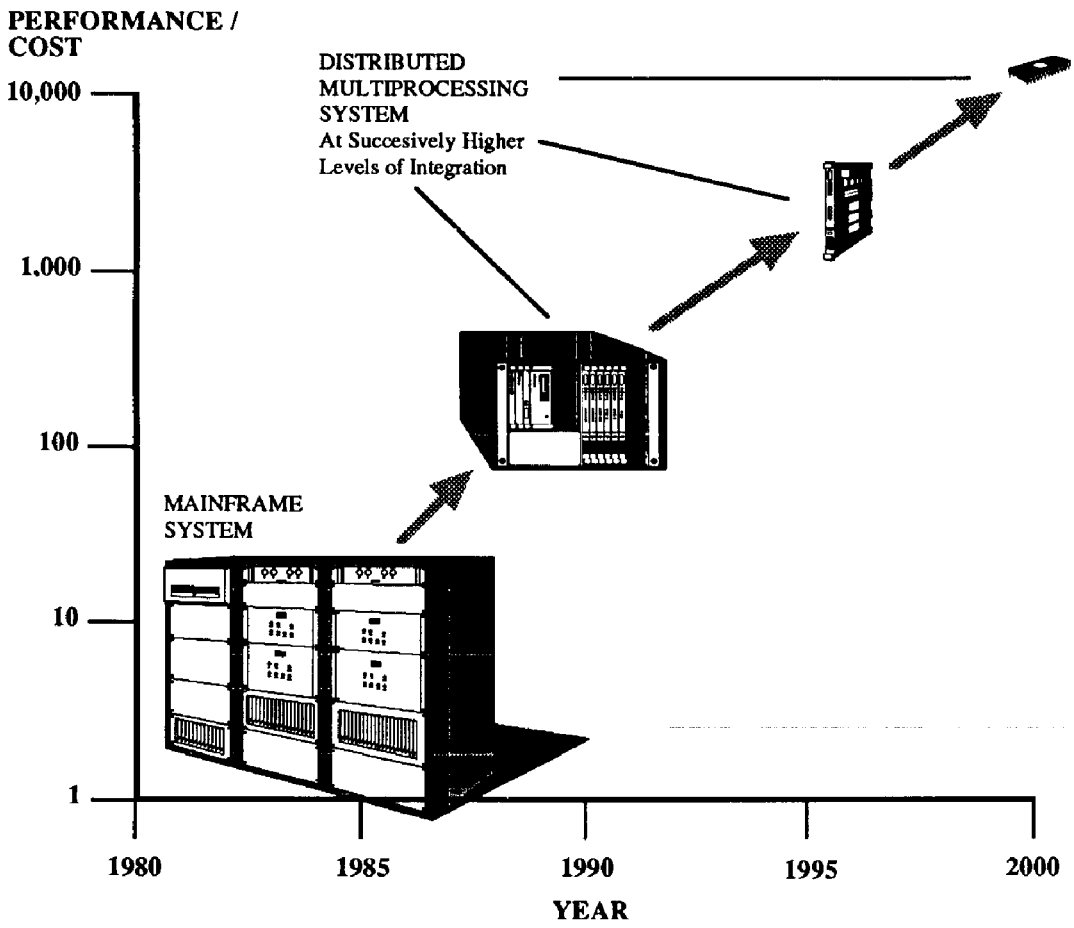

Figure 4. The Impact of Integration on Telemetry Systems

With an HDL Synthesis design methodology, this natural evolution toward higher levels of integration can be efficiently applied to telemetry data systems. The VHDL descriptions of ASICs being designed today can be reused to economically create future ASICs of even higher integration levels. Several VHDL chip designs can be merged, synthesized and fabricated into a single higher integration chip. Thus, advances in circuit fabrication technology can be taken advantage of without significantly repeating design work. Using this method, the Return-Link Processor card may undergo additional iterations. Several return-link channels may be put on a single card by merging VHDL designs and using denser implementations.

In the not too distant future, even commercial CPUs may be included with VHDL designs to create single ASICs. Several vendors presently offer Reduced Instruction Set Computer (RISC) processor designs for embedding in their ASIC implementations. The major drawbacks of utilizing these processor designs is that they arc expensive, technology dependent and vendor specific. However, ASICs with embedded processors will be practical when standard VHDL CPU designs become readily available.

CONCLUSION

The Microelectronics Systems Branch at GSFC is using new design methodologies to continue the evolution of telemetry data systems to higher levels of integration. Hardware Description Languages and automated logic synthesis tools are being used to create very dense ASICs that generically implement telemetry processing functions. The ASICs will enable the development of a new generation of functional components; each of which integrate several telemetry processing subsystems into a single card. The availability of these open bus card components win offer system developers continued improvement in the performance and economy of ground telemetry data systems.

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NOMENCLATURE

ASIC	Application Specific Integrated Circuit
CCSDS	Consultative Committee for Space Data Systems
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CCC	Channel Controller CPU
CVCDU	Coded Virtual Channel Data Unit
DSN	Deep Space Network
ECL	Emitter Coupled Logic
FIFO	First-In First-Out
GaAs	Gallium Arsenide
GSFC	Goddard Space Flight Center
HDL	Hardware Description Language

I/0	Input/Output
Mbps	Megabits per second
MESFET	Metal Semiconductor Field Effect Transistor
NASA	National Aeronautics and Space Administration
RISC	Reduced Intruction Set Computer
RTL	Register Transfer Level
SMEX	Small Explorer
TOPEX	Topographical Explorer
VCDU	Virtual Channel Data Unit
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuits
VLSI	Very Large Scale Integration
VME	Versa Module Euro
ULSI	Ultra Large Scale Integration