MODERN TECHNIQUES FOR MONITORING AIRBORNE TELEMETRY

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ABSTRACT

The testing and integration of modern avionic systems is facing us with new dimensions of complexity and sophistication. A smaller, faster avionic distributed processing system and small airborne spaces are demanding a new, innovative way to handle the telemetry requirements.

The various types of data, ranging from analog values like temperature, vibrations, pressure and bi-level signals, up to the contents of fast buses like the MIL-STD-1553B and/or distributed multi-processor systems (performing calculations of a distributed nature) challenge the telemetry engineer coping with this task in the most efficient way.

INTRODUCTION

The telemetry realm Airborne and Ground stations methodologies have changed very little in the last 10-15 years.

The traditional way of collecting airborne data, mostly analog, via multiplexers, or monitoring a serial bus like the MIL-STD-1553B and transmitting it to the ground telemetry station is not enough for the elementary modern avionic system.

A typical airborne instrumentation system consists of the following components:

- Sensors - Temperature, vibrations, pressure, linear bilevels, etc.
- PCM multiplexers with A/B multichannel capability.
- Recorders or transmitters.

The purpose of this paper is to present a new concept of integrating the various sensors, buses and distributed processing subsystems into a single telemetry serial bus, utilizing a unique approach of a master/slave configuration.

A TYPICAL AIRBORNE SYSTEM

A common airborne system is composed of analog/digital sensors, avionic subsystems interconnected via MIL-STD-1553B buses and various satellite systems connected to the main avionics via discrete lines.

The various avionics systems such as Radars, Navigational systems, computers and other subsystems are distributed among the different avionic buses.

A stereotype subsystem may be composed from several CPUs tied together via an internal bus such as VME, MULTIBUS-11, or π bus.

The variety of internal information exchanged among the processors is invisible to the outside world (i.e. the MIL-STD-1553B which interconnects the avionics subsystems externally to the modules). This information is essential for the avionic developer during the integration and fly test periods.

The existing methods of collecting the data will involve several collecting links and thus several transmitters or recording channels.

THE INTEGRATED APPROACH

The heart of this approach is an MLM designed PCM Frame Formatter (PFF) VLSI chip. This PFF may be installed in each subsystem, CPU board or PCM multiplexer.

This formatter can operate as a stand-alone device in a single acquisition system, or be networked in a master/slave architecture.

By cascading several PFFs together, it is possible to build a flexible data acquisition system network.

The PFF is incorporated into the PCM multiplexer, configured to operate as a master on the PCM bus while the other PFFs are assembled on the various CPU boards. The PFF appears to the local controller on each board as a memory mapped device. The local controller initializes the VLSI formatter to the proper operational mode (Master/Slave, Frame size, Sync pattern, etc).

From this point it operates autonomously, transmitting the data supplied by the local CPU to the PCM bus according to the master formatter commands.

The 1553 to PCM controller (MPI) is also configured to operate as a slave on this PCM bus (Figure 4). This is equipped with FIFOs and timers and can be initialized as a selective monitor on the multiple 1553 buses.

The PCM Formatter can be used also in the software development phase, monitoring software debugging.

The system operates as follows:

The master formatter on the main multiplexer instructs each device as to the time to put its information, in serial form, on the PCM bus. In its own time slot it adds the digitized analog and bi-level information that has been collected by the master.

The pre-modulation function is also performed in the main multiplexer. In this way, various types of data are integrated into one stream, composed from sensors output, events, 1553 bus and CPU distributed data and is transmitted to the ground telemetry station to be recorded on a single channel.

The example in Figure 3 illustrates the PFF interconnection scheme for multiple processor architecture as used in one of MLM system designs. It should be noticed that two of the PFFs are in the slave mode while the third one is a master on this network.

THE PCM FRAME FORMATTER (PFF/8)

The VLSI frame formatter block diagram as described in Figure 4 is divided into the following main blocks:

- Host Interface Module
- Sequencer Module
- Data RAM
- Frame Format RAM
- PCM Bus Interface Module

The Host Interface module is used to initialize the VLSI as to the operating mode and status monitoring. The sequencer module performs control functions according to the sequence needed to move the data in and out of the chip. The Data RAM is a dual buffered device which is loaded by the telemetry data to be transferred to the PCH bus. The Frame Format RAM contains the structure of the PCM frame for that device.

The PCM Bus Interface module interfaces to the external PCM bus.

Highlights:

- ❑ All PCM frame parameters can be programmed
- ❑ Appears as a regular RAM to the local controller
- ❑ Flexible frame format and word length
- ❑ Easily interfaces to the popular microprocessors
- ❑ Transmits data rates from I Hz to 8 MHz using internal clock
- ❑ Accepts separate external bit rates clock
- ❑ Accommodates several outputs formats such as NRZ-L, NRZ-M, NRZ-S, Bi-PHASE and VITERBI coded 3/4, ½ data
- ❑ Acts as master or slave unit
- ❑ Enables frame format changes during mission
- ❑ Has a self-test built-in capability
- ❑ Single power supply 5 volts, 0.15 watt, 68 PGA package

MPI - MUXBUS TO PCM INTERFACE

The MPI module implements all IRIG 106-86 chapter 8 “MIL-STD-1553” requirements in a flexible, modular design approach. Up to 8 dual redundant 1553B buses can be incorporated into a single PCM stream and sent out. The module provides up to 4 serial outputs to multi-track tape recorder (RNRZ or BIO modulated).

MPI can be configured as a standalone formatter or a slave device on the PCM system bus. In the last case, 1553 data will be transmitted together with other system information as embedded frame. In order to utilize the PCM bus in an efficient way, all monitored 1553 data is stored in a 4K x 27 FIFO.

Highlights

- Intelligent 1553B message monitor enables:

  Word type recording (data, status, command)
  Extensive error reporting
  Message selectivity
  16 bit time tagging of each message
  16 bit response time attached to each message
  Functions as a Remote Terminal for software upload and testing

- Provides up to 8 Megabit/s TTL, NRZ-L and NRZ-S data formats

- Programmable frame length

- Messages are never cut by frame boundaries or filler words.

SUMMARY

A method of integrated telemetry approach was described coping with the modern needs of avionlc systems.

Two different approaches to the variable requirements of modern airborne telemetry needs were shown here. The advantages gained by the integrated method are clearly visible, saving space and allowing the user to reach into the internal world of data that was difficult to get until now.

The conservative way of coping with the requirements shown in the example, namely to use several data collecting systems with each one using its own transmitter or adding external submultiplexers, is very expensive in any imaginable way, complicating the data reduction and time synchronization between the various streams.

A new device is now in final design stages to give an answer to systems without the need of a local host. This device (PFC90) will operate in three modes:

a. With host computer (higher bit rate, identical to markl)

b. As standalone system for data collection

c. In high bit rate systems (digitized video).

The device is described in the appendix to this paper.

APPENDIX: THE PCM MARK II

1. GENERAL DESCRIPTION

The PFC90 (PCM Formatter/Controller-PFF8 mark2) is designed to perform the general PCM controller and formatter functions. The PFC90 acquires data In three different configurations:

1.1 Host-based System

The PFC90 is connected to a host as a memory mapped I/0. The host loads data to internal memory (512x16 RAM), which operates in double buffer mode like in markl.

1.2 Moderate Data Acquisition System

The PFC90 controls and acquires data from the simple data acquisition system that includes components for acquiring analog and bi-level input signals. In this mode, the PFC90 does not require any host. The PFC90 uses external memory which determines the data acquire and transmit sequencing.

By integrating the PFC90 with the external components in a hybrid form, there is a single module solution to a complete data acquisition.

1.3 Flexible Data Acquisition System

In this mode, the PFC90 acquires data from a host, as an inhost based system and from additional external memories. The PFC90 uses its internal memory for inputs and outputs sequencing then formats and transmits this data and sync words, serial to the RF transmitter. The external memory can be used for very fast data (video) transmission.

2. FEATURES

The PFC90 is implemented in a 1 micron HCMOS technology “cell” based array. It is packed in an 84 pin PGA. The PFC90 contains 1Kx16 bits RAM memory. One half of this memory is used for storage of the transmission formats, while the other half is used in the host driven configuration. The 512x16 RAM used for the data memory is divided into two buffers, in a flexible configuration. 128x16 is used for data and 384x16 is used for data acquisition format.

2.1 Host Based System (MARK 1]

The PFC90 appears as a RAM for the host system. The host can access the internal registers and the internal memories. During the initialization phase, the host loads the internal registers and the format memories and then instructs the device to start the transmission. In the transmission phase, the host loads data to the internal data memory which operates in double buffer mode.

When the chip terminates the transmission the buffer initiates an interrupt request and starts to transmit the other buffer. After the chip transmits a word from the buffer, it loads it with a filler word, if required. The chip allows each word in the minor frame to transmit the filler word or the old data word, in cases when the data in the buffer is not updated.

The chip contains an internal interrupt controller which interrupts the host when at least one of the following events occur:

- ❑ Terminate transmitting data buffer
- ❑ Master reset command
- ❑ Master message
- ❑ Selftest fault.

2.2 Autonomous System

The PFC90 supplies the interface to the data acquisition system components.

The PFC90 uses external memory (EPROM) that keeps the content of the internal registers, the content of the transmission format memories and the content of the acquisition formats memory. During “POWER ON RESET” the PFC90 self initializes

the internal registers and the transmission formats memories and then starts the transmission mode. During the transmission the device reads the acquisition format—one instruction per sample time, for controlling and acquiring data from the data acquisition components.

The chip supports multiple formats by defining a schedule of formats in the external memory. The memory (EPROM) can be programmed by an external programmer/PC or microcomputer, on-board without disassembly.

2.3 Slow Mode Acquisition System

This mode supports a system with one “SAMPLE/HOLD” component. The chip acquires data in two phases.

In the first phase the channel is selected, the address and the type of channel are loaded to the external latch, by the PFC90 and the S/H component is set to sample state, controlled by the S/H pin.

The second phase holds the sampling value while the S/H is in “HOLD” state and instructs the A/D to start the conversion. When the conversion is terminated the result is read and loaded to the Sync Process Data Buffer (SPDB).

2.4 Fast Mode Acquisition System

This mode supports the system with two “SAMPLE/HOLD” components. The chip acquires data in two stages, in pipeline configuration. The first stage samples the channel and the second one holds the previous sampling result, while the A/D makes the conversion. The PFC90 can also read data from discrete registers, to acquire bi-level input channels or any other data type stored in the memories or the registers.

2.5 Data Acquisition Interface (Video)

In this mode, the PFC90 acquires data from different types of external memories and from the host.

During the initialization phase the host initializes the internal registers, the transmission, and acquisition of the internal format memories. In the transmission phase the PFC90 gains the control on the I/0 bus and acquires data from the external memories.

This scheme is used for fast video (digitized pictures) transmission. The digitized video is stored in the external memories and from this point is cared for by the formatter.

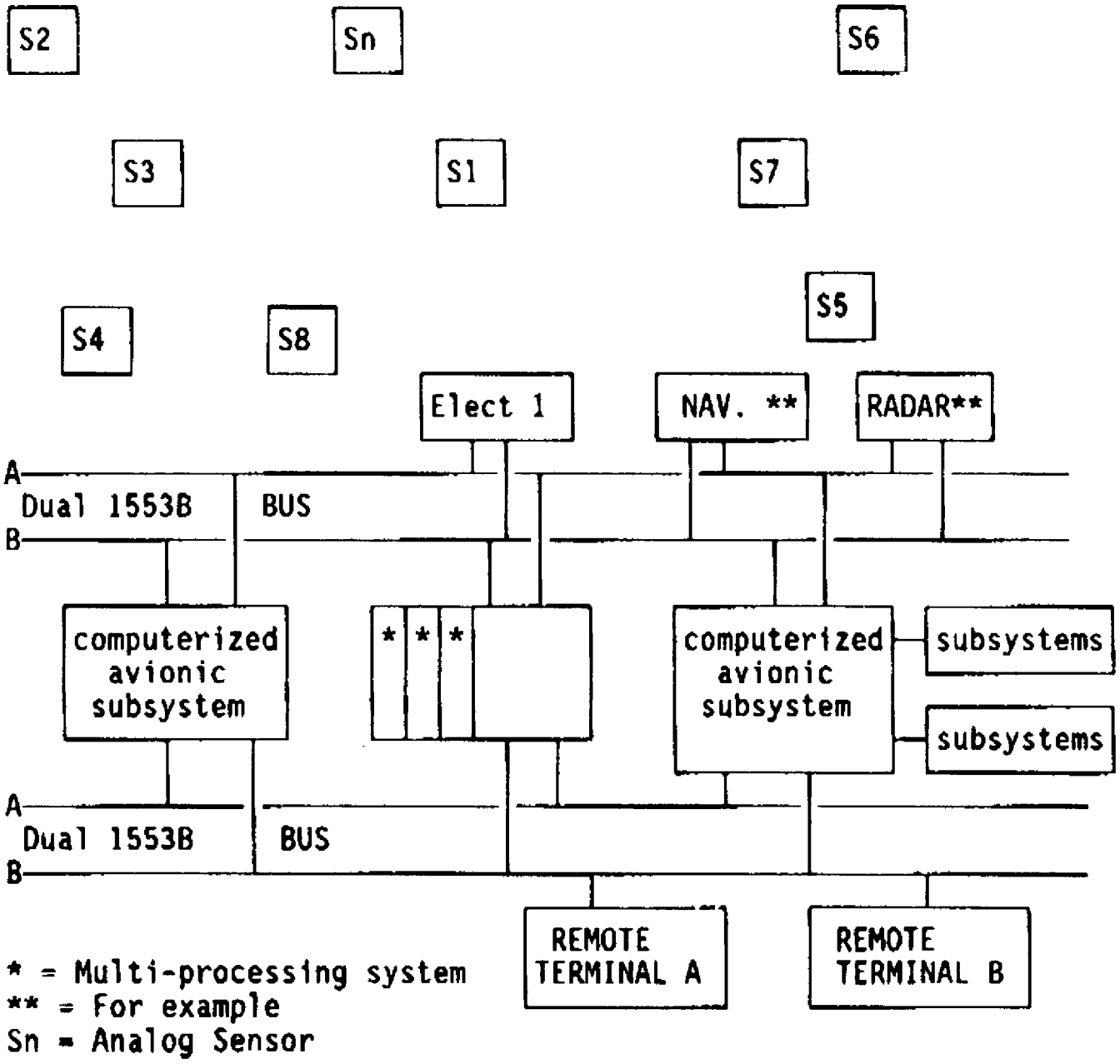

Fig.1: Typical Avionic System Data Acquisition Problem

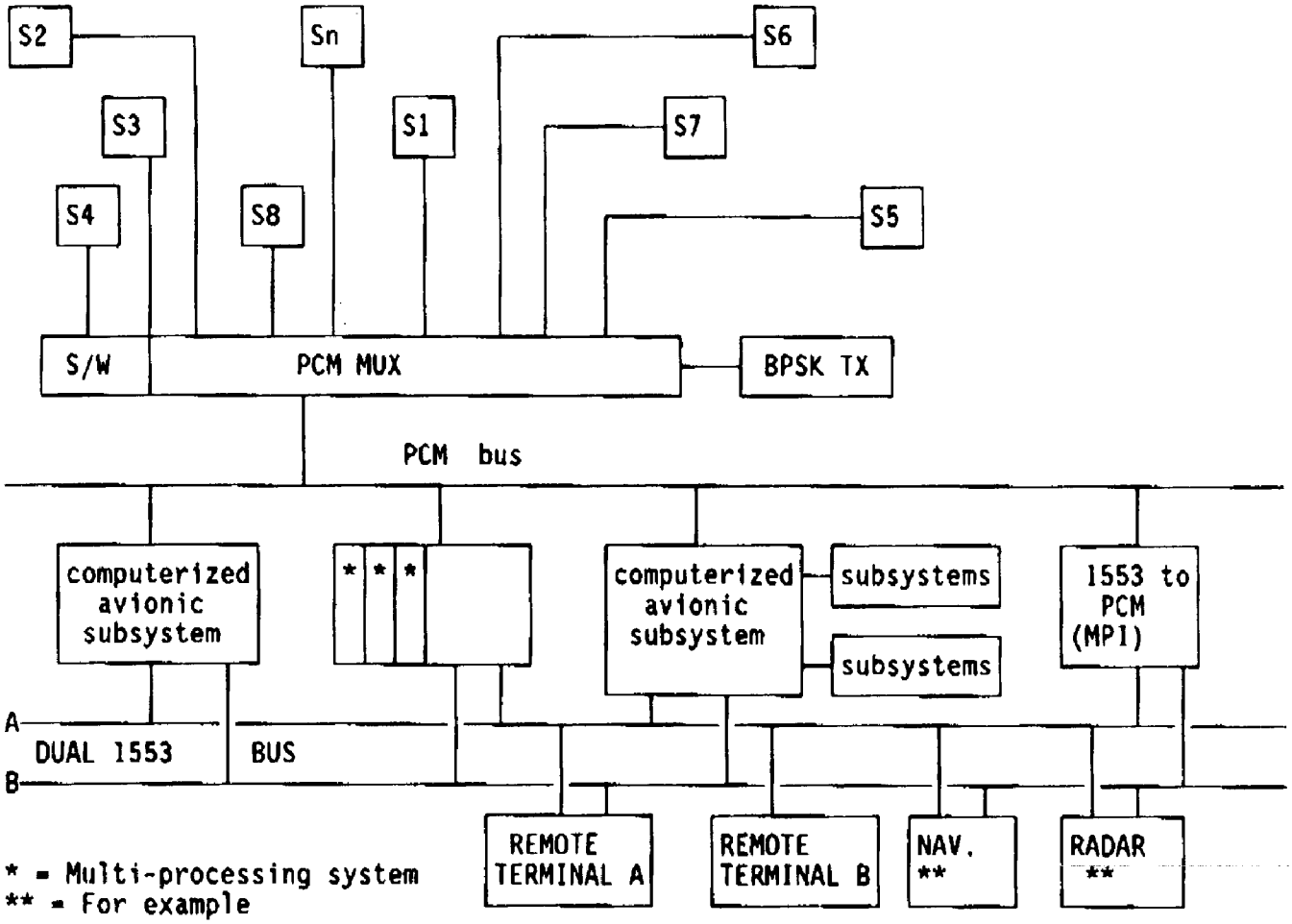

Fig.2: Typical Avionic System Data Acquisition Solution

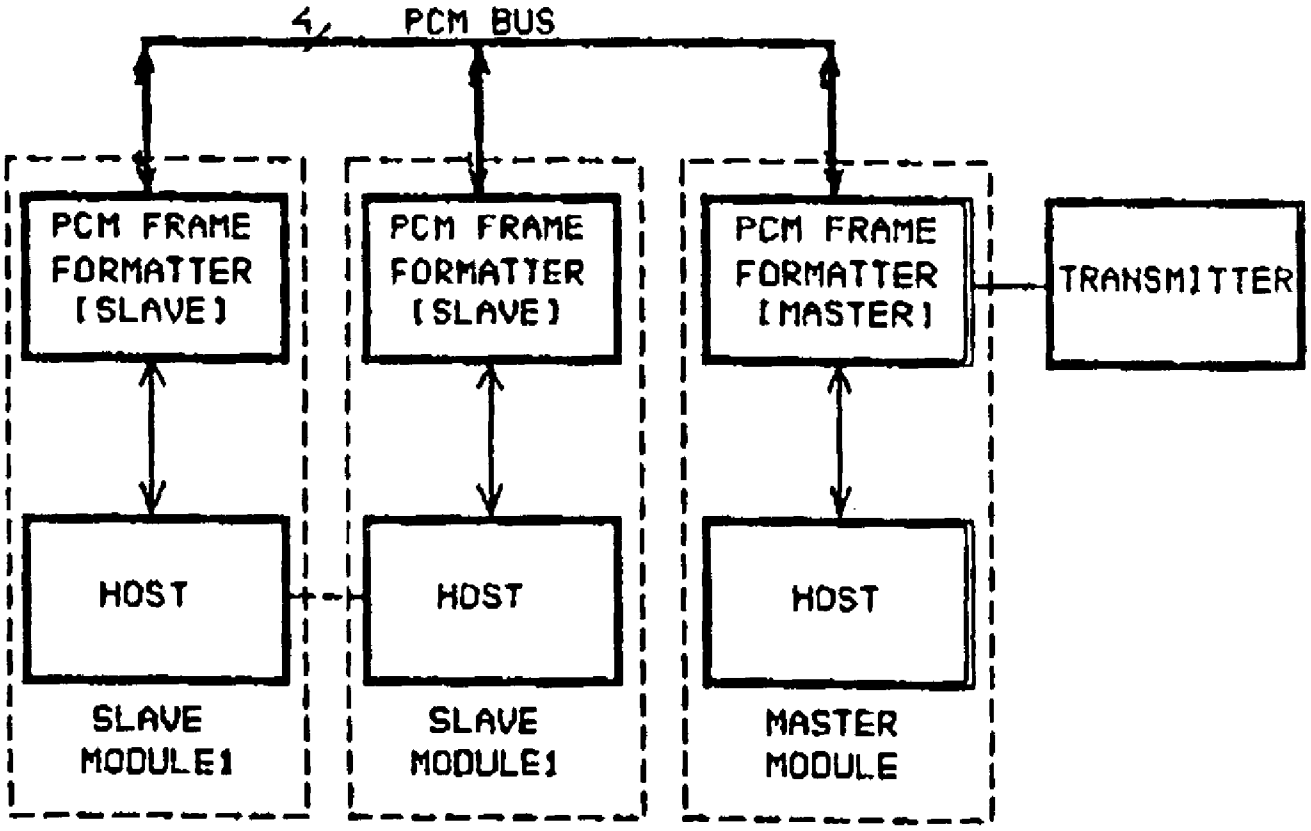

Fig.3: Multiple Processor Modules Configuration

- 4 WIRE MASTER/SLAVE BUS:
  - -WORD RATE-DEFINES THE TIME SLOT FOR A WORD INSERTION.
  - -BIT RATE-DEFINES THE TRANSMISSION BIT RATE
  - -MASTER SENT ADDRESSES & COMMANDS TO SLAVE
  - -DATA SENT BY THE SLAVE

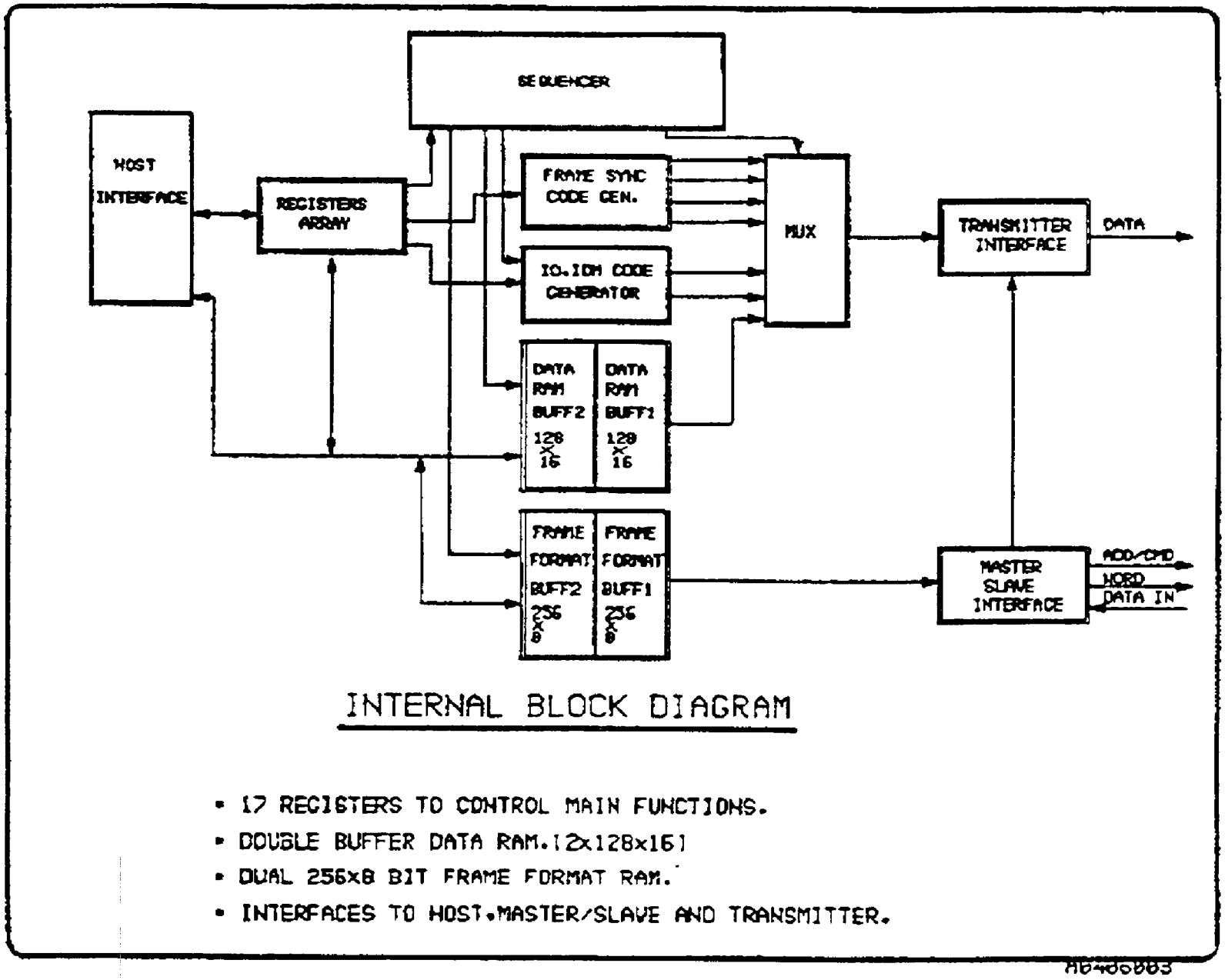

Fig.4: PFF8 - Block Diagram