A NUMERICAL CONTROL AND INFORMATION GATHERING TRANSMISSION SYSTEM

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ABSTRACT

This paper describes a numerical control and information gathering transmission system. The system is designed around an Intel MSC51 single chip microcomputer. The system has proven to be simple and dependable in a user environment. The system is described first, followed by descriptions of the hardware, the memory assignment, and the software strategy.

1.0 INTRODUCTION

The system described in this paper has been implemented in a hospital setting to allow for real time transmission of information throughout a local area. The system has proven to be robust and useful in its role.

2.0 SYSTEM INTRODUCTION AND USES

2.1 SYSTEM FORM AND FUNCTIONS

The system host machine is composed of the Numerical Controller (NUMC), the Analog Data Modulator/Demodulator (ADMD), and Command Inputs and States Output Device (CISO). The data transmission system is composed of the Signal Drive Device (SDD), the Control and States Bus Lines, and the Terminal Matched Filter (TMF). The Gathering and Control Elements (GCE) form the end user/machine interface. The system is illustrated in Figure 1.

The NUMC is the core of the system. It controls the ADMD, the GCE, and awaits input from the central user interface. It stores the GCE status data, modifies the system time, and writes the status data and system time to the display device (a CRT display).

The ADMD receives control signals from the digital controller. The ADMD works in one of three states: conductance, cut-off, and keep watch (wait). It communicates with all of the elements. In this paper, the ADMD is used as a voice modulator/demodulator that can communicate with one or more of the GCEs.

The CISO allows data interfaces with outside systems. For this paper, the outside data interfaces are a keyboard and a CRT display.

The SDD and the TMF are used to shape the signals on the data bus lines and provide an increase in the signal to noise ratio of the transmission system.

The GCE are remote processing systems. They decode address and function codes, execute fixed programs, and can relay GCE status data back to the host system. In addition, the GCE can store request status data and interrupt the system host to serve a request command.

3.0 HARDWARE DESCRIPTION

The NUMC is designed around a reliable industrial process control integrated circuit: the Intel MSC51. The NUMC is comprised of the MSC51, an address latch register, an address decoder, program memory, the analog signal mod/demod controller, data memory, the I/O interface, the data bus interface, and the even-odd check circuit. Figure 2 illustrates the NUMC design.

The NUMC primary features are:

- **8 bit CPU**
- **10 MHz external crystal**
- **46 data I/O lines**
- **three 16 bit software timers/event counters**
- **4kbytes EPROM**
- **512 byte RAM**
- **five 2-level interrupt priority structure**
- **programmable full duplex serial channel**
- **128 bit addressable RAM**

The NUMC works in one of three modes: (a) keyboard command, (b) time clock, © interrupt request from the GCEs. When working in the keyboard mode, the MSC51 uses an inquiry program to scan the keyboard for input. When working in the time clock mode, the timer can interrupt the MSC51 when it reaches a predetermined time count. The CPU then processes the interrupt program and can update the system memory or collect the GCE status data. When the GCE sends an interrupt signal to the MSC51, the GCE is polled for the GCE status data, and depending on the system program, the MSC51 can update or change the GCE status.

3.0 DATA PATHS

3.1 KEYBOARD COMMAND DATA PATH

When an operator pushes a key on the keyboard, a scan circuit sends a signal to the MSC51. Depending on the command, the MSC51 may change the state of the analog mod/demod, send(receive) data to(from) the GCE, or control the CRT interface circuit to provide feedback display to the operator.

3.2 TIME CLOCK DATA PATH

The 10 MHz oscillator generates a pulse waveform that is passed through a D-type flip-flop. The signal is then passed onto the external 16 bit timer of the MSC51. The external timer signal is passed onto the internal 16 bit timer of the MSC51 (to). After the timer reaches a time preset by the program, it can send an interrupt signal to the MSC51. The MSC51 can then write the system time and data to memory, start the timer again in the interrupt program, or collect the GCE status data.

3.3 GCE INTERRUPT DATA PATH

The GCE sendS interrupt signals that reach the data interface even-odd check circuit. The signal is passed to an invertor and the output of the invertor is passed to the MSC51 interrupt port. The interrupt program can examine the GCE interrupt code and subsequently update the state of the asking GCE.

4.0 GATHERING AND CONTROL ELEMENTS

The GCE are made up of the following parts: the unit code comparator, the function decoder, the even-odd check circuit, the request and sate register, and the analog/ digital receive and transmit controller. Figure 3 depicts the functional relationship.

The even-odd check circuit compares the data with the parity bit. When the comparison is true, the check circuit sends a true signal to the unit code comparator. The GCE which has a code that matches the code from the host system will be selected. The function decoder then decodes the signal from the host system. The decoded signal will then set or reset the control and state register which in turn controls the analog/digital into a receive or transmit state.

5.0 MEMORY DISTRIBUTION

The memory is divided into five parts in the NUMC:

- program memory in EPROM
- MSC51 internal RAM
- special function registers
- bit addressable RAM
- off-chip RAM

Figure 4 illustrates the memory mapping.

5.1 PROGRAM MEMORY

Programs are stored in the program memory. The program counter provides the address of the program memory in the MSC51. The MSC51 is capable of addressing up to 64 kbytes of program memory. However, the on-chip program memory is not used and 4 kbytes off-chip EPROM is used instead. The EPROM address range is from 0000H to 0FFFH.

5.2 INTERNAL MEMORY

The MSC51 has 128 bytes of on-chip data RAM. The internal RAM address is from 00H to 7FH. Different address regions have different functions. The functions are broken down

into: working register bank, direct addressed bit RAM area, and internal data bank. The memory was structured to integrate the address working register bank and the data bank. Addresses from 00H to 1FH are divied into four banks. Each bank has eight registers. The register banks are selected using the 3rd and 4th bit of the program state word. The correlation between the PSW state and the work register banks is shown in table 1.

PSW.4 (RS1)	PSW.3 (RS0)	CURRENT REGISTER
0	0	Register 0(00H-07H)
0	1	Register 1(08H-0FH)
1	0	Register 2(10H-17H)
1	1	Register 3(18H-1FH)

Table 1.

In the system, the states of RS0 and RS1 of the PSW can change to select one of the work register banks. Because of this, the system is capable to quick interrupt responses. If a register bank is not used, it can be used as data memory.

In this system the first work register bank is used as the keyboard command general purpose register. The second bank is used as the time clock general purpose register. The third bank is used as the elements service register. The fourth bank is the reserve register.

The other MSC51 internal memory bank is divided into two parts. One part is used as the stack memory (the base address is 47H). The other part of this memory is used as a special states memory (addresses between 30H and 46H). When the MSC51 is working on keyboard command interrupt processing, the PSW is written by PSW1 memory. When the MSC51 is working on time clock interrupt processing, the PSW is written by PSW2 memory. When the MSC51 is working on unit service interrupt processing, the PSW is written by PSW3 memory.

5.3 SPECIAL FUNCTION REGISTERS

The I/O latch, timer, serial port memory, control register, and states register are special function registers in the MSC51. They use internal memory at addresses 80H to FFH.

5.4 BIT ADDRESSED RAM

As in direct bit addressing, values between 0 and 127 (00H-7FH) define bits in the MSC51 internal RAM locations 20H - 2FH. These bits may be changed by software. The state of any of these bits may be tested for “true” or “false”. The program state making and bit control variable are put into these memory locations. In the present system, these bits are accessed by the service seeking program of the select and control units. These programs can read and write data.

Address bytes between 128 and 255 (80H-0FFH) define bits in a 2 x “special function” register address space. If no 2 x “special function” register corresponds to the direct bit address used, then the function is undefined.

5.5 EXTERNAL RAM AND INPUT/OUTPUT PORTS

RAM and I/O ports are addressed in the MSC51 64kbytes external RAM location. Addresses between 0000H and 00FFH define 256 bytes of RAM. Addresses between FF00H and FFFFH define I/O port addressing. The RAM memory is used to save restore state and control words of the GCE. I/O ports are used for data interface, even-odd check, the video display, the keyboard, and the printer.

6.0 SOFTWARE

6.1 KEYBOARD COMMAND MODE

In this mode, the keyboard is scanned for data input. The software is robust enough to overcome momentary “key mechanical shake” so as to avoid erroneous data input. Data scanned from the keyboard is relayed to the video display for operator feed back.

6.2 TIME CLOCK MODE

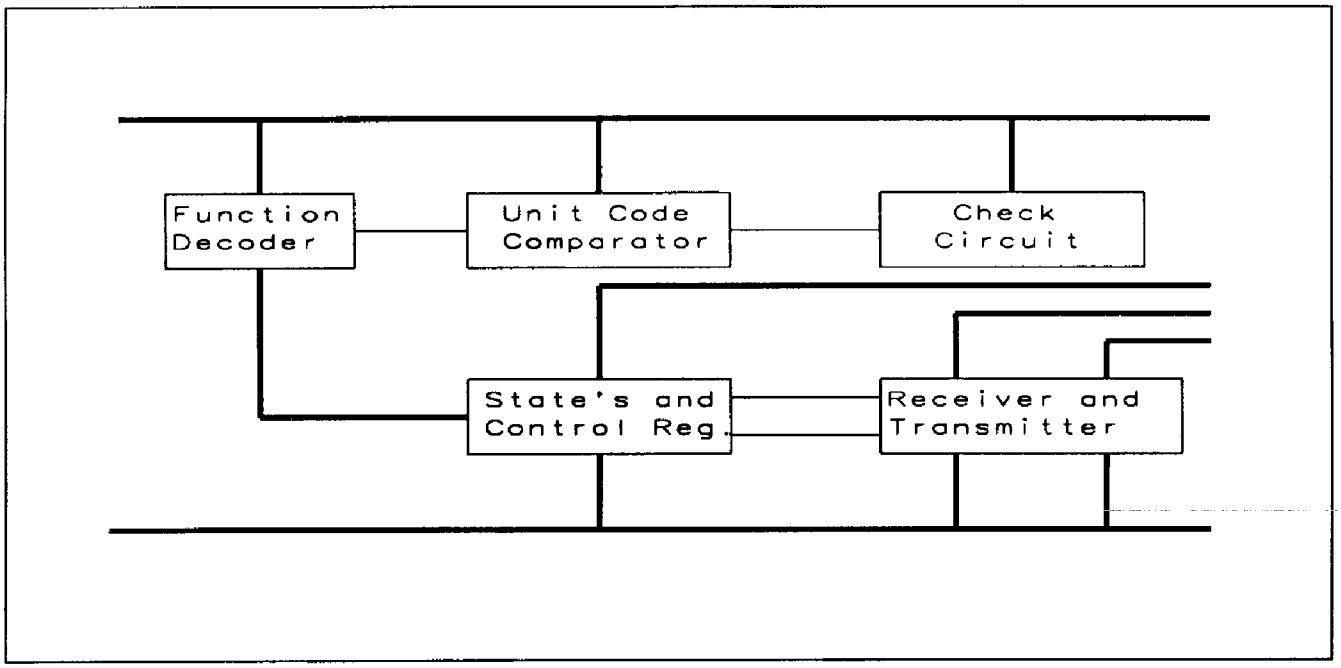
This is an interrupt driven software mode. This mode is used to execute various functions that must occur at precise times.

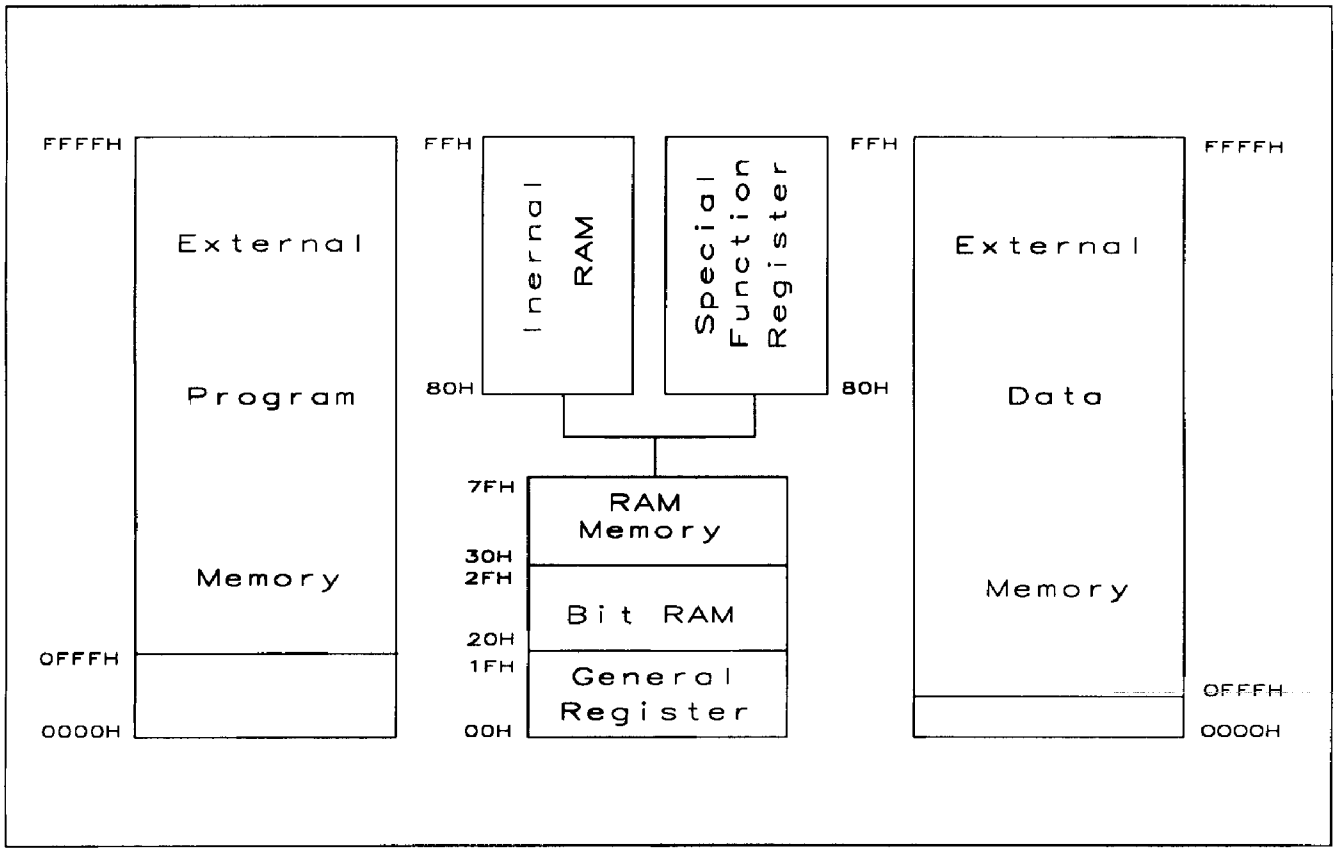
6.3 GATHERING AND CONTROL ELEMENT SERVICE MODE

This is an interrupt program that obtains the states of the various GCEs. It is different from the time clock mode. The time clock mode interrupt service routine masks the interrupt signal from the GCEs.

7.0 SUMMARY

This paper described the system design and characteristics of a numerical control and information gathering system that has been implemented in a real world environment. The system design has provided for real time control, and data gathering and telemetering, and has been successfully implemented in a user setting.


Function Decoder
Unit Code Comparator
Check Circuit
State's and Control Reg.
Receiver and Transmitter


FFFFH
External
Program
Memory
0FFFH
0000H
FFH
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80H
Special Function Register
FFH
80H
7FH
RAM Memory
30H
2FH
Bit RAM
20H
1FH
General Register
00H
External
Data
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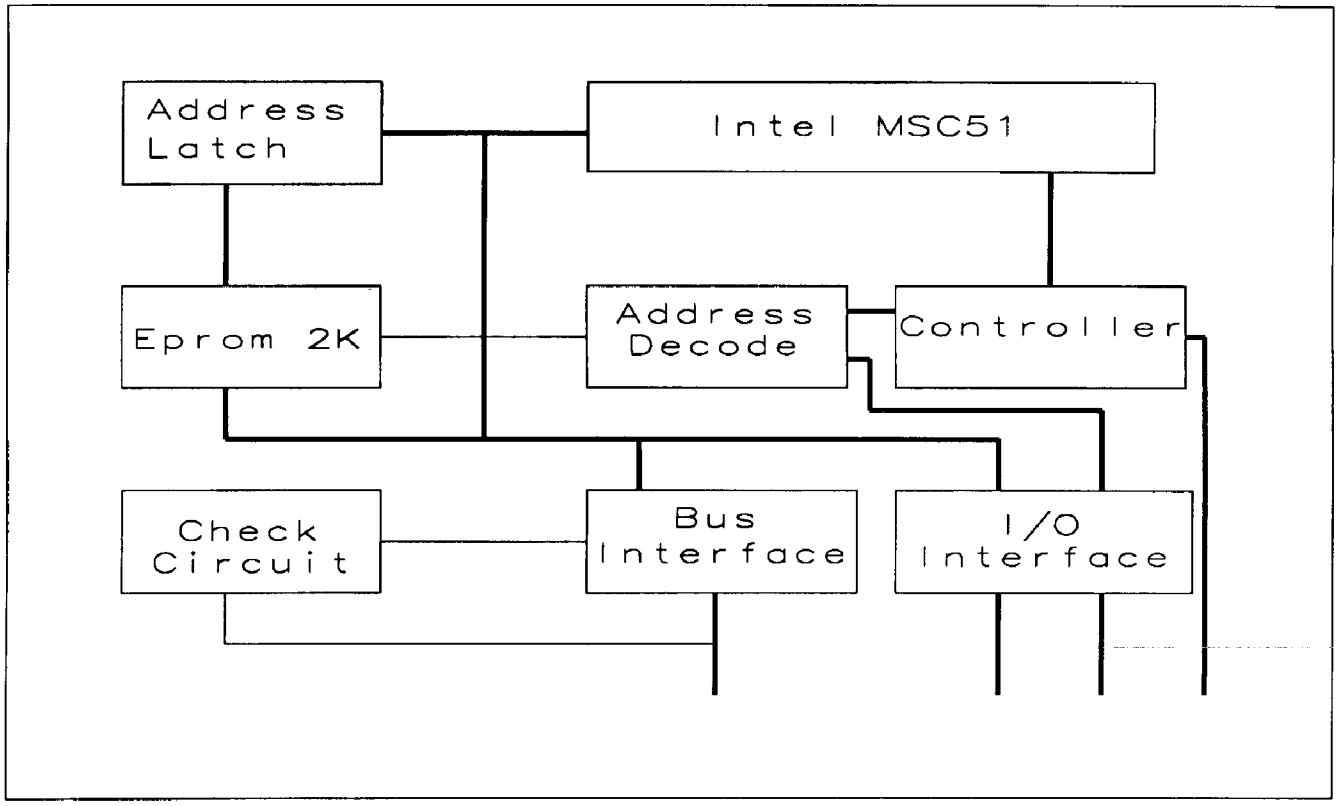
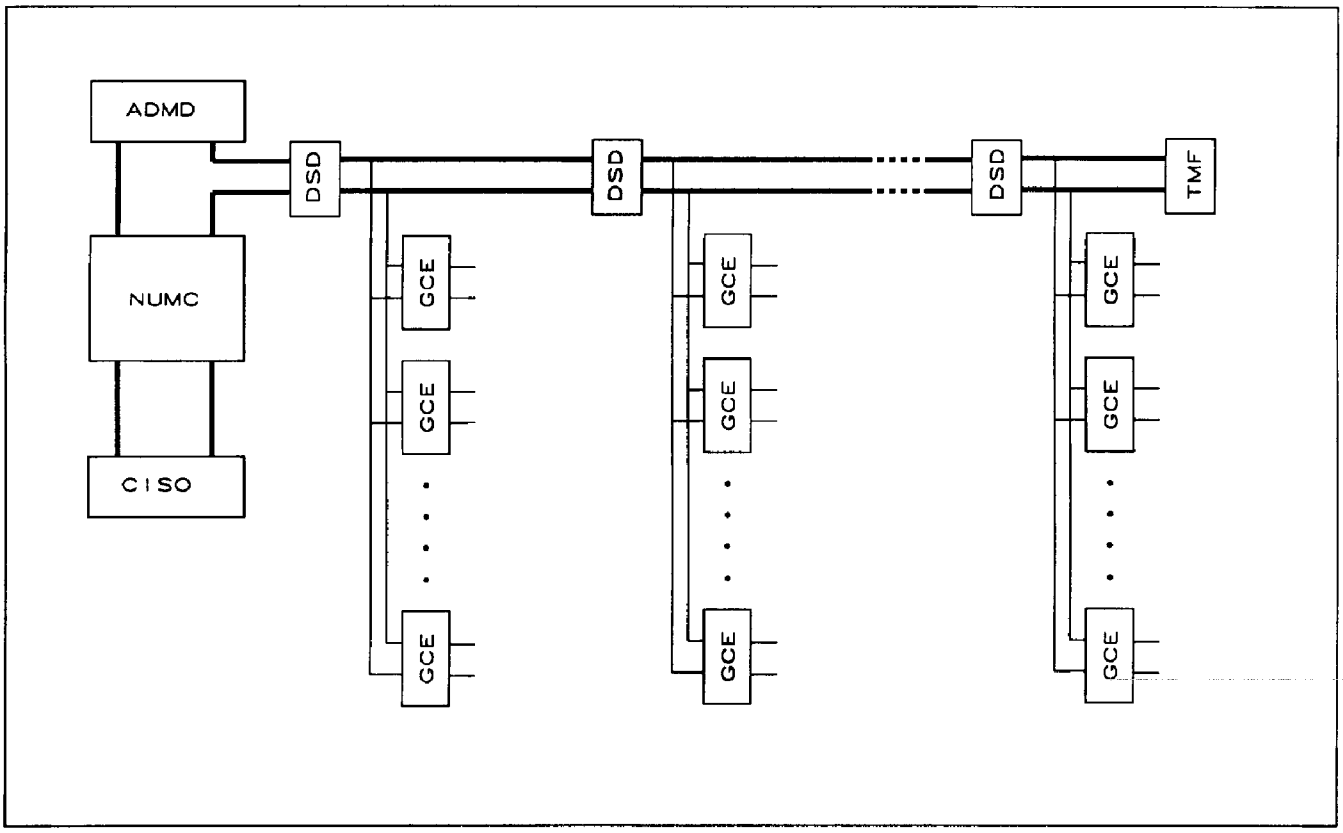

Address Latch
Intel MSC51
Eprom 2K
Address Decode
Controller
Check Circuit
Bus Interface
I/O Interface


ADMD
NUMC
CISO
DSD
DSD
DSD
TMF
GCE
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