DESIGN OF A FOUR-CHANNEL, 50 MBPS, STATISTICAL MULTIPLEXER AND DEMULTIPLEXER

John T. O'Donnell
Engineering Manager
Digital Communications
AYDIN MONITOR Systems
502 Office Center Drive
Fort Washington, PA., 19034

ABSTRACT

This paper discusses the design of a 50 Mbps Statistical Multiplexer and Demultiplexer, Model 781, manufactured by AYDIN MONITOR Systems of Fort Washington, PA. Two Model 781s connected through a 50 Mbps communications link constitute a full-duplex, 4-channel data link with a maximum aggregate throughput capability of 48 Mbps.

INTRODUCTION

The Model 781, shown in Figure 1 and in block diagram form in Figure 2, was designed under contract to NASA Goddard Space Flight Center (GSFC) for use in the ground network of the Tracking and Data Relay Satellite System (TDRSS). Ten of these units are in place to support Spacelab and Landsat-D data flow between White Sands, Johnson Space Center (JSC), and GSFC. Figures 3 and 4 show how the Stat Mux fits into the TDRSS data communications network. Data streams from the Spacelab and Landsat-D Satellite are relayed by TDRS to an earth station at White Sands, New Mexico. These data streams are merged by the Model 781 and transmitted in a 50 Mbps signal via Aydin's Model 2708 Modem and the RCA DOMSAT to receiving sites at JSC and GSFC. Companion units at these sites demultiplex the data and provide 4 serial streams to the ground data processing equipment.

In this paper we will look at the capabilities of the Model 781, note the customer's specification requirements, and examine the resulting implementation.

DEVICE DESCRIPTION

The Model 781 is a single chassis, EIA Standard rack-mountable unit that provides multiplexing and demultiplexing of up to 4 lines of serial synchronous data, each at any bit

rate from 100 Kbps to 48 Mbps. A multiplexer/demultiplexer pair (hereafter referred to as mux/demux) connected through a communications channel constitutes a transparent 4-channel data link. (The output channel data is continuous and at the same rate as the input.) The mux makes optimum use of the 50 Mbps communication link by using statistical multiplexing techniques, partitioning the input data stream, formatting the data in equal size blocks or frames with channel addresses and frequency information, and transmitting the data from each channel a frame at a time based on rate-determined priorities. The ratio of overhead information to frame size is less better than 4 %, making available better than 96% of the communication link bit transmission. The demux recognizes frames by detecting distributed synchronization patterns in the received data frame's destination by looking at distributed channel address information. It routes the frame to the appropriate output channel where an expansion buffer smoothes the 50 Mbps burst rate input to the nominal channel rate output.

The unit incorporates a microprocessor (uP) in the unit-operator interface for the mux and demux. In addition to processing operator control inputs the uP dynamically assigns input channel priorites based on channel data rates, monitors output channel expansion buffer fill to detect impending overflow or underflow, and adjusts channel output rates to correct any such tendency, thus preventing loss of data.

SUMMARY OF NASA'S FUNCTIONAL SPECIFICATION

NASA's procurement specification describes the functional requirements for the design, fabrication, and testing of a Statistical Multiplexer to be used on a 50 Mbps domestic satellite communication channel. In this section we'll highlight some of the salient technical requirements.

Specific Requirements

Transmit Section - The transmit section shall accept data on 4 ports simultaneously at any rate from 125 Kbps to 48 Mbps plus or minus 5 parts in 10^4 and transmit the data in frames with sync, frequency, and port address at a nominal 50 Mbps, determined by the clock from the transmitting modem or NASA's site standard. (The 5 parts in 10^4 variation in input speed is due to Doppler between the Shuttle and TDRS satellite.) No manual operation or control signals shall be required in the transmit section to change the input data rate. The clock speed shall be continuously measured at each port input and transmitted to the distant receive section in each frame. In addition, the frequency information is to be displayed on the front panel to six significant digits plus exponent.

The transmit section shall provide storage for the data frames being formatted from each of the four input ports and shall transmit them in whatever sequence meets the requirements

of an uninterrupted contiguous bit stream at the receiving port output. In addition, the frame sync information, port address, and frequency must be protected against errors clustered in bursts of 100 or more contiguous bits to prevent lost or misdirected frames or sudden changes in output frequency.

The transmit section shall provide a 50 MHz master clock with an accuracy of 1 part in 10^7 or better which can be phase-locked to an external site standard. This master clock will provide the transmit clock to the modem. In the absence of the site standard this clock will free-run and will automatically resume phase lock to the site standard when the external clock returns.

Receive Section - The receive section must accept frames at a nominal 50 Mbps, identify the sync pattern and port address, route the frame data to the appropriate output port, set the port output clock rate based on the received frequency information, and output an uninterrupted bit stream at the same bit rate as is being applied to that port at the transmit end.

The output ports must each provide an expansion buffer to smoothe the 50 Mbps burst input rate to the port's nominal output rate. Data presented at the receive port output shall be stripped of the synchronization, port address, and frequency information, and shall be accompanied by a coherent bit rate clock developed by frequency synthesizer circuits in each output port. The synthesizers shall be capable of generating any clock rate from 124.937 Kbps to 48-024 Mbps and must follow the continuous Doppler variation in the input clock at the transmitting location.

Test Features - The unit shall provide port and transmission system test functions and must be able to detect lost frames. The port test functions shall utilize a 2047-bit PN pattern that can be transmitted at 12 Mbps through any or all ports. The receive section output ports shall provide PN pattern checkers to detect bit errors. In conjunction with this test mode the unit shall have a local loopback capability such that the transmit section output can be internally connected to the receive section input. Receive bit errors in this test mode or when two units are connected locally as in an end-to-end configuration shall not exceed 1 in 10^{12} over a 24 hour period.

This concludes the summary of the customer's functional specification. In the next section we will look at the approaches taken to satisfy these requirements.

IMPLEMENTATION

This section deals with the realization of the customer's functional specification. It examines the architecture of the unit and describes the techniques employed to meet the specification's major technical requirements.

Unit Architecture

Figure 2 presents a simplified block diagram of the Model 781. As shown in the figure the unit comprises four major sections. At this point we want to look at the role played by each section and the relationship of one to another. Then we want to identify the functions performed by each of the modules within the sections.

The transmit and receive sections are in the data path while the clock generation and control blocks are auxiliary to the data path. Figure 5 highlights the transmit section emphasizing the multiplexing function performed there. Similarly, Figure 6 emphasizes the demultiplexing function of the receive section. These two areas are independent of one another but do share the common clock generation and control facilities.

The clock generation function provides time reference signals for frequency measurement and frequency synthesis in the transmit and receive sections respectively. It also provides a timing reference for the control section and generates the 50 MHz transmit clock signal.

The control section processes local and remote control inputs and provides status and frequency data for front panel and remote display. It reads frequency information at regular intervals from the transmit and receive section to establish transmit port priorities and generate the front panel frequency displays. It also monitors the average fill status of the receive port output buffers and applies output frequency corrections to maintain the optimum average fill.

Module Functions, Transmit Section - The transmit or multiplexer function employs three module types. There is a Data and Clock Receiver, HSR001, that provides high speed balanced receiver circuits matched to the user's external data and clock drivers. The receiver circuits provide differential-mode data and clock signals to the Transmit Multiplexer Input Modules (XMX001). There is one XMX module per channel, or port. These modules provide 1K x 31 compression buffers for the input data. The compression buffers convert the bit serial input to 31-bit wide words which in turn are organized into 248-word frames. The XMX modules signal the Transmit Module (XRV001) whenever they have a frame or more of data in their buffers. The XMX modules also continuously measure bit rate of the incoming data using a 100 Hz time base signal supplied by the CGN001 module in the clock generation section. The resulting measurement is stored in a

register monitored by the control section and is passed to the XMX at the end of each frame of data. Since measurements occur at a 100 Hz rate there is no problem accommodating the expected Doppler rate variation, since the transmitted frequency information is used to program the frequency synthesizers in the receive output ports.

The “frame ready” signals asserted by the XMX modules alert the Transmit module (XRV) that there is data to send. The basic function of the XRV is to transmit data frames from the input modules in such a way that each channel is able to maintain an uninterrupted output stream at its distant receive port. The XRV accomplishes this by responding to the XMX modules on a rate-determined priority basis such that the highest rate port has the highest priority with remaining priorities assigned to ports in descending order of bit rate. Priority calculations are made by the processor in the control section based on the frequency data from the XMX modules. The priority code is downloaded to the XRV module and is updated dynamically as input data rates change. This adaptive assignment of priorities and the fact that the XRV reevaluates priorities after each frame transmitted, insures that the highest rate port will be delayed no longer than one frame time from accessing the communications link. This prevents a high rate channel from underflowing its output buffer.

The XRV also formats the input data words into a frame structure that includes the overhead information required by the receive section to recognize and correctly route the received frames. This frame structure is shown in Figure 7 which details a format of 250 words by 32 bits per word. The 248 thirty-one bit words that constitute a frame in a channel’s input buffer are expanded to 32-bit words by appending a sync bit to each. These are transmitted, data bits first, in the first 248 words of the multiplexer frame. This portion of the output frame is further divided into 8 groups of 31 words as shown. The trailing sync bit in each of the 31 words in the first 7 groups is provided from a 31-bit Maximum Length Shift Register Sequence (MLSR). Thus, that bit position is used to transmit 7 repetitions of the 31-bit pseudo-noise sequence generated by the MLSR. This PN data serves a dual purpose. It is used in the receive section to establish word boundary synchronization so that the receiver need look for the distributed end-of-frame pattern only at word intervals, thereby reducing the probability of false correlation when there is a wide error tolerance. It also provides redundant, distributed transmission of the port address information since a different PN sequence or complement sequence is used for each port.

The sync information distributed in the last group of 31 words provides an end-of-frame indication. Distributing the pattern protects it against burst errors in the same way the port address information is protected.

The last 2 words of the frame are used for redundant transmission of the port frequency, and for passing the frame sequence counter. The frequency data comes from the input

module. It is read twice by the XRV after it has unloaded 248 words from the XMX buffer.

The XRV transmits the formatted frame at 50 Mbps to the communications link modem and a backup recorder.

Module Functions, Receive Section - The modules of the receive section demultiplex the data received from the 50 Mbps communications link. As shown in Figure 6 recognition and demultiplexing of received frames involves first the receiver portion of the XRV module, then the Parallel Pattern Detector (PPD) and Demultiplexer Output (DMX) modules, with the Frequency Synthesizer modules (SYN) generating the required output bit clocks.

The function of the XRV module in the receive context is to synchronize to the 32-bit words in the incoming frame so that the port address and end-of-frame pattern can be detected. The XRV acquires word synchronization by determining which bit position in the 32-bit word transmits the 31-bit PN sequence. However, the XRV does not search for the PN sequence itself but rather within the word the bit position whose data content is cyclic repeating every 31 words. The use of the PN data affords protection against the possibility of the user's data stream containing invariant bit positions recurring every 31 bits.

The algorithm used is adapted from a proposal by Van de Houten (2) for an adaptive synchronizer based upon the Sequential Probability Ratio Test (SPRT) described by Wald (3). In this case the SPRT is applied to each bit position of a 32-bit register through which the received frame is passed a word at a time. At each bit position the current bit value is compared to the bit value 31 words earlier (a continually updating memory provides a 31 word history) and if there is a match, an accumulated confidence level maintained for the bit position is incremented by 0 and if a mismatch decremented by 3. (The increment value for a bit match is normally zero for total immunity to invariant bit positions but can be internally set for .5 for faster word sync acquisition. The decrement value is established by the expected worst case bit error rate, in this case set for 10% for ease of implementation.) If there is a bit match plus a transition from the bit value one word time earlier, the bit position's confidence level accumulation is incremented by 1.25. Thus the bit slot transmitting the PN sequence is favored over one with invariant data due to the transitions in the PN data. Word boundary synchronization is achieved when one of the 32 confidence level accumulations reaches a limit called the Decision Error Confidence Level (DEC level). The DEC level is internally selectable over a range corresponding to a probability of decision error (DEP) of 10^{-4} to less than 10^{-6}. Figure 8 shows sync acquisition time versus DEC level for the SPRT word boundary detector. The three DEC levels shown, DEC = 16, 20, 24 correspond to DEP = 10^{-4}, 10^{-5}, 10^{-6}, respectively in the usual

implementation of SPRT (2) where the weight of a favorable outcome from the bit comparison is 1. However, in this particular application the weight of a favorable outcome is less than 1 for both cases shown so the DEP is even less. The DEC level is one-half the difference between the Go-to-Lock and Go-to-Search decision levels.

The result of word boundary synchronization is a word rate clock pulse occurring at the sync bit time. The XRV passes the serial data and synchronized word rate clock to the PPD which uses the word clock to examine the information in the sync bit position. The PPD uses four PN data checkers as port address decoders to determine which of two 31-bit MLSR sequences or their complements has been used as the word boundary synchronization pattern in the frame being received. The PN pattern checkers are allowed to "look" only after the XRV has acquired word sync. For the most stringent word synchronization criteria it takes 108 PN sequence bits or 108 words of the frame to acquire word sync in an error-free environment. This number is the sum of the number of word times required for synchronization, 77 as shown in Figure 8, plus the initial 31 words of history. (Acquisition time is extended by 6 word times for each error encountered). Thus, under these conditions there remains one-half of the PN data for the port address detectors to look at. A detector decides that it is receiving its assigned sequence if it encounters no more than 2 errors in a sequence length. If it encounters more than 2 errors it reinitializes and continues looking, and if less than or equal to 2 errors it raises a flag indicating that its associated port is the target for this frame's data.

The PPD also uses the synchronized word clock to shift sync bits through a 31-bit pattern correlator used to detect the end-of-frame pattern. The correlator can tolerate from 0 to 4 errors, internally switch-selectable. End-of-frame pattern detection sets the stage for routing the received frame to the intended output port. A frame timing generator is activated which produces word transfer pulses and time slot markers for the frequency data and frame sequence counter. The frame sequence counter is stripped out and compared to a local frame counter on the PPD card. The local counter is initialized to a received frame sequence number in a search mode (e.g. after a receive system reset) and thereafter incremented with each received frame. Therefore if a frame is lost, due to too many errors in the end-of-frame pattern for example, there will be a mis-compare on the next frame and thus a lost frame detected.

The received frame, which is shifted through an 8000-bit pseudo shift register, is partitioned into 32-bit parallel words and directed to the addressed DMX module which strips away the overhead information and provides the serial output.

There are four each DMX and SYN modules which are paired to perform the rate conversion from 50 Mbps burst mode input to the ports' commanded output rates. The DMX provides a 1K x 31 expansion buffer and parallel-to-serial converter to convert the

bit-parallel, word serial output of the PPD to an uninterrupted, bit-serial data stream at a rate controlled by the SYN clock. It strips and processes the frequency information in the recovered frame to program the SYN module and applies frequency corrections and updates the synthesizer's prescaler and decade dividers on command from the control section. It also allows the control section to read the received frequency and monitor expansion buffer fill. This module also provides a test data check circuit which monitors the 2047-bit repeating PN pattern when the channel is in the test mode.

On data startup the DMX requires two frames in its buffer before it will allow output of serial data. This provides an adequate reserve of data so that an output port will not underflow when its companion transmit port has to wait for access to the communications link. This initial level of buffer fill is used as a decision point by the control section processor in deciding whether or not a correction is needed for the output frequency. The processor reads buffer fill from a register that is updated at the end of each frame stored. If the number read is higher than the startup level a positive frequency correction of 100 Hz is applied to the output rate. If on two consecutive reads the numbers are lower and the second is less than the first a negative 100 Hz correction is applied. This capability allows the processor to compensate for time base difference in the transmit and receive sections and to bring the average buffer fill back to optimum after an abrupt change in transmit frequency. When the processor sees that the buffer fill is back to its desired level it sets the correction to zero.

The SYN output clock rate is controlled by the frequency information in the received frame and therefore varies in the same way as the input clock at the transmit end. Thus, the receive port output reproduces the Doppler effect experienced at the input. The system provides protecton against erroneous rate information being supplied to the SYN by requiring that the two received frequency words be identical and the guard bits match their pre-assigned value. Only then will the frequency program for the SYN be updated.

The SYN frequency synthesizer module employs a single-loop, subranging design to provide the required operational frequency range of 125 kHz to 48 MHz. Its voltage-controlled oscillator (VCO) operates over the range of 50-100 MHz. The VCO output is divided down to 100 Hz (since the reference is 100 Hz) by a pre-scaler, decade divider, and divide-by-N circuit where N is the received frequency measurement. The pre-scaler and decade divider ratios are decoded from the frequency measurement N by the DMX module but are updated only on command from the control section processor. The reason for this is that a change in either one causes a sudden change in output frequency since the VCO has to switch to a different subrange but cannot do it in zero time. Therefore if a port's nominal bit rate was at a frequency where a range shift occurs the expected Doppler variation of + or - 5 parts in 10^4 would carry the output rate across that range shift point, with unhappy consequences if the range was allowed to switch. To prevent this the

processor maintains a reference frequency for each output port. The DMX flags the first valid frequency received after a reset or pre-scaler ratio update. The processor saves that value and compares it with all subsequent frequency readings from that port. If the difference is greater than .1% a pre-scale/decade divider ratio update command is given. Thus in the case where the port nominal is at a range shift point the Doppler will move the frequency command to the SYN back and forth across that point without causing the VCO to range-shift. However, if there is a change to a new nominal the ratios will be updated since there will be a difference of greater than .1% between the old and new values.

This completes the description of the receive section.

Module Functions, Clock Generation Section - As mentioned previously the clock generation section provides timing reference for the transmit, receive, and control sections. This section is implemented by the CGN001 Clock Generator module and a 5 MHz, oven-controlled crystal oscillator. The CGN accepts an external primary reference to phase-lock the secondary internal master oscillator. This oscillator in turn provides the reference to phase-lock a 50 MHz oscillator on the CGN. The 50 MHz signal is provided to the transmit section to generate the 50 Mbps serial data and is divided down to provide reference signals for the frequency measurement and synthesis circuits. The CGN has a clock dropout detector which keeps the phase-lock loop closed as long as the external reference is present but allows the secondary master oscillator to free-run if the external reference is lost. In the free-running mode the oscillator output is accurate to better than 1 part in 10^7 with stability approaching 1 in part 10^8.

Module Functions, Control Section - The control section includes the Control and Interface Module, CIM003, the Decimal Display Board, HDB003, and front panel keypad and indicators. The heart of the control section is the CIM module. Most of its major functions have already been described. These include automatic transmit port priority calculation, receive port frequency correction, and, for the frequency synthesizer, prescaler/decade divider ratio update control. The CIM, through the front panel keypad provides full control of all port operating modes and test features. Concerning the latter it allows the operator to select local loopback mode, but any or all ports in test, and insert port errors and frame errors. It continually displays the frequency of signals connected to the transmit ports whether or not those ports are turned on. It displays transmit and receive port frequencies to 6 significant digits. (We note here that although the frequency measurement gate is only .01 second the CIM obtains effective 6-significant digit display accuracy by integrating 100 consecutive measurements.) On power-up the CIM executes an automatic diagnostic and operability test sequence. Finally the CIM provides protecton against inadvertent or accidental operation of critical keys by requiring a 2 second key depression for those functions.

The HDB module provides transmit and receive port frequency display and an indication of frequency synthesizer lock status.

This concludes the functional description of the design of the Model 781. However, there are specification requirements whose resolution could not be conveniently addressed in the above description. These are addressed below.

Protection Against Large Error Burst in Domsat Link - Dut to forward error correction coding on the Domsat channel, residual errors are expected to occur in bursts. The intent of the specification is to maximize throughput to the correct port even if the data contains a significant number of errors during a burst. The Model 781 accomplishes this by distributing the port address through the frame and by distributing the end-of-frame pattern (EOF). This technique provides immunity to error bursts over 100 bits in length. For example, if the error tolerance for EOF pattern detection is to 4, error bursts up to 128 bits can be tolerated without effecting frame throughput.

Low Internal Error Rate - Very conservative design rules were followed to ensure the unit could meet the internal error rate requirement of 1 in 10^{12} over a 24-hour period. In particular we elected to use an all-ECL implementation of the data path as opposed to combining ECL, and for example, power Schottky (LS TTL) . The reason for this is that the edge speed of LS TTL is 3 to 4 times greater than that of ECL (10K family). These speeds would pose a noise hazard to the ECL circuits which operate lower noise margins than the TTL circuits. This possibility would have been even more pronounced in this design since the LS TTL would have been used only in broadside functions where many lines change at once.

In addition to an all-ECL implementation for the data path the design incorporates the following precautions to minimize or eliminate interference between circuits.

- The IC panels are specifically designed for ECL circuitry and high speed wiring.
- Use of an automatic wiring system that provides optimized wire routing.
- Use of balanced signal transmission in the backplane to eliminate effects of ground shift and supply voltage variation between modules.
- Physical and electrical isolation of critical analog circuits from digital circuits.
- Special routing and termination of high-speed clock circuits.

CONCLUSIONS

The major technical specifications and the resulting design for a 50 Mbps Statistical Multiplexer and Demultiplexer have been presented. Additionally, the paper details techniques that provide the following highly desirable or necessary characteristics for a mux/demux used in a space data communications link.

1. Automatic frequency measurement and adaptive port priority assignment to allow unattended operation.

2. The ability to accommodate Doppler variation of port input rates while maintaining an uninterrupted serial output at the receive port.

3. Immunity of frame detection and routing to large error bursts.

4. Low internal error rate.

Finally, the discussion points out the critical role played by the microprocessor in the subject application.

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R. McGarvey, B. Faust, J. Kennon, - Project Personnel

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2. Van de Houten, R.S., “Adaptive Pattern Synchronization”, Proceedings of the ITC, 1967, Oct. 1967.
3. Wald, A., “Sequential Analysis”, John Wiley and Sons, INC, New York, 1947.

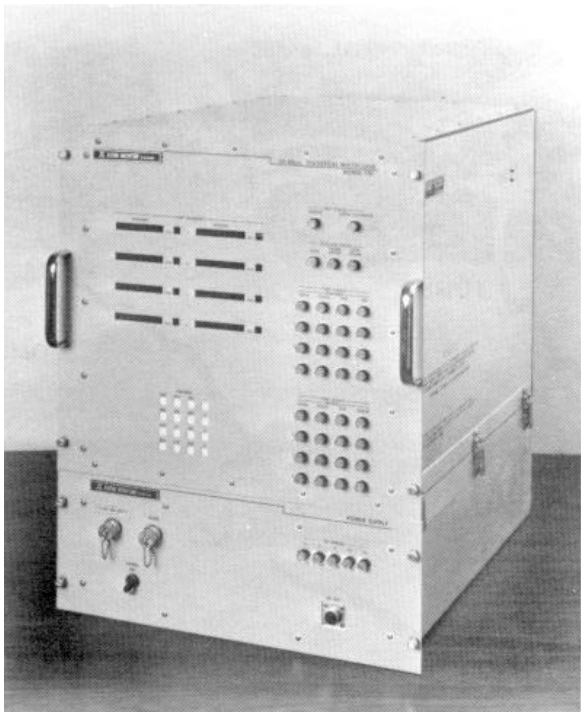

Figure 1 - AYDIN MONITOR Systems' Model 781

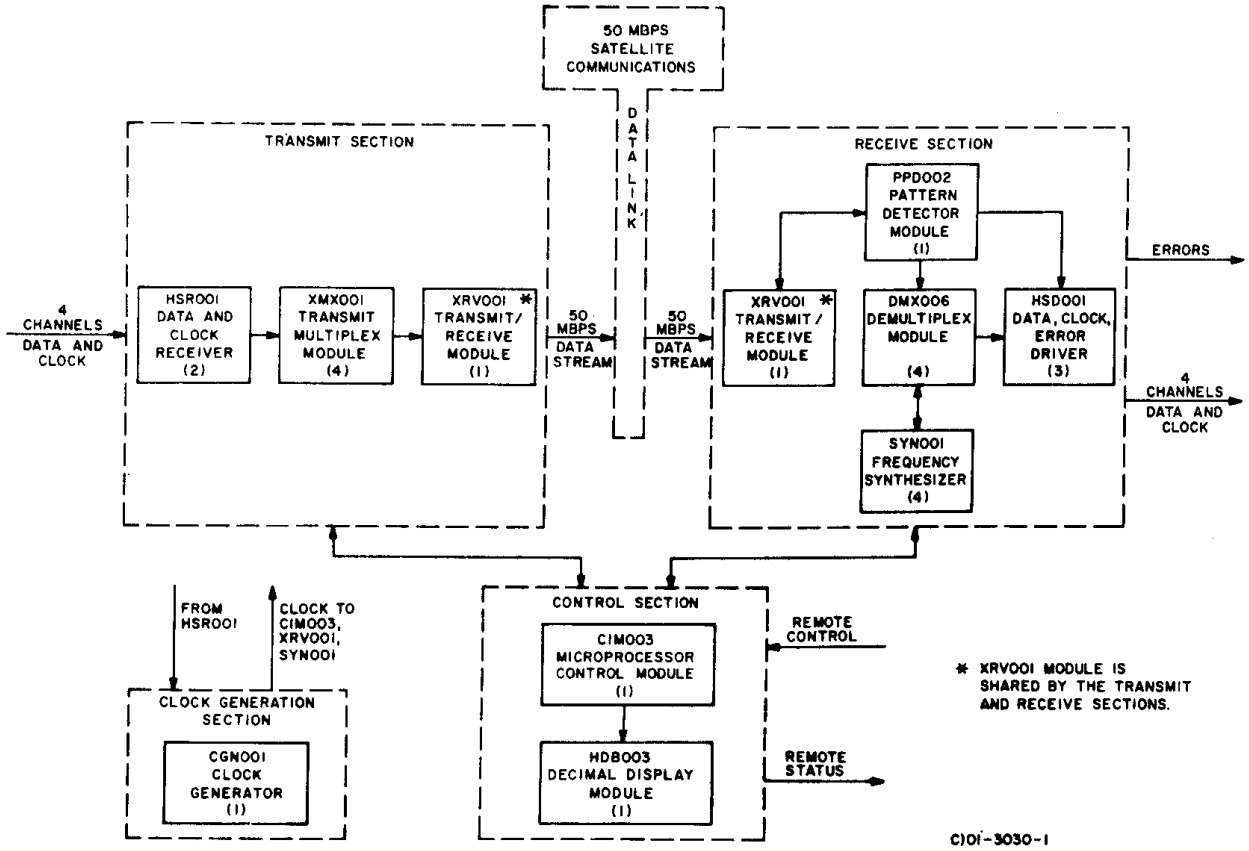

Figure 2 - Model 781 Simplified Block Diagram

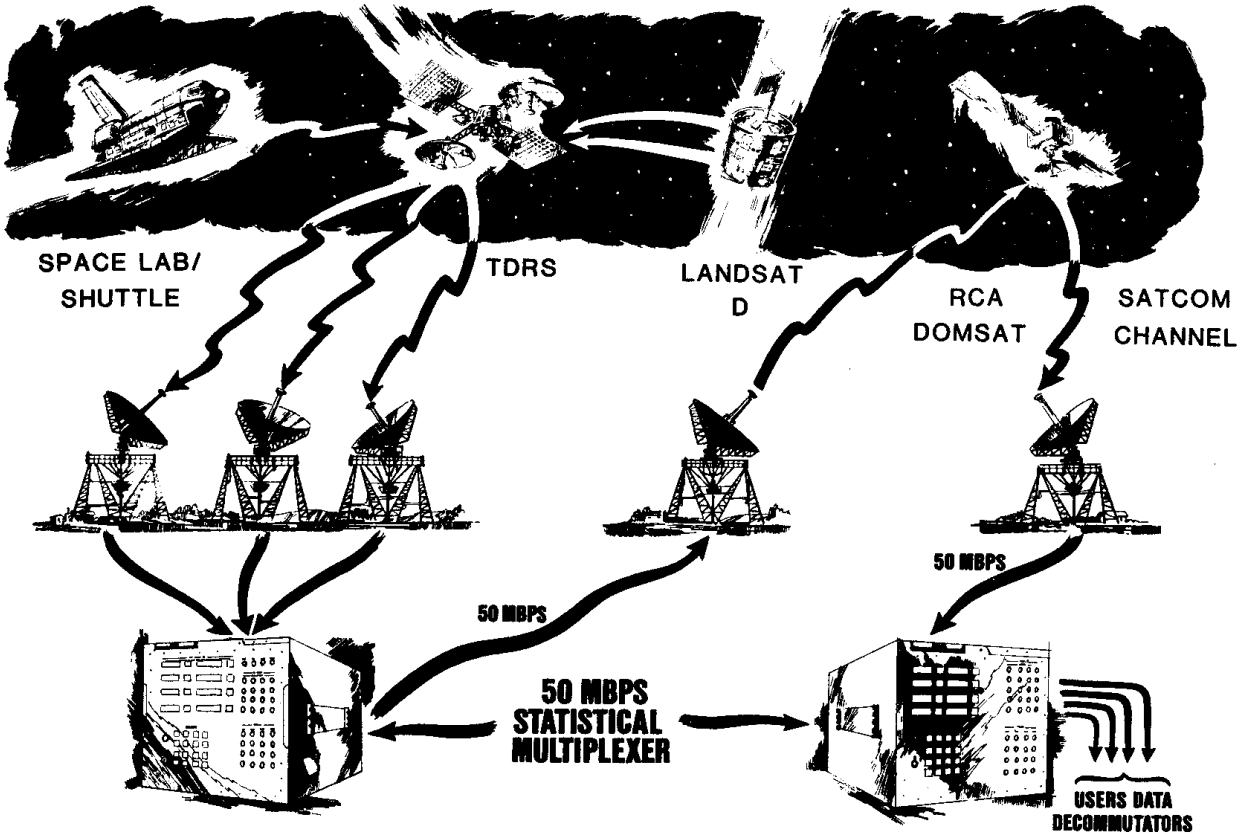

Figure 3 - Spacelab/Landsat Data Flow

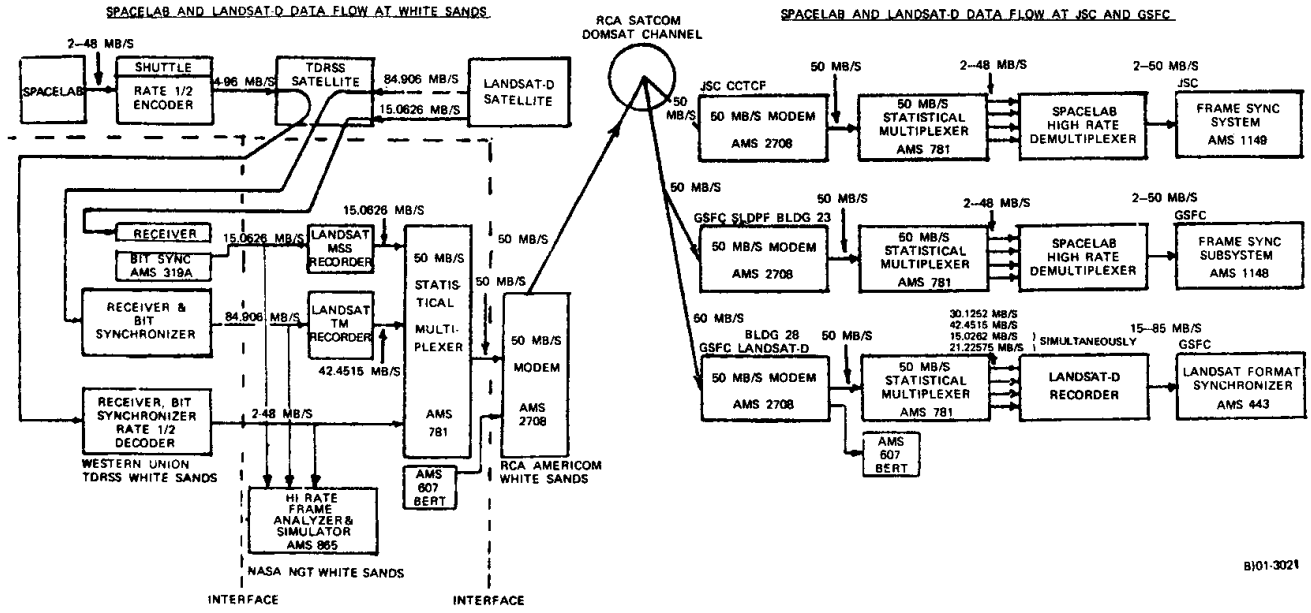

Figure 4 - Spacelab/Landsat Data Communications Network

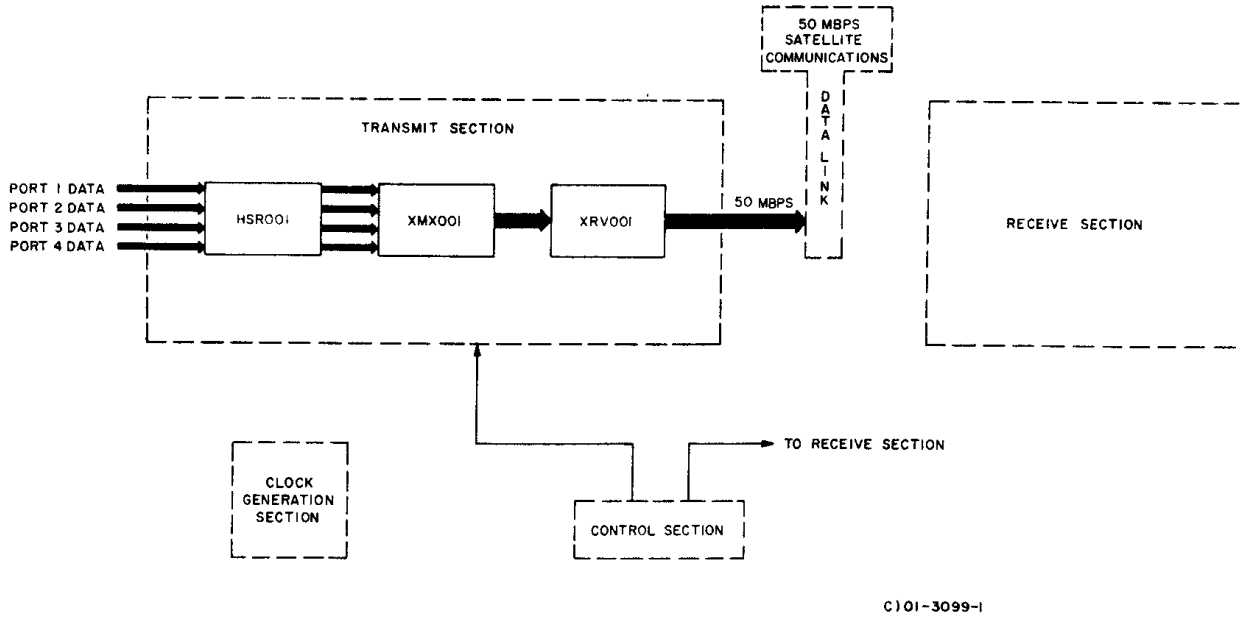

Figure 5 - Transmit Section Data Flow

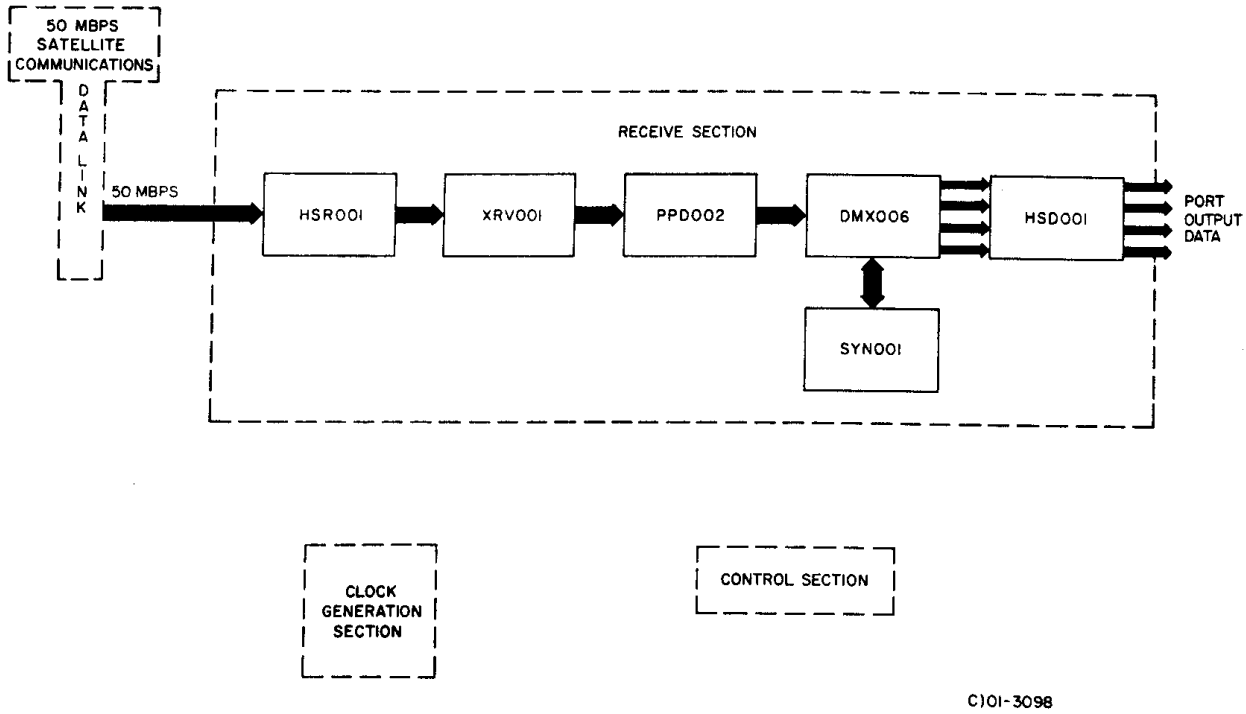

Figure 6 - Receive Section Data Flow

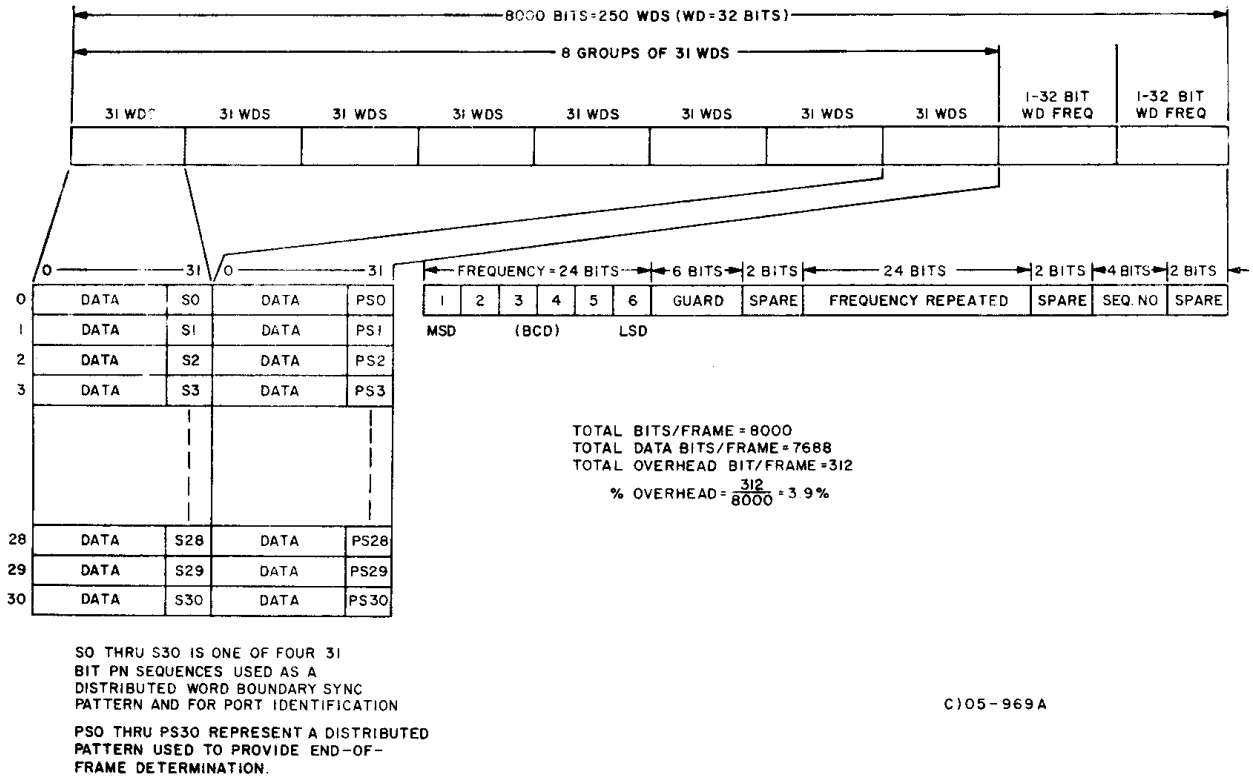

Figure 7 - Multiplexer Frame Structure

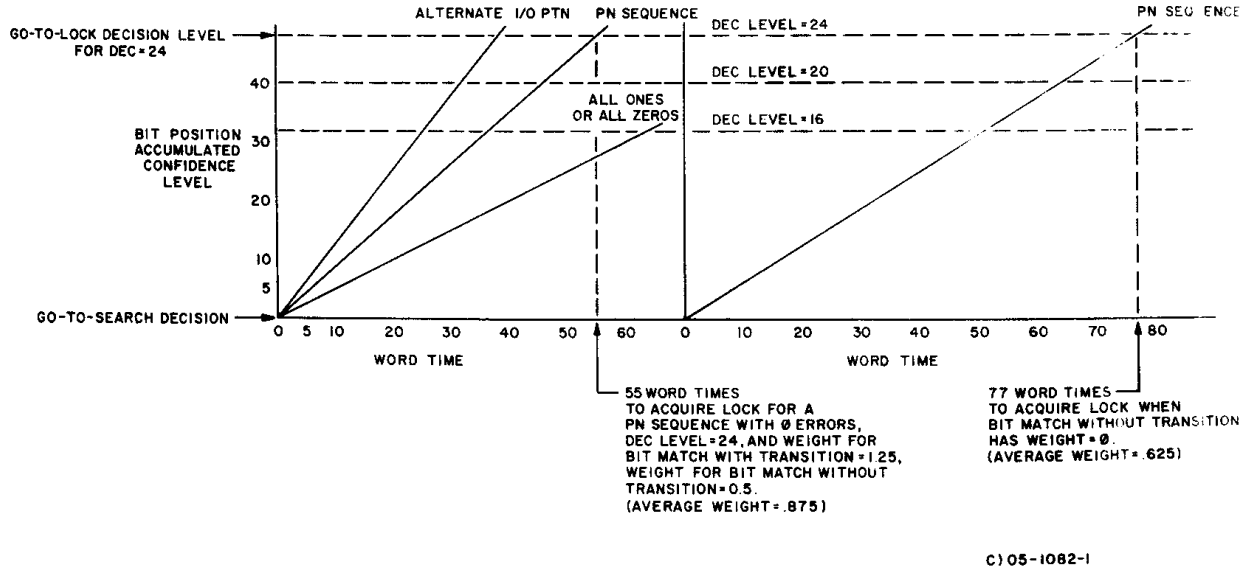

Figure 8 - SPRT Correlator Decision Time Versus Error Confidence Level