MIL-STD-1553 DATA BUS/PCM MULTIPLEXER SYSTEM

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ABSTRACT

A telemetry system which integrates MIL-STD-1553 bus data, dual-simplex bus data, vehicle performance data, and environmental sensor data multiplexing involves many interfacing constraints. The engineering design considerations and hardware constraints required to implement this system are presented in this paper.

INTRODUCTION

This system interfaces with a 1553 data bus in a bus monitor capacity and with an operational payload data bus. At the same time, it multiplexes performance and environmental data from a test vehicle operating in a flight regime. (Figure 1 is a block diagram of the system.)

The 1553 bus interface design requires that the system perform as a monitor and as a dummy remote terminal which does not respond with a status message. The processing design incorporates these constraints by modifying protocol tracking and message gap requirements. The system integrates the bus and sampled data into a secure 2.0 MBPS serial data stream conditioned for transmission.

The elements of the system are 1) 1553 Bus Data Processor, 2) Dual-Simplex Operational Payload Simulator, 3) Analog/Digital Signal Multiplexer, 4) Analog/Digital Signal Conditioner, 5) Format and Timing Unit, and 6) A Secure Data Support Unit. The entire system is packaged in a volume of less than 700 cubic inches.

1553 BUS DATA PROCESSING SECTION

The bus data processing section consists of a bus monitor, microprocessor, and buffer as shown in Figure 2. It monitors all 1553 bus data and converts the 20-bit words to a 24-bit word as defined in Chapter 8 of IRIG 106-88. The formatting differs, however, because of supercommutation requirements. The 24-bit words,

are made up of the 16-bit data words pre-pended with an 8-bit ID word, including a parity bit as shown in Table 1. These converted 24-bit words are inserted into the telemetry format at a 41 KWPS rate. This is adequate for a 1553 bus operating at a maximum rate of 46 KWPS (92% efficiency). The processing section can buffer a maximum word rate for 30 milliseconds without overflow. The data latency is a variable ranging from 76 microseconds to 4.9 milliseconds. (This is the time from the entry of a 1553 word into the processing section until it is output to a transmitter.) The actual time is dependent upon the timing between the buffer and the PCM format position.

Certain 1553 16-bit data words, a maximum of 32, are selected by the Quick Look (QL) module. The data words are transferred to the QL port which interfaces with the format and timing sections. The incoming data rate can be as high as 350 WPS. The data will be processed by the QL buffer and inserted into the format at 31.25 WPS, the subcom rate. If there is no change in the data between minor frames, the last data word is inserted. Thus, data of single-occurrence events will be transmitted continuously. Data latency for these words is much greater because of the longer time that the data must be buffered until it is inserted into the frame format. Data latency varies from 73 microseconds to 32.7 milliseconds.

As can be seen in Table 1, there are filler words (16 bits of an alternating 1/0 pattern) and error ID’s. The filler words aid in keeping an adequate number of bit transitions for maintaining synchronization of a data processing decommutator. This is necessary when the bus is down or if bus protocol is being continuously distorted. The error word ID is attached to the data word, without passing judgement on the validity of the data, only when an error is detected. Errors may include the occurrence of improper parity, invalid sync, incorrect sync, Manchester error, or incorrect bit count. The data word as received is combined with the error ID to form a 24-bit word that can be used during post-test bus diagnostics at a data processing facility.

ANALOG MULTIPLEXER

Test vehicle performance and environmental data is monitored by 77 analog/discrete inputs. These are specifically tailored to the input characteristics and spectral content of the data. Inputs consist of single-ended and differential data extracted from transducers such as strain gages, thermocouples, resistance temperature devices, vibration sensors, and acoustic sensors. Constant current and highly-stable, low-drift voltage sources provide excitation for the various

transducers. In addition, various system voltages are measured as single ended or discrete inputs and switch closures are output as digital words. A typical analog input path is depicted in Figure 3A.

Input conditioning circuits are utilized to normalize the various types of inputs. This ensures that only unipolar or symmetrical bipolar inputs of less than 2.5 Volts peak-to-peak are present at the input of the instrumentation amplifier. This voltage level allows the programmable gain amplifier (PGA) to be preset to a nominal gain of 2 in case signal attenuation is required. It also satisfies input requirements for the 0-5 Volt sample/hold amplifier and A/D converter.

The front-end instrumentation amplifier is used to provide accurate, stable gain for low-level inputs of either single-ended or differential types. It also drives the pre-sample anti-aliasing filters. Each input channel has separate gain and filter circuits. The anti-aliasing filters are Butterworth types with 1, 2 or 4 poles, depending upon the spectral content and input level of each signal. The 2- and 4-pole filter roll-offs (3 dB) are set for one-fifth the sample rate.

After pre-sample filtering is complete, the seven channels on each signal conditioning card are multiplexed into a single PGA. The PGA gain is controlled by an externally-programmable device (EPROM) and has a dynamic range of 1 to 32 steps with a nominal gain of 2 preset. This allows for a maximum programmable amplification of 16 or attenuation of 0.5.

One of the most crucial elements of the entire analog design process was to satisfy system bit rate and accuracy requirements for 77 channels while maintaining design simplicity. With a system bit rate of 2 MBPS, only 4.0 microseconds per 8-bit word was available for the A/D conversion process. The precision A/D converter used for this application requires a minimum of 1.2 microsecond hold time when short cycled from 12 bits to 8 bits. Therefore, 3 bits (1.5 microseconds) was allocated for the hold time. This left 2.5 microseconds (5 bits) for settling and sample time. Settling time requirements were satisfied by multiplexing the analog signal as shown in Figure 4. This design-simplifying feature constrains the format so that each of the 11 analog signal conditioning boards can only be addressed every fourth word.

The analog multiplexing design resulted in complete settling at the output of the PGA prior to being switched onto the analog bus shared by the signal conditioning boards. The bus capacitance was large due to the additive effect of 1) board enable switches on each signal conditioning card, and 2) the analog bus capacitance. This dictated the following design considerations:

A) Use of a current driver for each signal conditioner output

B) Short the capacitance-developed bus potentials to ground during the A/D hold times

These two design considerations insure that there is adequate drive capability and that each analog measurement is subjected to equivalent initial conditions resulting in minimal signal crosstalk.

Finally, to satisfy the gain programming requirements for both unipolar and bipolar inputs to the unipolar A/D converter, a two-value programmable offset is applied to the analog measurements prior to the A/D conversion. The offsets are programmed to “zero” for unipolar inputs and to 50% full scale for bipolar inputs. This results in a uniform A/D input signal level of 0-5 Volts for all analog signals. Note that due to the symmetrical characteristics of the bipolar signals, only 50% full-scale offsets are required. (Non-symmetric data signals would require offsets tailored to input signal characteristics.) This simplistic design thus achieves the required accuracy as shown by the calculations in Figure 3B.

OPERATIONAL PAYLOAD SIMULATOR

The simulator dual-simplex bus uses optical couplers to interface with an avionics computer. These couplers provide the necessary isolation required by the avionics system. The simulator state machine receives and recognizes 20 valid command messages and responds with 7 unique predetermined messages. The byte format of each message is: a start bit, 8 data bits, 1 parity bit, and a stop bit transmitted in a serial data format, LSB first. When valid command messages are recognized, associated data and CRC (circular redundancy check) words of the message are ignored. The recognized sync word is then used to initiate sending a “canned” response message, and sets a “bit” in a digital word, indicating that the command has been received and recognized. Each message includes a status word, data words, a two-word CRC, and a synchronization word, occurring in the following order:

STATUS WORD, DATA WORD,..,DATA WORD, CRC1 WORD, CRC2 WORD, SYNC

The two “canned” CRC words in the 7 response messages are derived using Modulo 2 arithmetic from the first 6 least significant bits of the status and data words of the message. The sync word is not used in the derivation. The CRC polynomial for the derivation is $X^{12} + X^{11}$, $+ X^3 + X^2 + X + 1$. The generated CRC

word 1 contains the 6 least significant derived CRC bits appended with a binary 01. CRC word 2 contains the derived 6 most significant bits, also appended with a binary 01.

The simulator also accepts a timing discrete (minimum pulse duration of 3 milliseconds) from the avionics computer through an optically-isolated interface. The coupled signal interfaces with an analog channel sampled at 1000 times per second.

ACKNOWLEDGMENTS

The system described in this paper is the result of cooperation between Boeing Aerospace and Loral Conic personnel. The authors wish to thank the participants from both organizations for their enthusiasm and dedication during system development and the preparation of this paper.

TABLE 1. 1553 24 BIT WORD STRUCTURE

ID BITS	±	DATA BITS	WORD DESCRIPTION
P 0 0 0 1 1 1 1	+	16	COMMAND A
P 0 0 0 1 1 1 0	+	16	STATUS A
P 0 0 0 1 1 0 1	+	16	DATA A
P 0 0 0 1 1 0 0	+	16	ERROR A
P 0 0 0 0 0 0 1	+	16	FILLER
P 0 0 0 1 0 1 1	+	16	COMMAND 8
P 0 0 0 1 0 1 0	+	16	STATUS B
P 0 0 0 1 0 0 1	+	16	DATA B
P 0 0 0 1 0 0 0	+	16	ERROR B

A = Primary channel of a dual redundant bus
B = Secondary channel of a dual redundant bus
P = Parity Bit (odd parity)

TABLE II. MULTIPLEXER FORMAT

```
A B C D E F G H I J K L M N -WI-- -W2-- -W3-- -W4--
A B C D E F G H I J K -W5-- -W6-- -W7-- -W8-- -W9--
A B C D E F G H I J K L M N -W10- -W11- -W12- -W13-
A B C D E F G H I J K -W14- -W15- -W16- -W17- -W18-
A B C D E F G H I J K L M N -W19- -W20- -W21- -W22-
A B C D E F G H I J K -W23- -W24- -W25- -W26- -W27-
A B C D E F G H I J K L M N -W28- -W29- -W30- -W31-
A B C D E F G H I J K -W32- -W33- -W34- -W35- -W36-
A B C D E F G H I J K L M N -W37- -W38- -W39- -W40-
A B C D E F G H I J K -W41- P U U U U U Q Q S S S I

8 BITS/WORD   250 WORDS/FRAME     1000 FRAMES/SEC 2.0 MBPS
  32 FRAMES/MAJOR FRAME     14 SUPERCOM WORDS
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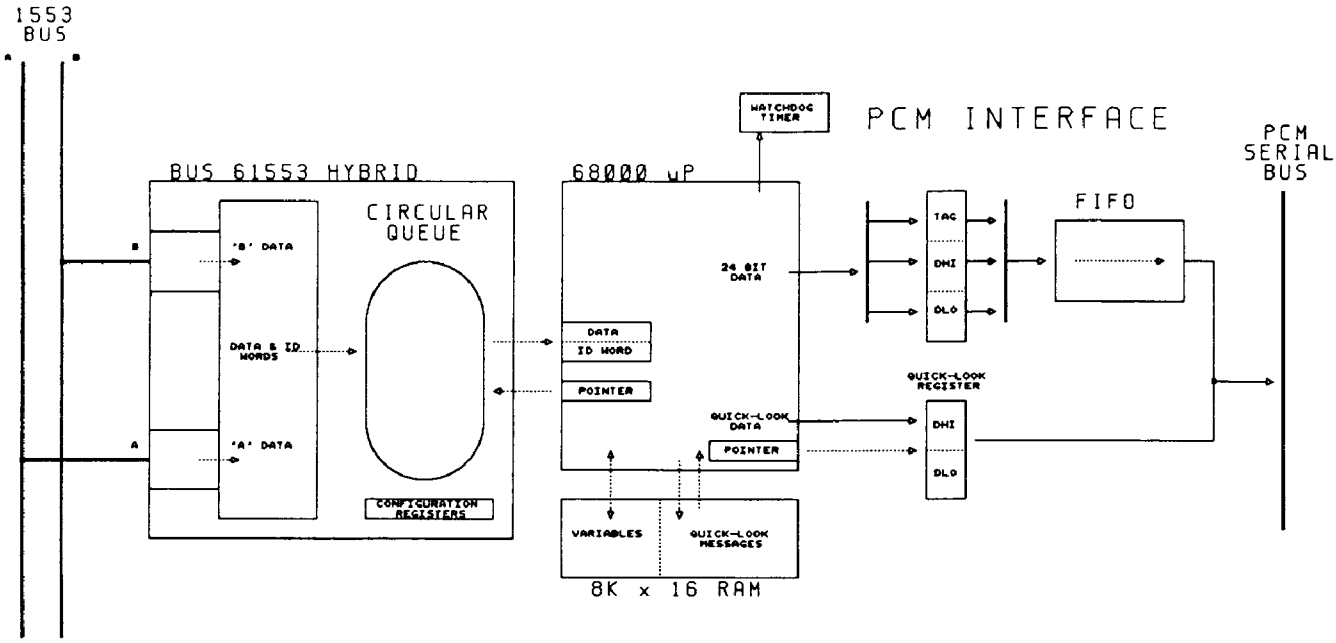

1553
BUS
WATCHDOG
TIMER
PCM INTERFACE
PCM
SERIAL
BUS
BUS 61553 HYBRID
68000 uP
CIRCULAR
QUEUE
FIFO
B
'B' DATA
DATA & ID
WORDS
A
'A' DATA
CONFIGURATION
REGISTERS
DATA
ID WORD
POINTER
24 BIT
DATA
TAG
DHI
DLO
QUICK-LOOK
REGISTER
QUICK-LOOK
DATA
POINTER
DHI
DLO
VARIABLES
QUICK-LOOK
MESSAGES
8K x 16 RAM

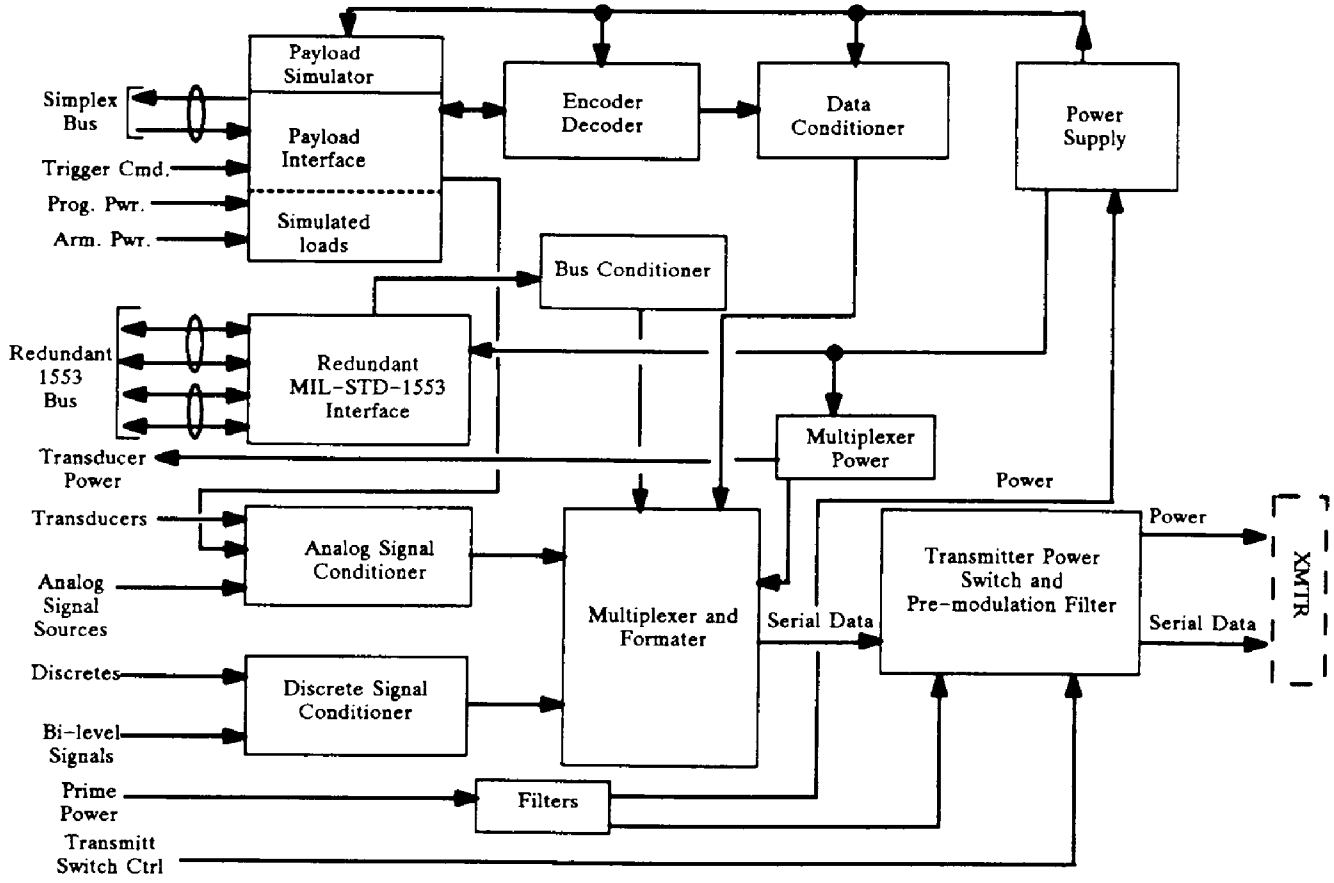
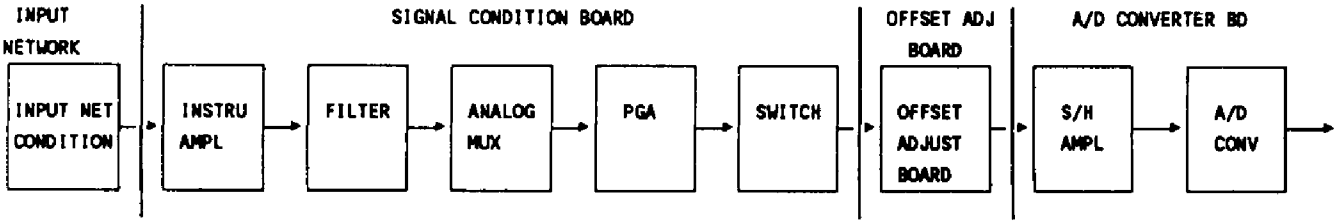

Payload Simulator
Payload Interface
Simulated loads
Simplex Bus
Trigger Cmd.
Prog. Pwr.
Arm. Pwr.
Encoder Decoder
Data Conditioner
Power Supply
Bus Conditioner
Redundant 1553 Bus
Redundant MIL-STD-1553 Interface
Multiplexer Power
Transducer Power
Power
Transducers
Analog Signal Conditioner
Analog Signal Sources
Multiplexer and Formater
Serial Data
Transmitter Power Switch and Pre-modulation Filter
Power
Serial Data
XMTR
Discretes
Discrete Signal Conditioner
Bi-level Signals
Prime Power
Filters
Transmitt Switch Ctrl

Figure 1

SIGNAL CONDITIONING ACCURACY ANALYSIS

The following flow diagram depicts a typical path for the acquisition of an analog signal into the PCM NRZL data stream and the errors that are accumulated along the way:



ERROR:

A B C D E F G H I

A = RSS error due to the input conditioning on the Input Network board.

B = RSS error due to the Instrumentation Amplifier on the Signal Conditioning Board at a specific gain setting.

C = RSS DC error due to filtering on the Signal Conditioning Board.

D = RSS error due to the analog multiplexer on the Signal Conditioning Board.

E = RSS error due to the PGA unit on the Signal Conditioning Board.

F = RSS error due to leakage of the output switch on the Signal Conditioning Board.

G = RSS error due to the Offset Adjustment Board.

H = RSS error due to the droop characteristics of the Sample/Hold Amplifier on the A/D Converter Board.

I = RSS error due to the A/D conversion on the A/D Converter Board.

$$\text{TOTAL SYSTEM RSS ERROR} = \sqrt{\sum_{X=A}^{I} \left[X \right]^2} \quad ; \quad \text{RSS = ROOT SUMMED SQUARE}$$

Calculation for RSS value is as defined above. Because RSS values are additive, the total system error shall be an RSS value of the component errors A through I which shall have been RSS calculated as well.

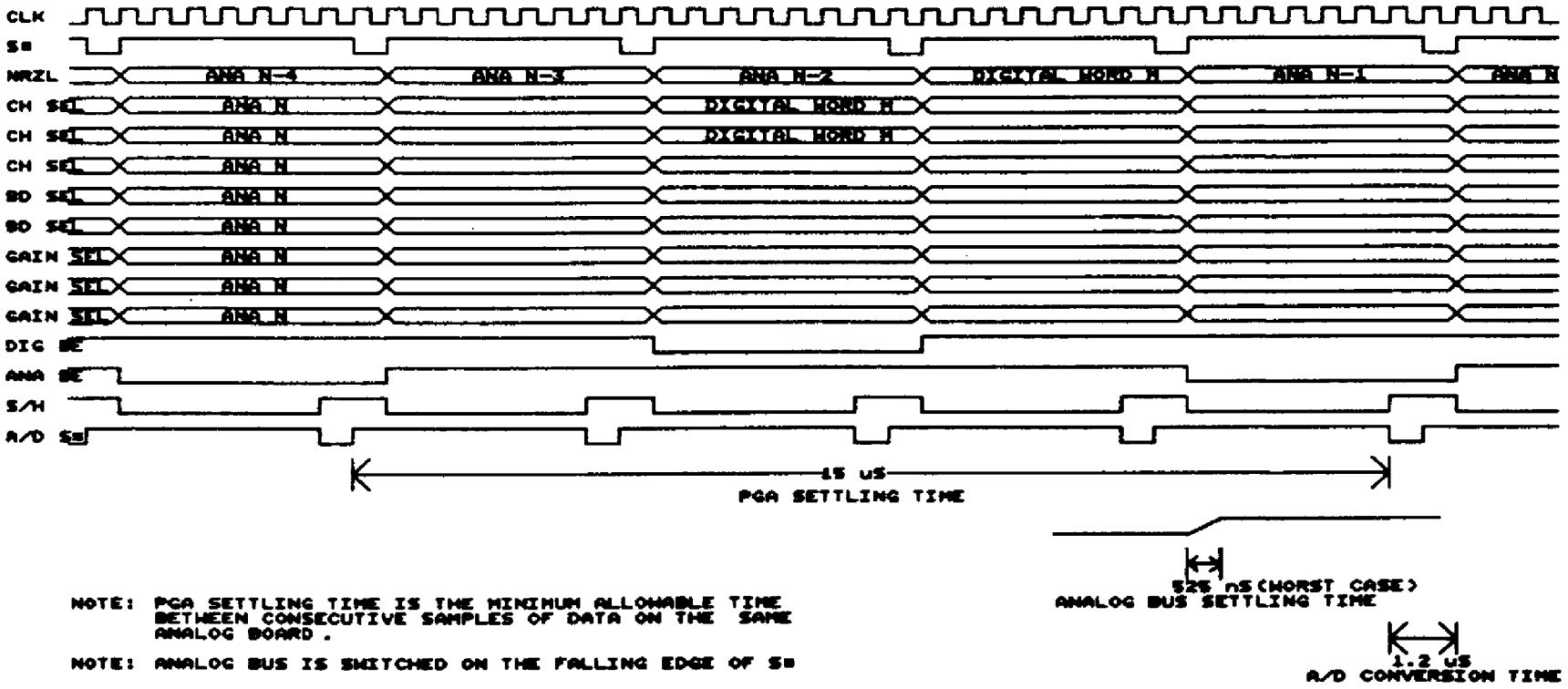
Also, one major assumption made was that initial errors such input offset voltages, gain tolerances, etc, are trimmable to zero and, thus, are not included in the accuracy analysis.

Figure 3A.

OVERALL SYSTEM RSS ERROR - INITIAL ERRORS ARE TRIMMED TO ZERO

	SIGNAL	RSS ERROR A	RSS ERROR B	RSS ERROR C	RSS ERROR D	RSS ERROR E	RSS ERROR F	RSS ERROR G	RSS ERROR H	RSS ERROR I	RSS OVERALL ERROR
Strain Inputs	P1	0.2112%	0.304%	0.016%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.5374%
	P3-P8	0.2112%	0.304%	0.007%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.5371%
	S1-S6	0.2112%	0.244%	0.009%	0.004%	0.036%	0.0003%	0.3142%	0.0243%	0.256%	0.5200%
	S7-S14	0.2112%	0.478%	0.009%	0.004%	0.036%	0.0003%	0.3142%	0.0243%	0.256%	0.6628%
Vibration Inputs	V1-V11	-------	0.211%	0.013%	0.004%	0.036%	0.0003%	0.3142%	0.0243%	0.256%	0.4592%
Resistance Temp. Devices	T1-T3,T6,T9, T10,T11,T13, T14,T19-T22, T25,T26	0.5936%	0.304%	0.007%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.7722%
	T5,T15,T16 T18,T23,T24	0.5936%	0.304%	0.004%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.7722%
Thermo-couples	T4	0.7018%	0.707%	0.004%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	1.0695%
	T7,T8,T12	0.7018%	0.707%	0.007%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	1.0695%
	T17	0.7018%	0.972%	0.007%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	1.2605%
Acoustics	A1-A4	0.206%	0.172%	0.009%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.4729%
Missile-power	E1,E2,E4	0.3802%	0.172%	0.007%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.5707%
Fire Command	E3	-------	0.172%	0.007%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.4256%
Voltage Meas.	E13,E14	0.206%	0.172%	0.007%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.4728%
	E15,E16	0.3827%	0.172%	0.007%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.5723%
	E17-E19,E23	0.3827%	0.172%	0.004%	0.004%	0.036%	0.0003%	0.2899%	0.0243%	0.256%	0.5723%
	E20-E22	0.3093%	0.172%	0.013%	0.004%	0.036%	0.0003%	0.3142%	0.0243%	0.256%	0.5400%

Figure 3B.



NOTE: PGA SETTLING TIME IS THE MINIMUM ALLOWABLE TIME BETWEEN CONSECUTIVE SAMPLES OF DATA ON THE SAME ANALOG BOARD.

NOTE: ANALOG BUS IS SWITCHED ON THE FALLING EDGE OF S#