STRETCHING THE CAPABILITIES OF TAGGED DATA WORD SELECTION

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ABSTRACT

The goal of Word Selector hardware design is to place the selection and scaling of displayed data parameters under the control of destination observers. An initial design, discussed at the 1984 ITC, received its input telemetry data from a Compressor with modest throughput. The proliferation of nontraditional formats has forced the adoption of telemetry data preprocessors in place of simple Compressors. A new generation of Word Selectors is being developed with greater speed (1 million parameters/second), a serial data interface, and the equivalent scaling capability of traditional patch panel demultiplexers. The number of nonvolatile local setup files has been increased by 40%.

INTRODUCTION

Digital data buses and Word Selectors have been added to the Naval Weapons Center (NWC) Telemetry Ground Station to supplement an existing analog data distribution system. The display of digital format data is an outgrowth of a requirement to supply NWC's Range Control Center with real-time data and appended identification tags. The Word Selector effort has overcome the inherent growth limitations of analog patch panels and made use of existing computer and compressor equipment,

Figure 1 is a ground station digital data flow diagram showing 34 existing Word Selectors and two newly acquired EMR 8715 Preprocessors. The 8715s replaced EMR 714 Compressors which had no data processing ability other than tagging and pass/fail. While it is acknowledged that these preprocessors do have the ability to manipulate data and assign it to destinations, the intention is to operate with generalized setup files and throughput all data of potential interest. Selection and scaling of specific parameters can be accomplished in simple Word Selectors that individually are responsible for a small fraction of data traffic. The Word Selector concept has grown from a way to realize digital data distribution to a way to complement powerful preprocessors with hardware that is easy to set up and modify.

MOTIVATIONS FOR REDESIGN

The initial Word Selector, introduced in 1984, has been refined to the extent of its flexibility. Binary, offset binary, and 2's complement formats can all be scaled by bit deletion. Internal realization of most significant bit (MSB) alignment (variable word length capability) has always been part of the design. Recently, a useful step in operability was made by embedding three-step calibration data into live telemetry. This latest refinement was in support of multiple simultaneous telemetry exercises. In general, the circuit design was felt to be adequate for production and 40 units have been built.

Adoption of 8715 preprocessors has made it advisable to review the Word Selector design for potential upgrades. Foremost, the preprocessors have a throughput capacity of 600K words/second with expansion capability. The design goal is to improve maximum Word Selector throughput from 400K words/second to 1 million words/second.

Experience with using the existing Word Selector has shown that its inability to create multiple displays from the same tag is a serious limitation. Similarly, the proliferation of binary discrete data has shown arbitrary bit selection in the fashion of patch panel demultiplexers to be a desirable feature. The combination of these two features—multiple displays from same tag plus arbitrary bit manipulation—creates the ability to "unpack" data in unlimited ways. The present ability to scale binary, offset binary, and 2's complement data is not sacrificed.

ADDITIONAL DESIGN GOALS

Serial Data Interface

The transparent asynchronous transceiver interface (TAXI) is available from Advanced Micro Devices, Inc. for transmission and recovery of parallel data over a serial link. The versatile chip set can operate in cascade mode for transmission of 32-bit words. The synchronization overhead associated with TAXI makes serial data rate 50 Mb/s for a parallel rate of 1 million 32-bit words/second. The serial data is emitter-coupled logic (ECL) and can be transmitted over a pair of RG-58 cables. It will be necessary to construct a tree of ECL buffers to ensure proper termination of the highly fanned-out system.

RS-232 Remote Setup

The strictly manual setup control of the first Word Selector has proven somewhat awkward when reconfiguring from one predefined format to another. Although only four keystrokes art required to reconfigure each box, a bank of 20 Word Selectors can be a

burden on a busy schedule. A 9600-baud RS-232 interface is being prepared to make a host computer setup possible,

PROCESSOR ORGANIZATION

A flow diagram of the new design (Figure 2) demonstrates its essential simplicity. As soon as a 32-bit word is received, the tag value is used as an address to 32K-byte RAM. The output byte assigns any combination of eight digital-to-analog converters (DACs) to the corresponding data field. Only 15 out of 16 tag bits are used since the most significant tag bit has been mandated to be logical “one.”

Simultaneously, the 16-bit data field is mapped into 9-bit DAC inputs. The bit mapping is accomplished by an army of nine 16-input multiplexer (MUX) chips. Each MUX selects a single DAC input bit. Associated with each MUX block is a gate that can invert the bit (MSB only) or replace it with logical “zero.”

Each incoming data field is bit-mapped eight times for the eight DACs, regardless of how many DACs have actually been assigned. In the majority of cases, the number of assigned DACs will be zero or one. Figure 3 illustrates the timing sequence for each input parameter. Bit mappings are executed at a 10-MHz rate. The Word Selector is ready to accept a new input 0.9 microsecond after latching the last input.

MICROCOMPUTER CONTROLLER

Sixty-nine byres of information are required for a Word Selector setup—24 bytes are used for TAG RAM and 45 bytes for multiplexer control. EEPROM memory with a capacity of 8K bytes can store 118 setups. Creation, storage, and retrieval of this information is performed manually with a keypad and 80-character IEE display (Figure 4). The microcomputer controller is based on an MC 6809 microprocessor. TAG RAM (32K x 8) and Bipolar RAM (8 x 45) are placed on the microprocessor bus by three-state transceivers for setup.

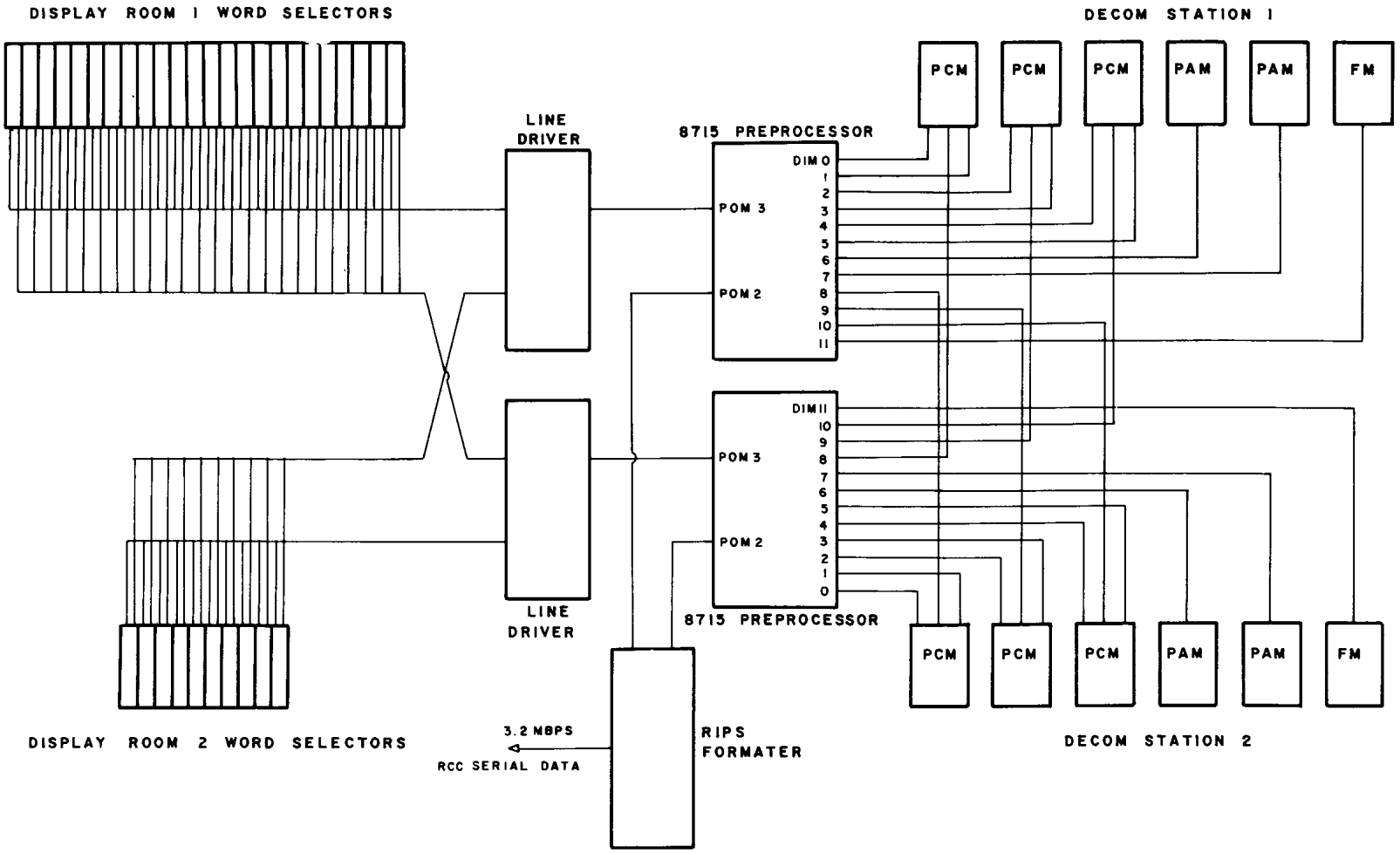

Figure 1. T-Pad Digital Data Flow Diagram.

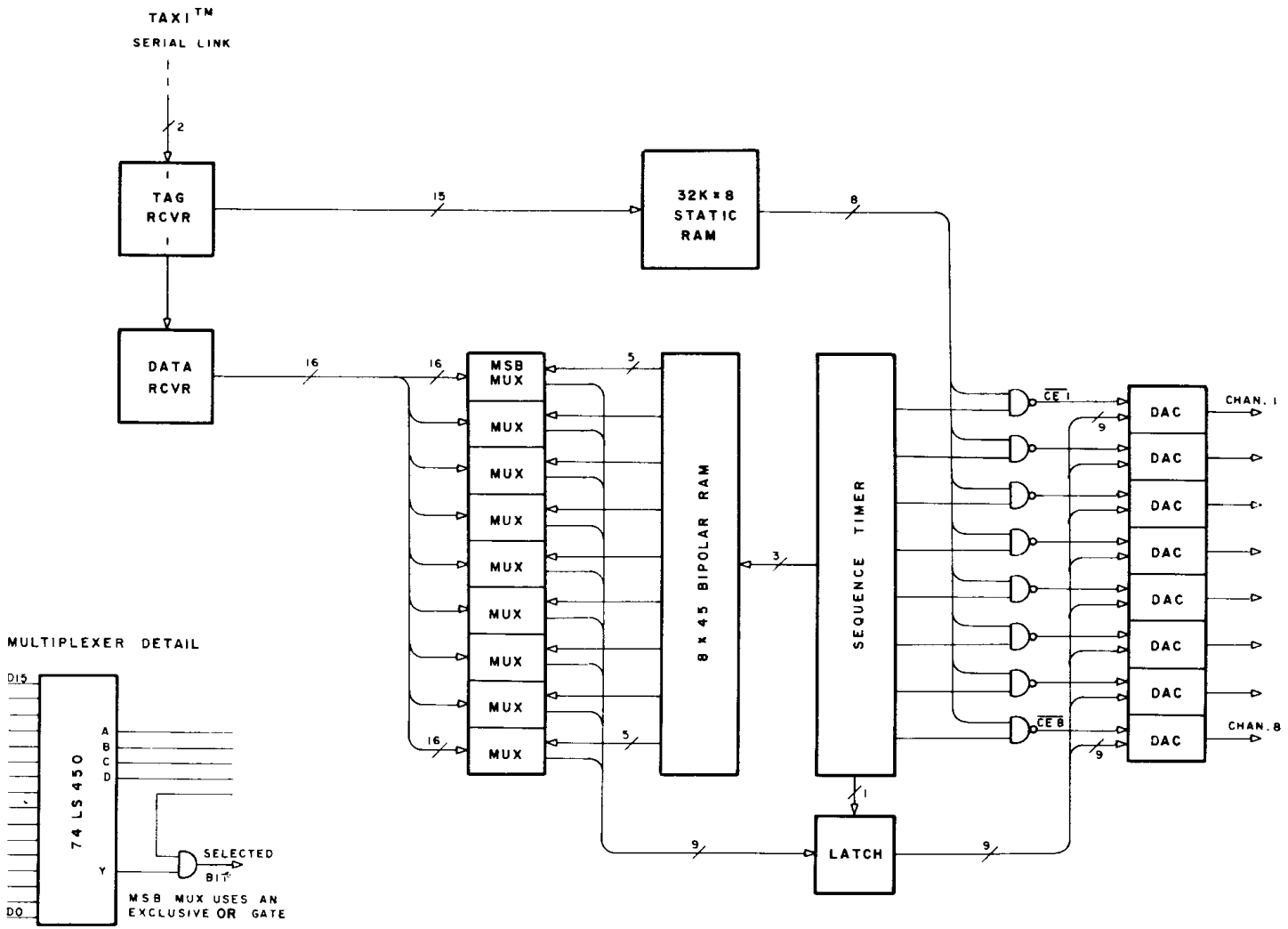

Figure 2. Processor Flow Diagram.

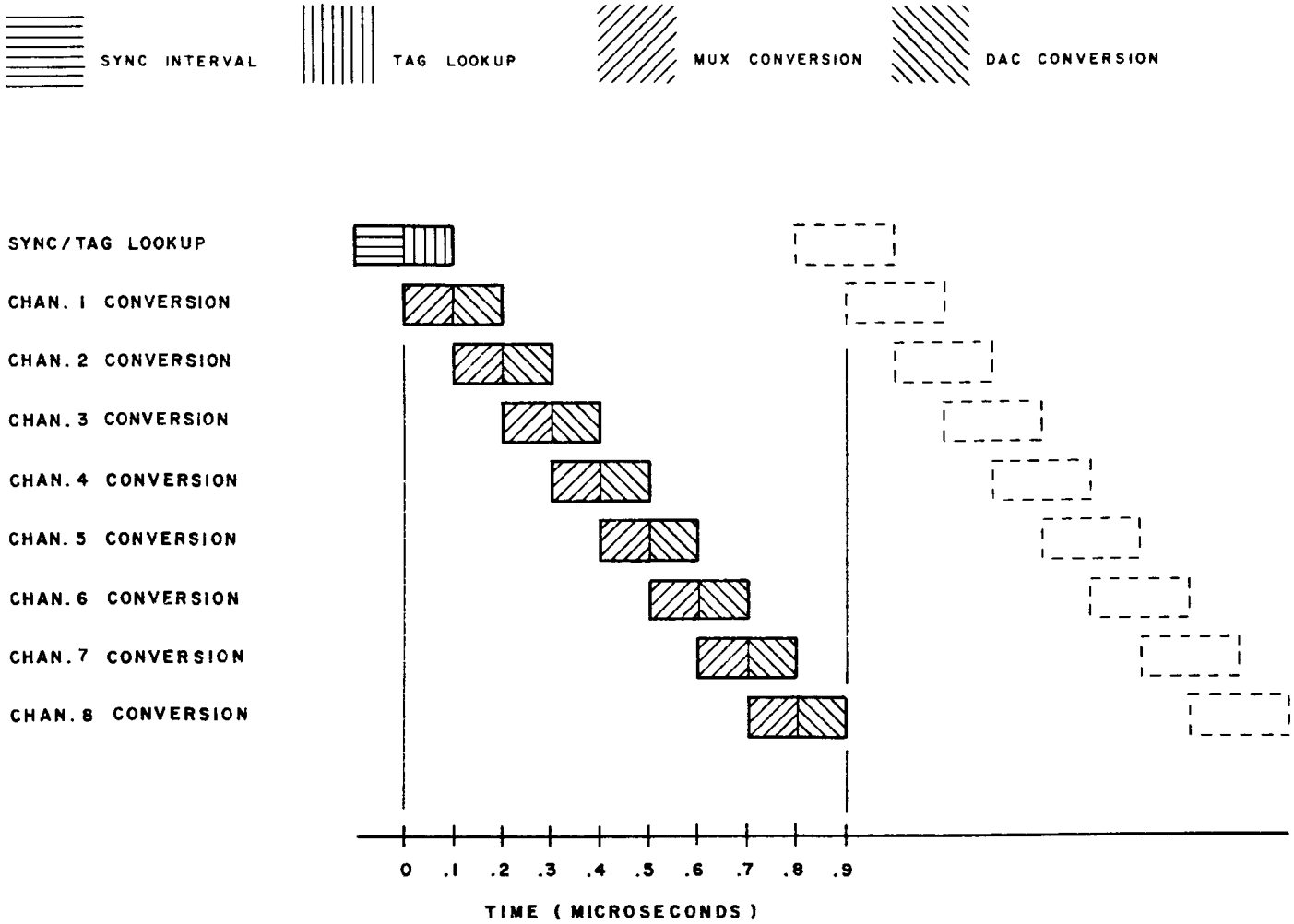

Figure 3. Overall Timing.

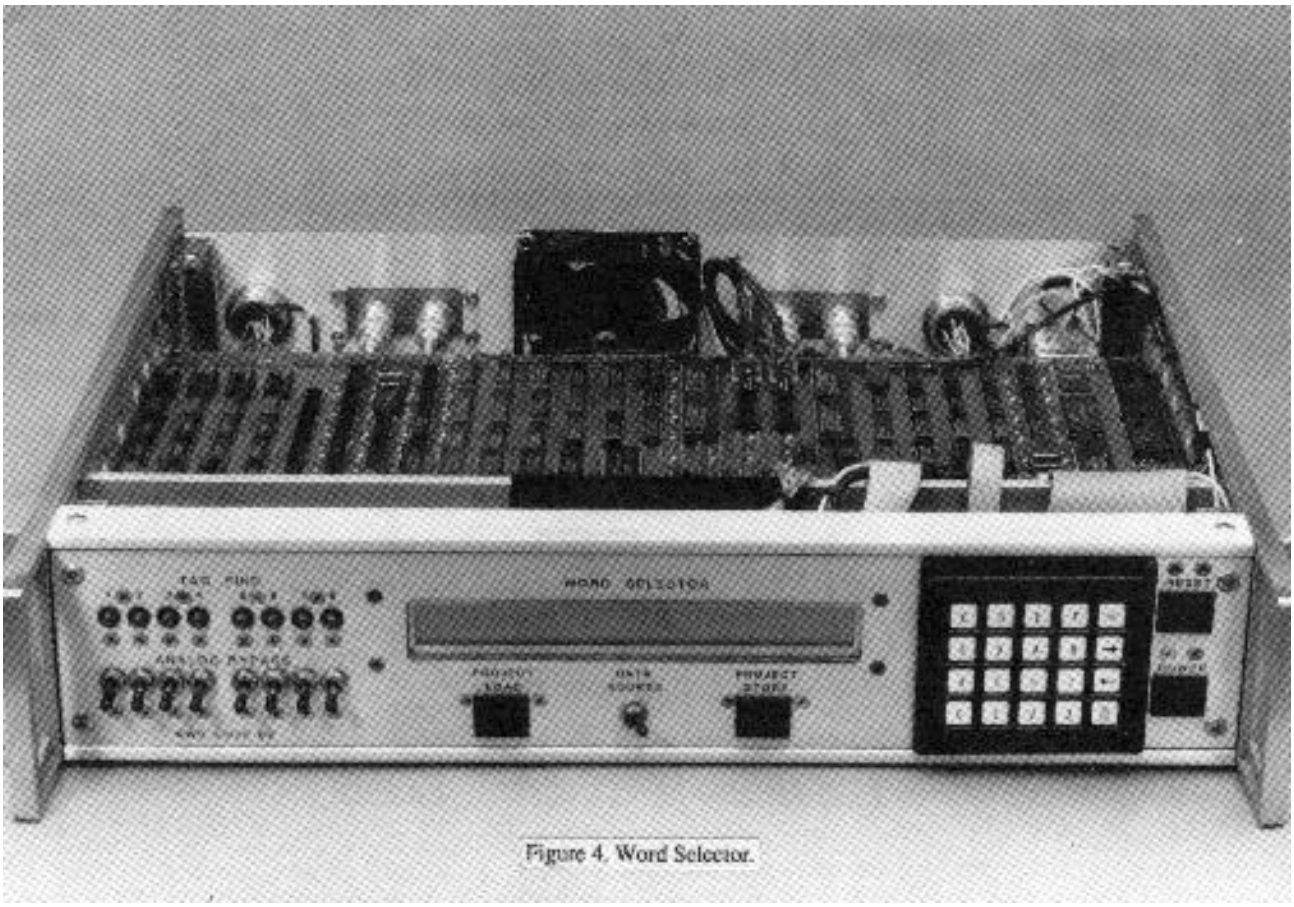

Figure 4. Word Selector.