DIGITAL TV TRI-STATE DELTA MODULATION SYSTEM FOR SPACE SHUTTLE KU-BAND DOWNLINK

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ABSTRACT

The anticipated requirements for Shuttle Orbiter Ku-band downlink communication include the transmission of a digital video signal which, in addition to accommodating the black-and-white TV pictures, must also be able to relay to the ground the color TV information encoded in either field-sequential or NTSC color formats. Furthermore, at the expense of additional onboard hardware and increased bandwidth due to the digitization process, the picture privacy feature can be provided for the downlink. Thus, an objective for the future Space Shuttle TV equipment is the development of a digitization technique which is not only compatible with data rates in the range of 20 -30 Mbps, but also provides good quality pictures.

This paper desribes a tri-state delta modulation/demodulation (TSDM) technique which is a good compromise between implementation complexity and performance. The salient feature of TSDM is that it provides for efficient run-length encoding of constant-intensity segments of a TV picture. Axiomatix has developed a hardware implementation of a high-speed TSDM transmitter and receiver for black-and-white TV or field-sequential color or NTSC format color. The hardware aspects of this TSDM are discussed in the paper also.

INTRODUCTION

The existing Space Shuttle onboard equipment provides for transmission of analog TV signals via an S-band (2250 MHz) FM downlink. This downlink, however, is available only when the Shuttle is within line of sight of a ground station. Furthermore, because of the severe constraints on the effective radiated power, the bandwidth of this link is limited, thus precluding the use of any “privacy” feature for the downlink TV signal.

In the near future, a forthcoming Ku-band communication system(1) onboard the Shuttle Orbiter will utilize a high-gain steerable-dish antenna to communicate with NASA's Tracking and Data Relay Satellite System (TDRSS) to provide a TV transmission capability simultaneous with two other communications channels. Alternately, 50 Mbps of payload digital data can be provided simultaneously with the other two communications channels. Initially, the TV modulation technique will be analog FM, similar to S-band, with no privacy capability. A potential requirement for privacy, however, can best be provided by digital techniques. Scrambled digital TV, if implemented at moderately low data rates, will also provide the possibility of simultaneous transmission of payload digital data as long as the total data rate (TV plus payload data) is within the 50 Mbps Ku-band system capability.

Figure 1 shows the overall space and ground functional configuration which could be used to accommodate Shuttle digital TV with scrambling for privacy to be transmitted to the U.S. Air Force Satellite Control Facility (SCF) and the NASA Johnson Space Center (JSC).

POTENTIAL TECHNIQUES FOR TV DIGITIZING

The commonly used delta modulation encoder produces a sequential output that indicates whether the final output voltage should increase or decrease. It acts like a DPCM system with only one bit per sample. Hence, it is referred to as a "bistate" encoder. Acceptable performance with this encoding scheme is realized by an increased sampling rate as compared to a PCM coding scheme. Because the bistate delta modulator requires relatively low data rates compared to PCM, considerable effort has been spent trying to perfect a delta modulation system(2,3).

The goal of every design approach is to trade off fidelity of reproduction versus the allowable data transmission rate and the amount of hardware used. The best solution also depends on the qualities of the signal being sampled. Video information tends to be a series of amplitude steps from one luminance level to another. These level steps are connected by voltage changes with large dv/dt values. When handling a video signal, a delta modulator must handle very sharp rise and fall time signals, then settle rapidly to a new luminance value, with no overshoot, ringing or other added noise. The relative delay for different frequency components in the picture is also important.

Figure 2 is a block diagram of a bistate delta modulator which illustrates its operation. D_k is the difference between the input signal S_k and the output of the estimator X_k. This difference signal is passed through a hard limiter whose output is a bit B_k which causes the estimator to change its output. This bit is the signal which is transmitted over a communication link to the receiver. The receiver consists of only the estimator portion of

the transmitter block diagram. The sampling rate of the delta modulator determines the amount of delay inherent in the digitizing process. The faster the sampling rate, the smaller the inherent delay.

The hard limiter in Figure 2 guarantees that the estimator will increase or decrease its output every time the sample clock cycles. This characteristic of indicating only changes results in the inherent "granularity" in the reproduction of a constant-luminance signal since the modulation scheme must always output a sample corresponding to an increase or decrease in voltage. The reconstructed signal will average to the correct level by varying up and down around the desired output level. Any attempt to smooth the delta demodulation output will slow the response to step changes and, therefore, reduce picture "sharpness."

Conversely, if the bistate delta modulation scheme is designed to provide good rise and fall times, the amplitude of the level jitter around the desired output will increase and more granularity will appear. Furthermore, the amount of overshoot and ringing after an abrupt edge will, in general, increase as the delta modulator system is designed to reduce slew time. Various attempts to alleviate these conflicting requirements and reduce the overshoot and ringing have been proposed(4,5).

TRI-STATE DELTA MODULATION TECHNIQUES

The tri-state delta modulator (TSDM)(6,7) has characteristics that make it especially suitable for encoding video information. By indicating the "no-change condition" with a special code, the TSDM breaks the connection between rise time performance and steady-state level jitter inherent in a bistate delta modulator.

In comparison with the bistate delta modulation, the TSDM approach shown in Figure 3 quantizes D_k into three values instead of two. The third value indicates that D_k is between $-\epsilon_v$ and $+_{\epsilon v.}$ This condition causes the output of the estimator to remain at its previous value. Just as in the case of bistate delta modulation, the receiver consists of the estimator only. This third state eliminates the granularity inherent in bistate delta modulation; it permits the TSDM to be optimized for transient performance without considering granularity problems. With the exception of the third state, the operation of the TSDM is identical to the bistate delta modulator shown in Figure 2.

As indicated in Figure 3, the TSDM state is determined by comparing the estimate X_k with the input signal S_k to produce a voltage difference signal D_k. This voltage D_k is tested for sign and magnitude to produce B_k. The rule is:

$$B_k = \begin{cases} \text{Sgn}[D_k], & \text{whenever } |D_k| > \epsilon_v \\ 0, & \text{whenever } |D_k| \leq \epsilon_v \end{cases}$$

Since $D_k = S_k - X_k$, a positive value for D_k signifies that X_k must be made more positive to match S_k; therefore, $B_k = +1$ must cause X_k to become more positive. The equation used to calculate X_{k+1} from X_k is simply

$$X_{k+1} = X_k + B_k \left|\Delta_{k+1}\right|$$

where B_k may be +1, 0 or -1 and $|\Delta_{k+1}|$ is given by

$$\left|\Delta_{k+1}\right| = \begin{cases} 1.5\ \Delta_k \text{ if } B_k = B_{k-1} \neq 0 \text{ and } \left|\Delta_k\right| > 2\Delta_0 \\ 3\Delta_0 \text{ if } B_k = B_{k-1} \neq 0 \text{ and } \left|\Delta_k\right| \leq 2\Delta_0 \\ 0.5\ \Delta_k \text{ if } B_k \neq B_{k-1},\ B_k \neq 0,\ B_{k-1} \neq 0 \\ 0 \text{ if } B_k = 0 \\ 2\Delta 0 \text{ if } B_{k-1} = 0,\ B_k \neq 0 \end{cases}$$

When $|D_k| \leq \epsilon_v$, the feedback signal X_k is close enough in value to the input signal S_k so that the system should maintain its state. It does this by making $X_{k+1} = X_k$ and setting $\Delta_{k+1} = 0$ whenever $B_k = 0$. That process is unique to tri-state delta modulation.

The adaptive characteristic of the system is realized by the $|\Delta_{k+1}| = 1.5\ \Delta_k$ term. When B_k has the same sign m times in sequence, the value of Δk is multiplied by $(1.5)^{m-1}$ so that the slope of the feedback signal increases without limit until $X_k \geq S_k$. Once that happens, the B_k vector changes sign and the values of $|\Delta_{k+1}| = 0.5\ \Delta_k$ reduce the slope as the X_k signal changes direction. This provides for the eventual settling of X_k to a value near S_k by reducing the value of Δ_k by a factor of 2 every time X_k crosses S_k. If S_k remains constant long enough, X_k will eventually settle to within $+\epsilon_v$ of it, if ϵ_v is at least as large as 1/2 the resolution of the DAC that produces X_k. Once this happens, B_k will be equal to 0 and the systems will stay at rest until S_k changes again.

When B_k changes from $B_{k-1} = 0$ to either $B_k = +1$ or $B_k = -1$, the system must inject a starting value for $|\Delta_{k+1}|$ since $|\Delta_k|$ was 0. That is handled by the $2\Delta_0$ term which is simply a constant value selected to provide a large enough initial slope to the S_k feedback signal when it must adjust to a step input in S_k so that the slew time is minimized.

The initial value of $2\Delta_0$ must be injected whenever $\Delta_k = 0$ and $B_k \neq 0$. Two terms are required for this injection because the values of B_k, B_{k-1}, etc. are the only data available to

the estimator. A sufficient condition for $\Delta_k = 0$ is that $B_{k-1} = 0$. Therefore, whenever $B_{k-1} = 0$ and $B_k \neq 0$, the system must inject $2\Delta_0$ for Δ_k. However, it is possible for Δ_k to work its way down to 0 without ever having $B_k = 0$. This requires S_k to change value at just the right time during the process of X_k settling toward the input voltage. This eventuality is handled by the term for $|\Delta_{k+1}|$ which injects $2\Delta_0$ whenever $B_k = B_{k-1} \neq 0$ and $|\Delta_k| < 2\Delta_0$.

TSDM DIGITIZER/RECONSTRUCTOR IMPLEMENTATION

Figure 4 is a block diagram of a tri-state video digitizer with the receiver input and output indicated in dotted lines. Because the receiver is only a portion of the transmitter, it will not be discussed separately. As shown in this diagram, the analog video signal S_k is compared with the reconstructed analog estimate of the previous sample X_k. The analog difference D_k is applied to the A/D converter. The hysteresis bias, or "dead zone," $\pm\epsilon$, is also applied to the analog bias input of the A/D converter. The analog error is then sampled by the A/D unit and transformed into B_k values according to the previously described algorithm. Each B_k value, which is a two-bit number, is then applied to the B_k storage register. At the same time, the previous value of B_k is clocked into the B_{k-1} storage register. Once B_k and B_{k-1} are clocked into their respective storage registers, the logic and decision unit (LDU) initiates its analysis of the condition of these vectors.

The hardware block diagram of Figure 4 implements the required tri-state algorithm. To provide the fastest sampling rate possible, the various alternative computations are performed in parallel and the appropriate result is selected by a 4-to-1 MUX. There are two 4-to-1 multiplexers: one for the next value of x and one for the next value of Δx. The decision concerning which input to select is made by the output of the A/D converter B_k and by the comparator which operates on both $2\Delta_0$ and the output of the Δx register. The implementation shown in Figure 5 provides the maximum amount of time for the DAC, analog subtractor and three-state A/D converter to settle by performing all possible calculations while they are settling, then selecting the actual output needed. The x register input, for example, may be any one of the following numbers, x, x $+3\Delta_0$, x $-3\Delta_0$, x $+1.5\ \Delta$x, x $-1.5\ \Delta$X, x $+0.5\ \Delta$x, x $-\ 0.5\ \Delta$x. Of these seven possible values, three may be eliminated by using the previous value of B_k i.e., B_{k-1}. That is the reason why the decoding logic driven by the B_{k-1} register, in turn, drives the x register adder/subtractor units comprised of ALU's A, B and C. However, at any particular sample time, only one of these ALU's has the right value of next X_k.

As shown in Figure 4, there are three output line groups emerging from the LDU. One of these output line groups (a dual line) controls the two 4-to-1 multiplexers. The second single line controls the 2-to-1 multiplexer. Finally, a six-wire output line group (comprised of three dual lines) controls the three ALU's. Depending on the present vector B_k and the

preceding vector B_{k-1}, the LDU sends the appropriate commands to the 4-to-1 multiplexers. It also sends the appropriate add/subtract commands to the x-register ALU's A, B and C. The ALU at the output of the Δx register, however, is always in the "add" mode. In this ALU, the value of Δx is added to a "right-shifted" value of itself (i.e., 0.5 Δx), thus providing the next value of 1.5 Δx. To ensure that the Δ-modulator does not "hang up" within a dead zone, the output of the Δx register is always compared with the $2\Delta_o$ value. If the value of the Δx register is less than $2\Delta_0$, the comparator controls the 4-to-1 multiplexers to select $3\Delta_0$ as the next increment. The value of $3\Delta_0$ is also selected when the LDU indicates that a transition from a no-change state (i.e., constant intensity) to a change state, i.e., an increase or decrease in intensity has occurred on the latest sample.

For the receive mode, the logic implementation is the same as that shown in Figure 4, but without the analog subtractor or A/D converter. As indicated by dotted lines, the received data stream is applied directly to the B_k and B_{k-1} storage registers and the reconstructed analog video is taken from the output of the D/A converter.

RUN-LENGTH ENCODER/DECODER IMPLEMENTATION

The block diagram of the run-length encoder used in the transmitter side of the link is shown in Figure 5. The high-speed encoding circuitry accepts the B_k values at the sample clock rate and outputs a sequence from that sample, as shown in Table 1. The sample clock rate is fixed. Since the encoding process produces a variable number of bits out, depending on the sample inputs, the data output rate of the encoder varies. Sixteen (16) bits of the encoder output are grouped together and transferred in parallel to the FIFO block. This parallel transfer reduces the data transfer rate to one acceptable by the rotating buffer.

The rotating buffer provides the necessary elastic storage between the varying input data rate and the fixed output rate. The output of the FIFO, under normal circumstances, is clocked by the transmission channel clock which is supplied to the TSDM from an external source. If the picture being transmitted happens to encode very efficiently so that insufficient data is entering the FIFO to replace the data being clocked out, the run-length encoder circuitry is apprised of this by the "potential underflow" line shown in Figure 5. When a potential underflow problem exists, the run-length encoder circuitry waits until a new horizontal synchronization pulse occurs. At this time, the run-length encoder generates a codeword indicating end of valid data. When the synchronization pulse is complete, the run-length encoder transmits another codeword, which signifies the start of valid data. In between these two times, the run-length encoder may generate fill bits of all zeros to maintain the FIFO buffer in its proper state of fill. The handling of those pictures which encode very efficiently is thus relatively simple. The rotating buffer has another

output that indicates potential overflow. This output feeds back to the encoding circuitry, which changes its operating mode when the possibility of overflow occurs.

The basic reason for potential overflow is the type of picture being encoded. The pictures with large areas of constant brightness encode very efficiently (see Table 1) and the buffer does not have an overflow problem. Those pictures having a great deal of detail with very few constant-brightness areas do not encode very efficiently. Since the tri-state delta modulator has three states for every sample instead of two, it inherently generates more data bits for a given number of samples than a bistate delta modulator. However, the general tendency for bistate delta modulation to produce granularity is less objectionable in those pictures with a large amount of detail. Therefore, the run-length encoder circuitry can change its mode of operation when the buffer is in danger of overflowing. The encoder then sends a special sequence for its horizontal synchronization word which indicates the change of mode, and the encoder switches to bistate delta modulation. This removes the encoding table and merely sends a normal bistate delta modulation stream over the data link until the potential for buffer overflow has been eliminated.

IMPLEMENTATION OF RUN-LENGTH DECODER

Figure 6 is a block diagram of the receiver run-length decoder. It is essentially the encoder turned around. The FIFO provides data to the decoding circuitry upon demand so that the output of the decoder can be a constant sample rate despite the variable-length decoding process. The elastic storage in the receiver rotating buffer forms the other half of the elastic storage in the transmitter. The total information stored in the two memories should vary, roughly together, depending on how the picture data is modified by the encoding algorithm. The sample rate into the encoder is constant, as is the output at the decoding end of the link. The link between the encoder and decoder also has a fixed rate which is somewhat greater than the sample rate in order to obtain the improved picture quality of tri-state delta modulation. The actual link data rate and the type of picture being scanned determine how often the system degrades to bistate delta modulation.

EXTENSION OF TSDM TO NTSC COLOR TV

The previous discussion has considered TSDM as a technique for digitizing a single video signal that is presumed to be the NTSC luminance component used for black-and-white TV transmission. Because field-sequential color transmission utilizes a sequence of such components, as provided at the output of a rotating color-wheel filter, the approach described is applicable without modification for systems such as those in use today by the Space Shuttle. For standard NTSC color TV transmission, however, the TSDM technique is applied to each of the three color components, Y, I and Q, where Y is the luminance component and I and Q are the chrominance components.

Figure 7 shows the method of handling those components, each with its own run-length encoder. For maximum data comparison, each component should have its own run-length encoder before multiplexing. Otherwise, since the color and luminance components do not correlate well, there is little data rate reduction for the chrominance components when multiplexed with the luminance information.

Relative time delays are quite important in this scheme, and differential delays have to be added to the I and, especially, the Y channel to compensate for the long delay inherent in the Q channel due to its narrow bandwidth. This narrow bandwidth implies a low sampling frequency which produces more delay in the digitizing process.

SUMMARY AND CONCLUSIONS

The main advantages of TSDM are summarized as follows:

(1) It permits run-length encoding techniques to reduce required channel data rate. Depending on the particular picture being scanned, the TSDM scheme with three states per sample and run-length encoding requires less channel data rate than bistate delta modulation. While this statement does not apply to all possible pictures, run-length encoding of the TSDM output can consistently reduce the required channel data rate well below one bit per sample.

(2) TSDM eliminates granularity in the reconstructed video. It performs this function without degrading rise or fall times, compared with a bistate delta modulation system.

(3) The system described herein, when used to handle the luminance information in a color link, uses about 40 chips. This chip count does include a run-length encoder or scrambling sequence generator. A higher speed version which Axiomatix has recently completed uses about 70 chips. A receiver which may be driven by either transmitter version with minor modification uses about 36 chips.

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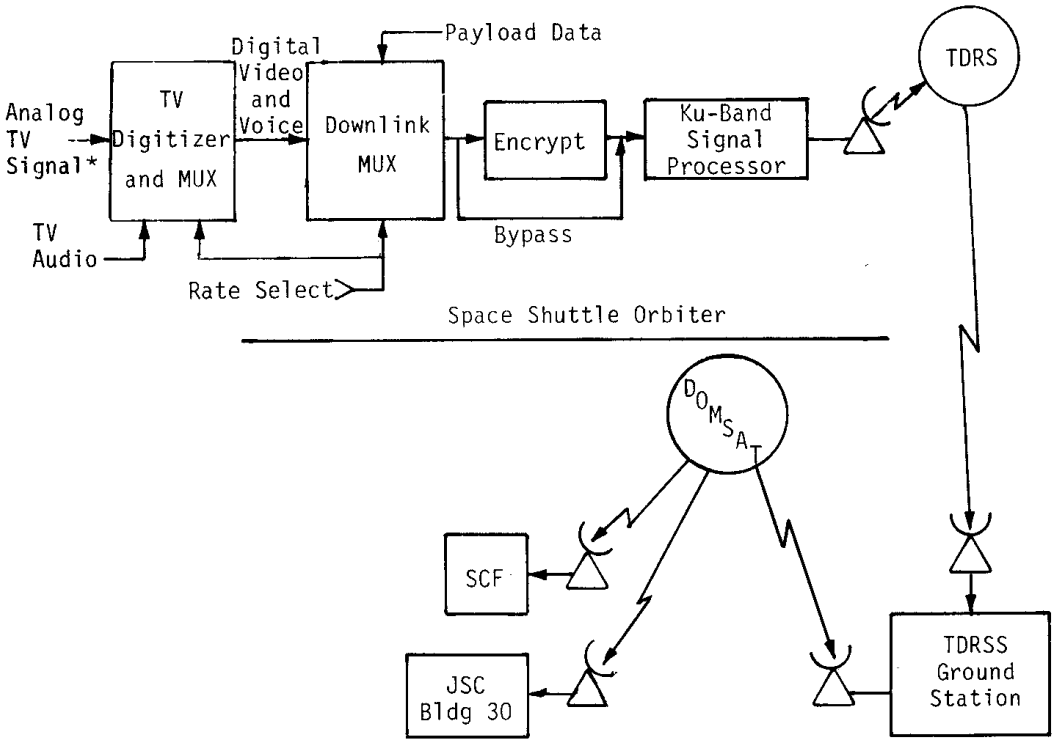
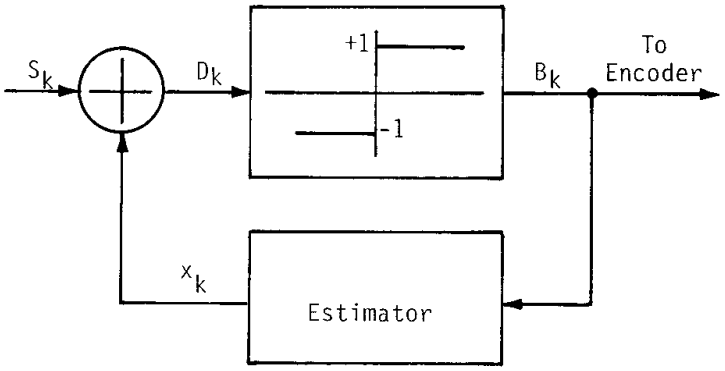


*Black and white, field-sequential color or NTSC format color.

Figure 1. Digital TV and Multiplex System Architecture: General Requirements



where:

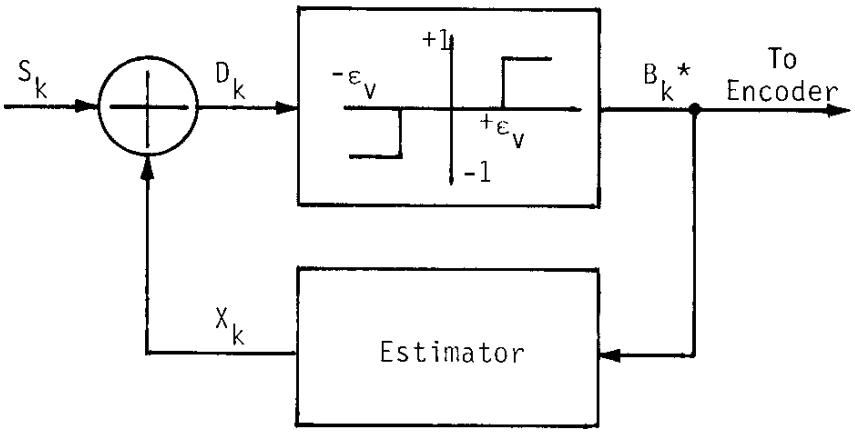
S_k = Signal to be transmitted (sampled and digital)

X_k = Estimate of signal to be transmitted

D_k = Quantized Difference ($D_k = S_k - X_k$)

B_k = Activity vector (signal rising or falling)

Figure 2. Conventional (Bistate) Delta Modulator Functional Block Diagram



*With TSDM, the B_k vector can also represent a "signal-steady" condition.

Figure 3. Tri-State Delta Modulator (TSDM) Functional Block Diagram

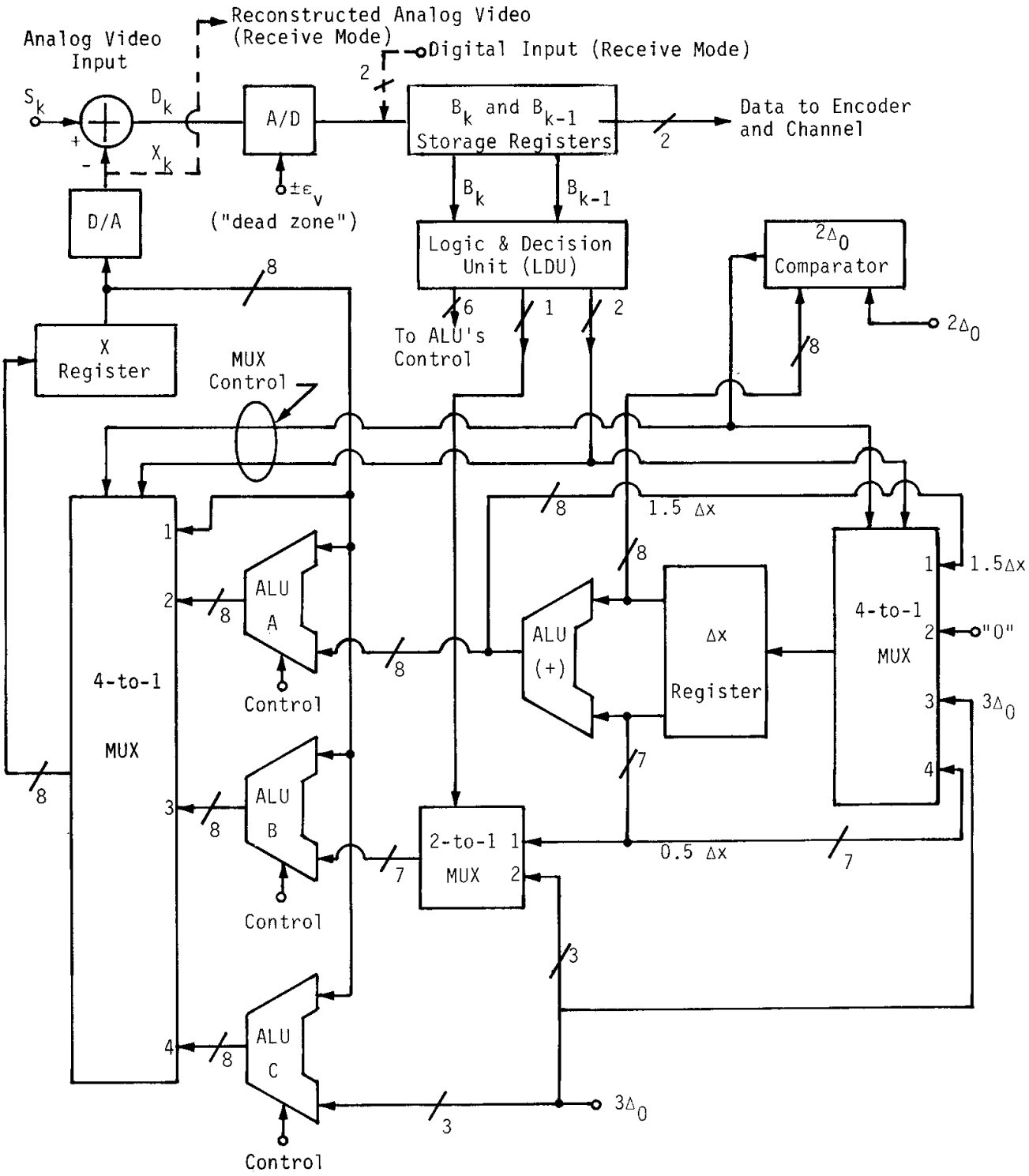


Figure 4. Tri-State Video Digitizer (and Reconstructor Block Diagram)

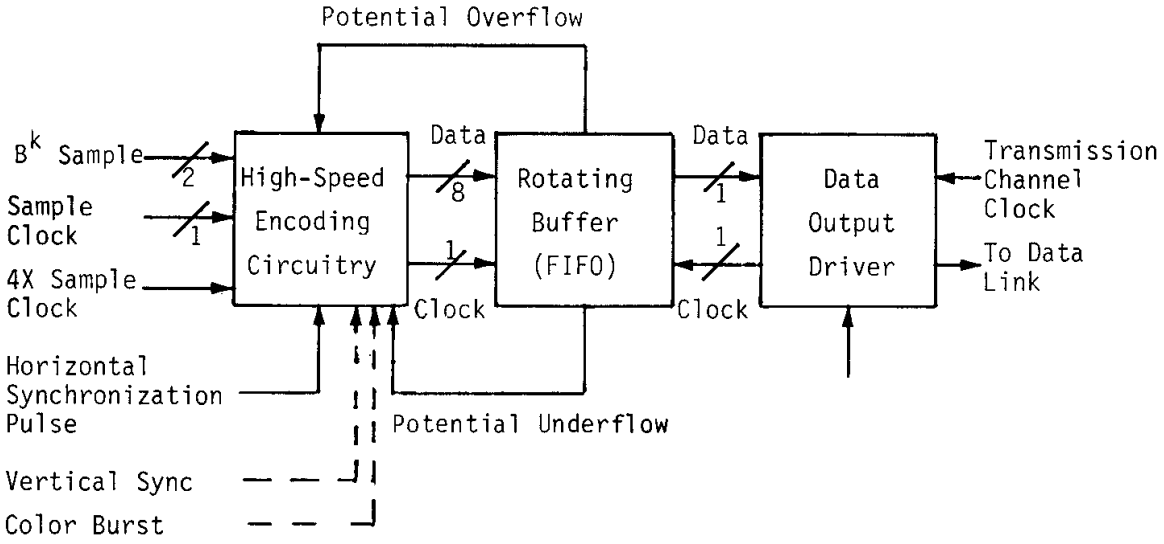


Figure 5. Run-Length Encoder (Transmitter Side)

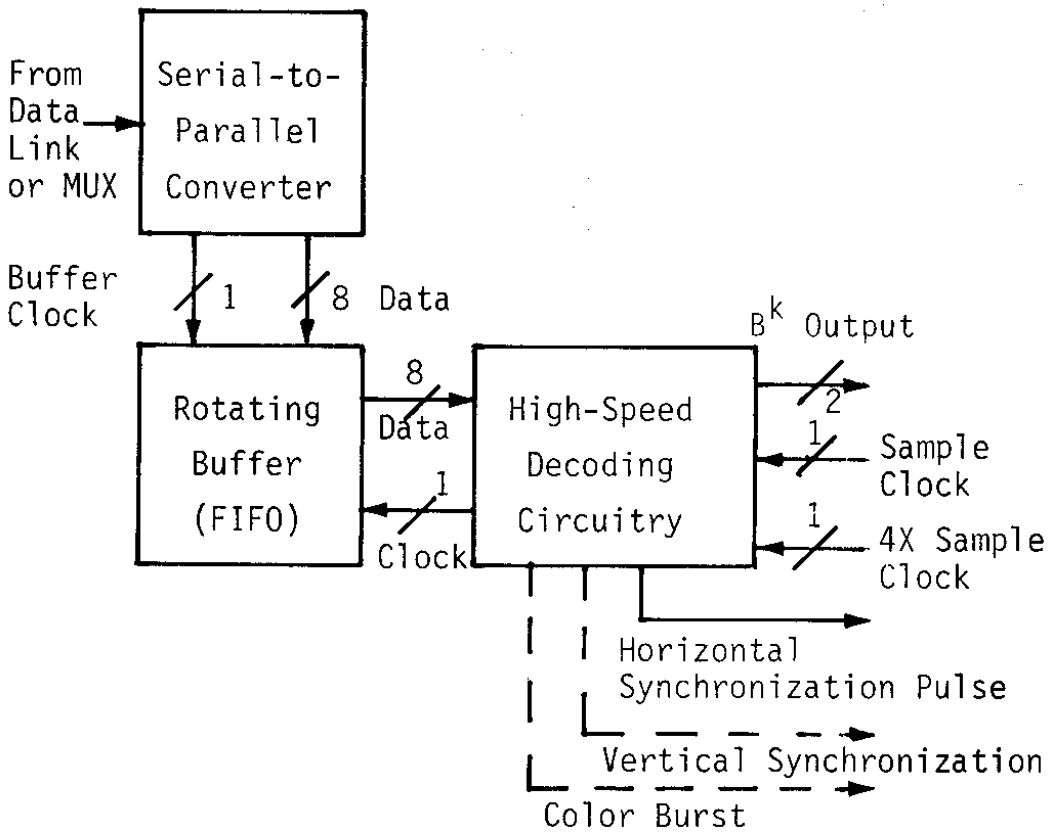
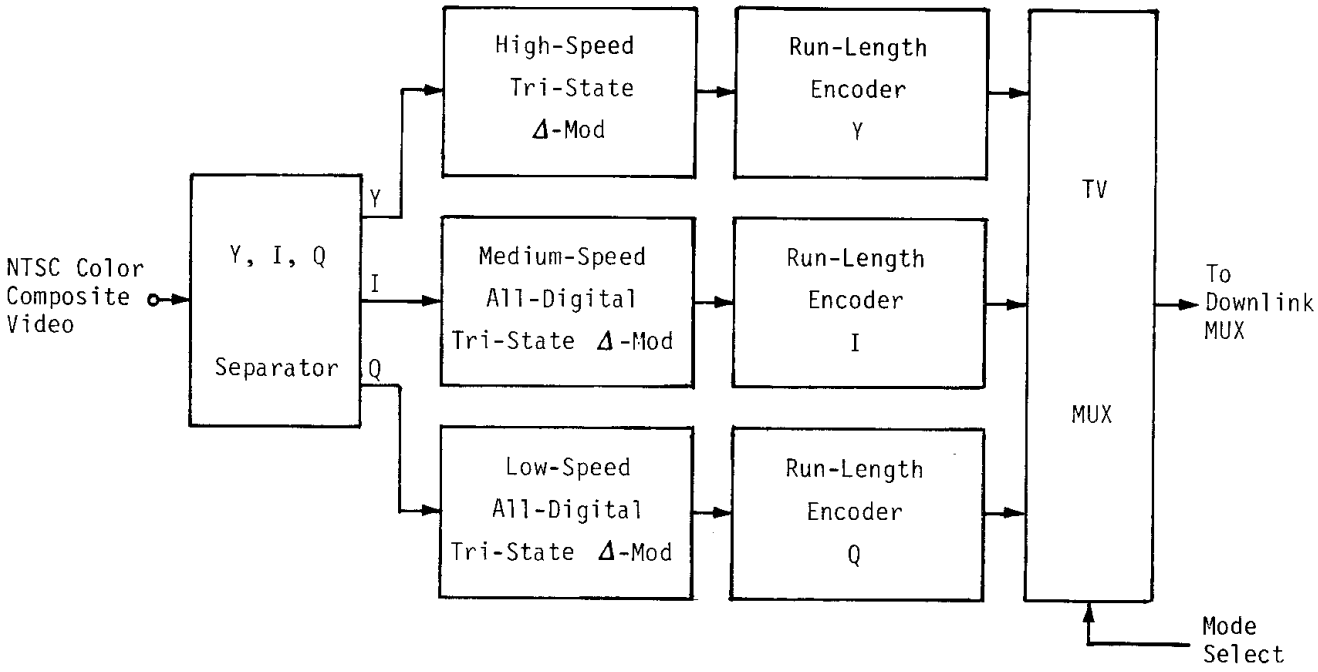


Figure 6. Run-Length Decoder (Receiver Side)



Component	Maximum Bandwidth (MHz)	Maximum* Bit Rate (Mbps)
Y	4.2	15 - 20
I	1.5	4 - 8
Q	0.5	1 - 2
		Total ≈ 20 - 30

*After coding.

Figure 7. NTSC Color TV Component Digitization

Table 1. Encoding Table

B_k Vector	Transmitted Sequence
+1	10
-1	11
0	01110
Two 0's in a row	01101
Three 0's in a row	01100
Four 0's in a row	01011
Five 0's in a row	01010
Six 0's in a row	01001
Seven 0's in a row	01000
Eight 0's in a row	00