ARCHITECTURAL CONSIDERATIONS FOR A GENERIC MULTI-PORT DIGITAL INTERFACE

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INTRODUCTION

Telemetry system requirements are driven by technological developments in other areas, thus the capabilities of one are mirrored in the capabilities of the other. Contemporary systems typically involve two or more digital subsystems, each operating at a unique clock rate; an increase in complexity that needs to be addressed by the Telemetry system designer. Although the subsystems may be exchanging information, complete synchronization is seldom realized in discrete systems. Because the Telemetry system must provide information sufficient to isolate data/process corruption, it must accept data from the various subsytems at different rates and times. What is needed is a technique to de-couple the Telemetry system clock rate from that of the Subject system or any of its subsystems. This technique must bridge the gap between the synchronous data transmission fundamental to the Telemetry system and the asynchronous data transfer required by the various non integrated subsystems.

This paper will discuss the design challenges offered by such a Subject system for both real time and post flight analysis. It will discuss how the restrictions imposed by the IRIG standards and anticipated mission requirements factored into developing the architecture for a Generic Multi-Port Digital Telemetry Interface.

Most engineers would agree that given adequate resources, the majority of problems can be elegantly resolved. They might also agree that real projects or problems seldom come with completely adequate resources; that the elegant solution is the source of the job challenge and is usually the result of compromise. These fundamentals of engineering are especially true for the Telemetry system designer who is usually consulted after the main system level concepts have been determined and is tasked with insuring that total machine state is available for analysis.

There will be two terms used in this paper that had best be defined. These definitions are not intended to be complete as presented but merely to simplify the task of describing he basic system characteristics. First, synchronous data transfer is defined as a transaction which occurs on similar edges of a common clock, or in other words, the data has clock coherence. In such a system, the total data rates are well defined and critical timings are minimized. In asynchronous data transfer it is implicit that there is no common clock. To a certain extent, the data is always over-sampled in an asynchronous system. For instance, a UART or 1553 based system over-samples at the bit level to determine the word boundaries; in an asynchronous parallel interface, the control and data lines are perhaps de-bounced or delayed which can be considered as another form of over-sampling.

Before the machine architecture is discussed in detail, there are some problems unique to asynchronous sampling of digital data that should be addressed. One problem in over-sampling and stream mixing is spectral distortion of the data. For example if three data sources are formatted into a stream comprised of three contiguous data blocks, the data will be distorted in time when viewed with real time processing hardware. This distortion will be proportional to the relative data block sizes and the degree of over-sampling and basically is the result of compressing in time symmetrically sampled data. This effect is as more pronounced for super-commutated data. It can of course be removed by time correlating the data via computer with the performance penalty of non real-time processing. Thus, to insure compatibility with the various IRIG facilities and equipments, care should be taken to insure that the bandwidth of all parameters intended for real time spectral analysis be limited to accommodate this distortion. The alternative would be to distribute the data from the various streams as symmetrically as possible in the formatted stream which is of course a major architectural consideration; in any event some distortion is inevitable. The second problem is internal time correlation. Because all of the data is being processed asynchronously, some sort of frame tag is needed to characterize the relative frame skew of the various systems. This can be included in the respective data blocks by the source systems and used in post mission analysis. One last consideration in an over-sampled asynchronous system concerns the Main-frame/Sub-frame

organization as is defined by the IRIG document. This type of data format is not possible; the Subframe Identifier becomes irrelevant as a result of the frequency imbalances or possibly non-sequential due to the redundant data. Techniques using tagged data to extend frame depths must be used with great care to insure that all critical data is available from real time processing on IRIG compatible equipments.

The design goal s for this project were to develop a digital instrumentation interface that was sufficiently generic to facilitate use on various projects without major redesign or hardware modification. It was also desired that the basic design be modular to allow multiple data ports and permit parallel design tasks. For flexibility, discrete, parallel and serial ports were required. The familiar constraints of power, size and development time were of course major drivers. Lastly, it was desired that the final architecture support both synchronous and asynchronous operation without major hardware redesign or modification.

The subject system comprised two asynchronous digital sources and a block of analog parameters. One digital source required a burst mode parallel port with minimum access and word transfer times. The second digital source was a UART driven serial port that would transfer data continuously. The analog data block was comprised of single ended medium range measurements that included low bandwidth composite PAM data streams. The analog processing hardware will not be discussed further.

The Telemetry system that resulted uses attributes of both synchronous and asynchronous techniques to assure reliable data collection and transmission. One aspect of the machine performs synchronous data transfers from the host. It accepts the data on clock edges that are temporarily aligned by a sequencer. This alignment allows the data to be reliably stored and the response time of the interface to be characterized. It then over samples the data blocks via a double buffering technique to eliminate the over and under runs resultant from the frequency imbalances in the asynchronous systems. The data from the three sources is concatenated into three data blocks which form a Major frame. Each block is further divided into regions defined by fixed update boundaries. These regions contain current

information for that portion of the block and are updated as each system asynchronously transfers new data to the Telemetry Interface.

The serial port is divided into three boundaries while the Parallel port has one; therefore, for any given transmitted data frame, new data will occupy one region as is defined by these boundaries. The remaining regions will contain redundant data as a result of the over-sampling. The over-sampling represents the compromise inherent in this solution, in this case a reduction in the effective data bandwidth made available to the source system. All the word assignments in a data block are unique in a given Major frame and consistent in adjacent frames, thus, with the exception of the real time spectral distortion, all parameters are available for evaluation by standard IRIG equipments. As mentioned earlier, the frame skew characterization requires additional computer processing.

The final design required 23 standard DIP IC’s which comprised Electrically Programmable Logic Devices, 2k of Asynchronous Dual Port Static Ram, UART, discrete counters and differential receiver/transmitters. For this application, it was fabricated on one 3"x5" printed circuit card and required less than 1.8 Watts. Approximately 10% of the programmable capability has been left for future use. The time from concept development to working prototype was 5 months.

Three major technical drivers were factored into the architectural requirements. First, the final machine had to have the capability of handling multiple data ports that were de-coupled from the main system clock, i.e full synchronous operation. The main problem here was to insure reliable operation during the pseudorandom interruptions from the asynchronous sources. This had a dramatic impact on the sequencer design as minimum and maximum output cycle times were balanced with the cycle time for the respective ports. The second consideration was how to insure that all data transferred to the Telemetry interface received transmission. It was desired that this function be guaranteed by the interface hardware to eliminate any future questions for data integrity. The solution was a completely de-coupled sequencer that stored the write and read events and coordinated the buffer updates. As in the first

consideration, the cycle times, or machine map had to be balanced with the requirements of both sequencers. Lastly, it was desired to make provisions for synchronizing the output sequencers with one of the multiple data ports. Important considerations here were clock gereration, distribution and sequencer interaction. This resulted in, programmable initialization controls, clock paths and spare I/O. A major on impact on the sequencer design was to insure reliable operation in the asynchronous environment by eliminating metastable conditions in the EPLD’s. This was done by identifying critical asynchronous paths and insuring single state distances.

Architecturally, the machine is comprised of 2 basic sequencers that control the basic data formatting tasks for the composite data stream. Both sequencers are interlocked and have been designed to operate either from an internal oscillator as in the case of asynchronous operation or from an external clock as would be required in synchronous operation; this clock is used to derive the data rate of the telemetry link. Functionally. one sequencer determines correct word placement and serialization while the other decodes the mapping for the RAM. The criteria for decoding the RAM map is programmable and is central to the over-sampling and placement of the update boundaries. These two sequencers represent the synchronous/asynchronous boundary and are able to be de-coupled from the rest of the system clocks when operated in the asynchronous mode. The remaining sequencers are essentially custom designed to the requirements specific to the data part. The parallel Port uses a high speed burst mode and a generic 3 wire protocol. Typical word transfer rates are 600nS yet will vary as the respective clock edges are de-skewed. The basic sequencer operation debounces the control lines and coordinates the transfer of new data to the correct region of the RAM map. The state map also contains recovery paths for protocol failures. Once a complete region has been transferred, another de-coupled sequencer updates and arbitrates the output RAM pointers such that the region boundaries remain intact. This has the effect of insuring fixed data formats that are relatively insensitive to short term input data rates. Because the frame structure is hardwired in the EPLD's, compatibility with IRIG equipments is also assured. The serial port sequencer uses a discrete input to determine the occurrence of the first word in a data block. In this

application, the word depth of this port has been maximized for this particular system, thus, the source system can control the depth of a specific block in software by the assertion of the first word discrete. In each case, the data transfer is required to be sequential.

As was mentioned, the overall design is completely modular. This architecture is essential when providing completely de-coupled data parts to mutually asynchronous systems. The modular design permits stand-alone operation with only part or all of the ports operational. This modularity also permits the asynchronous multi-port concept to be expanded in proportion to the RAM resources and the long term external data rates. The use of a very generic protocol and the fact that the protocol is, by virtue of the ELPD’s itself programmable provides a device quite easy to modify for other requirements. The ability to operate in either an asynchronous mode on an internal clock or from an external clock, still de-coupled from the other data port removes the design compromise found in the over-sampling of the high speed parallel port.

INTERFACE SPECIFICS

TRANSMITTED DATA RATE	2.5 mBPS	8 bit Words	625 Words/Frame 500 Hz
TRANSMITTED DATA FORMAT	64 ANALOG , 40 SERIAL PORT	500 PARALLEL PORT	
UPDATE BOUNDARIES	ANALOG-NONE	SERIAL-3	PARALLEL-1
PARALLEL PORT INPUT RATE	600nS minimum / 8 bit Word		
PARALLEL PORT DATA FRAME	500 Words at 250 Hz		
SERIAL PORT INPUT RATE	50 Kbps @ 10 bit format		
SERIAL PORT DEPTH	PROGRAMMABLE LESS THAN OR EQUAL TO 40 Words		
SERIAL PORT FRAME RATE	125 Hz		