AIFTDS-8000 - A NEXT GENERATION PCM SYSTEM: CONCEPT THROUGH FINAL DESIGN

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ABSTRACT

Development of a next generation modular PCM system to satisfy a variety of applications for a decade or more resulted in a greater design effort than the use of the latest device technology to satisfy a current customer's functional needs. Functionality of the existing product line, as well as competitive products, was coupled with a survey of users' present and future needs, and their opinions of both the good and bad features of existing products. The survey covered system architecture, system throughput, signal conditioning, packaging, software, telemetry, recording and support. A phased development schedule implemented current customer requirements first, followed by development of ultimate system capabilities. Proof-of-concept prototyping proved extremely cost effective as significant changes and improvements in both mechanical and electrical designs resulted from the prototyping. Extensive internal design reviews permitted a wide range of engineering talent to contribute to the overall design. This major undertaking was started just over two years ago with mechanical prototyping and environmental testing of the new "Loaf-of-Bread" (LOB) packaging concept. The core system functionality, composed of 17 different types of functional modules, is now entering the production phase following full environmental qualification. Expanded system functionality is currently developed through proof-of-concept operational hardware which will be upgraded to production hardware within the year. The mechanical modularity achieved by the LOB package will permit system users to make low cost, periodic upgrades of key system functional elements by slice replacement without obsolescence of the majority of the users' delivered hardware.

INTRODUCTION

For decades the telemetry industry has primarily developed new products and systems under contracts to satisfy specific customer requirements and not under the broader guidelines used by commercial product developers. With the number of new-start military and commercial aircraft programs rapidly declining it was decided that the next generation of modular PCM systems could not just respond to the next major customer's needs and ignore the current and future needs of the rest of the user community. This decision was reinforced by new functional requirements of the first customer, which, if implemented as proposed, would have materially increased the size of the existing multiplexer box at a time when many users were saying the box was already too large for many current and almost all upcoming flight test applications.

These events caused a complete rethinking of not only classical packaging concepts but total system architecture and the procedures to be used for the development of the new system. A crash program was launched to investigate truly modular packaging concepts in parallel with an industry requirements survey. The results of this effort pointed to the need for a significant departure from the original design objectives envisioned at the start of the program. The user survey showed that not only reduced package size was essential, but the system throughput needed to be much greater than was originally believed necessary. A "Loaf-of-Bread" (LOB) package concept was developed which permitted doubling the channel capacity per cubic foot of aircraft volume and eliminating many of the restrictions imposed by fixed size boxes. A mechanical prototype was built and subjected to vibration and shock testing in order to verify viability of the new packaging concept and acceptability to the customer of the launch program.

In the area of signal conditioning, cost estimates of the new software controlled Programmable Presample Conditioner Unit (PPCU) led to the conclusion that all potential system users would not universally agree that a 100% software controlled data acquisition system was cost effective (or affordable). Thus, it was necessary to include in the overall system design provisions for existing hardwire programmable presample conditioners to supplement the software programmable units. It was also necessary to develop a more accurate cold junction compensation technique for processing thermocouples. The survey showed the need for increased accuracy over a narrower operating temperature range to satisfy wind tunnel and ground engine test applications. This, of course, expanded the system word length requirements to be able to process 16-bit

words as well as the classical 10-bit and 12-bit words used in most current flight test applications.

A CRITICAL LOOK AT EXISTING DESIGNS

The first task in developing the new system was to take a critical look at both the existing system architecture and at other manufacturers present designs and try to assess the good and bad points of those designs.

System Architecture - Without exception, all users considered it essential to have a distributed system architecture with a central controller and remote multiplexers and signal conditioners. System throughput was where the widest range of requirements was identified. Some current flight test programs such as the Canadair RJ program only identified needs of 20k to 40k wps as they still planned to use FM/FM for dynamic data channels. Agusta Helicopters in Italy was using 128k wps, as was Caterpillar in testing large earth moving equipment. For the LHX program, Sikorsky was planning to use multiple PCM streams and an aggregate data acquisition word rate of about 800k wps. The European fighter had specified throughputs of up to 400k sps as had Douglas for the MD-11/C-17A data acquisition systems. Rolls-Royce had identified needs for approximately 500k wps for a 2500-channel engine test system (steady state and transient data only) with over 1 M wps for a 5000-channel system for a new large engine. At the same time the US Navy on the F-14D program identified a need for 1.8M wps to acquire and merge data from eight 1553B data buses, pilot voice and other general parameters, plus data from a DMA channel between the radar and flight computers converted to eight 1.5M bps PCM streams (150k wps/stream). Just these few users generated a 90:1 ratio of throughput requirements for currently identified applications. Since the past 20 years has shown a steady and consistent increase in data acquisition system throughputs, it was clear that a system must be able to handle these currently identified requirements yet at the same time, by parallel system expansion, be able to have throughput capabilities significantly beyond these identified requirements.

Recent developments in tape recorders backed up these conclusions. Single track recorders from Datatape and Honeywell provide recording bit rates to 4.8M bps with 8mm cassette recorders, 8.0M bps with VHS recorders, 20M bps with S-VHS recorders, 100M bps with 14-inch reel-to-reel rotary head machines and up to 420M bps with the new MIL-STD-2179 cassette recorders. Ku-band telemetry would also support much wider bandwidth rf links than the present

L- and S-band links. At the same time, it appeared necessary to be able to divide high aggregate throughputs into multiple low bit rate PCM streams to permit existing 7-, 14-, 28- and 40-track longitudinal head recorders for onboard recording at low enough tape speeds to permit 1 to 3 hour recordings with only one pass through the recorder.

System channel capacity was another critical capability requiring evaluation. The existing AIFTDS-4000 system had a master/slave remote multiplexer capability. One master unit (functioning as a central controller) could control up to 44 slave Remote Multiplexer/Demultiplexer Units (RMDUs) with up to 352 analog inputs per RMDU. This permitted configuring a system with a total of 15,488 channels. Less than 1/5 of this capacity was ever used in a single system because it was orders of magnitude beyond the requirements for classical temperatures, pressures and positions for airframe certification. At the same time, however, Aerospatiale recently flew an A320 flight test with 120 ARINC 429 buses that generated over 30,000 measurands on one test aircraft. ARINC 429 data requires two or three PCM words to acquire one 32-bit measurand. Two PCM words are required to acquire a 16-bit MIL-STD-1553B bus data word while the data acquisition system concurrently samples 10-bit or 12-bit classical temperatures, pressures and positions. For large systems with many digital data buses, the PCM channel (word) addressing capability of 15,488 words did not seem totally adequate for the next generation of PCM system architecture. Thus, it was decided to double this capacity to 30,720 channels (or PCM word addresses) and change the product identifier from AIFTDS-4000 to AIFTDS-8000.

Signal Conditioning - The AIFTDS-4000 system had always permitted concurrent use of either integral signal conditioners and multiplexers packaged on pluggable PC cards installed in I/O card slots of a RMDU chassis or separate signal conditioner cards installed in 16- or 64-channel Presample Conditioner Units (PCUs) feeding 32-channel differential analog multiplexers in the RMDU. Signal conditioner complexity only permitted packaging from 4 to 12 channels per card. Thus, an RMDU chassis with 11 I/O card slots could only support from 44 to 132 channels. However, with the use of colocated 16- or 64-channel PCUs, one RMDU chassis with eleven 32-channel differential multiplexer cards could support up to 352 analog inputs. Thus, the decision to use integral or separate signal conditioners, or a combination thereof, was left to the system designer depending on the channel density of different types of sensors in each zone of the test aircraft requiring an RMDU. Without exception, this system capability was considered by users to be essential in future

systems. The AIFTDS-4000 signal conditioners went through their lost pluggable PC level upgrading in the mid-1980s. Therefore, it was decided to keep the 16-channel and 64-channel PCU packages as is, with the next upgrade to raise their operating temperature limits from +71°C to the +85°C operating limits of the new AIFTDS-8000 system. Other manufacturers also offered standalone or integral signal conditioning, so there was no significant difference in competitive products here except to consider the use of hybrids to materially reduce the signal conditioner's size.

Teledyne Microelectronics is currently the world's largest manufacturer of hybrids and produces hybrids that cover the product range from signal conditioners through computers to microwave rf devices. Thus, reducing the size of the PCM system through the use of hybrids could be easily accomplished in-house if the market demanded if. Here, however, most customers surveyed indicated they wanted to be able to repair the hardware themselves (or have in-country representatives be able to do the repairs in Europe or Asia) so they did not have to send modules back to the factory for repair. Of course, the higher cost of hybrids over discrete ICs entered into the picture and none of the users wanted to make the significant investment necessary to purchase an inventory of a large variety of spare hybrids to permit field repairs, unless it was necessary for their application. This sentiment even flowed over into the use of surface mount devices because, at this time, even that technology requires a significant capital investment by the user just to be able to replace devices.

From the standpoint of size it appeared that the primary flight test users who must have the much smaller multiplexer or signal conditioner size afforded by an all-hybrid system implementation were testing drones, RPVs or helicopter rotors. Rotor testing often required sampling 300 to 400 strain gauges with the complete PCM system on top of a rotor in an area typically less than 16 inches in diameter and 10 inches high, and coming off the rotor on slip rings with serial PCM. The market for microminiature hybridized systems did not appear large enough to justify the costs of concurrent development of both a microminiature hybridized system and its functionally equivalent larger discrete version.

Packaging - Packaging was the area where it was believed necessary to provide a significant improvement in the state-of-the-art. Modularity of PCM systems for decades was implemented with different boxes of different sizes for different types of signal conditioners and multiplexers. The survey showed a desire for modularity at the Line Replaceable Unit (LRU) level.

The AIFTDS-4000 system attempted to satisfy this need by offering a Short RMDU chassis with four I/O card slots and a Long RMDU chassis with eleven I/O card slots. Experience with this concept in package modularity indicated that most zones of a test aircraft either had too many channels for a Short RMDU (16 to 48) with integral signal conditioning, or just a few more channels than are possible with a Long RMDU with integral signal conditioning (44 to 132). The net result was that the user almost always required a Long RMDU box that only used 5 or 6 I/O card slots or it was necessary to install a second Long RMDU that still had only 1 or 2 I/O cards installed. Because of the high cost per channel of the short RMDU box (the chassis and power supply costs were a significant part of the whole RMDU chassis costs) very few customers opted for the short RMDU chassis over the years.

The principal cost drivers of the empty box were the eleven 66-pin center jack screw I/O connectors and the flex cables to route input signals from the connectors on the the front face of the box to the I/O side of the 150-pin backplane connector. As depicted in Figure 1, this chassis has 25 flex cables and over 3000 hand solder joints making, it a very labor intensive assembly. Flex cables, however, were essential to reducing the height of the box and in providing constant distributed capacities from I/O slot to I/O slot and chassis to chassis. To keep the connector face of the box as small as possible and still provide the 66 pins/connector required by a 32-channel differential multiplexer, only two types of I/O connectors could be used; either the Deutsch center jack screw rectangular connector or the Hughes Bullseye center jack screw round connector. The 4" high by 8" wide dimensions of the AIFTDS-4000 RMDU chassis thus were dictated by the need to accommodate eleven 66-pin Bullseye connectors plus a twelfth connector to bring thermocouple reference wires into the chassis. All available twistlock MS connectors providing the same pin capacity would have made the multiplexer box nearly three-fold larger.

In the beginning the Hughes connectors cost only about $60 a mated pair. Although their cost was higher than low cost “D” series connectors, they were still acceptable. However, over the years, because they were not multi-sourced, their cost rose to over $360 a mated pair. The best solution to these packaging problems was the LOB packaging concept where low cost “D” series Mil-Spec I/O connectors are attached directly to one side of the PC card with the 90-pin extendable backplane connector attached to the opposite side of the PC cards. This eliminated all costly flex cables and permitted mass soldering processes to replace hand soldering.

For years two U.S. PCM system suppliers had offered modular LOB system packages. They were recently joined in this area by a European PCM system supplier and a U.S. aircraft manufacturer with their in-house designed digital data acquisition system. One of the two U.S. suppliers producing an LOB PCM system package offered a microminiature design based on the exclusive use of hybrids, while the other used discrete devices in a larger LOB package. All of these system packages, however, have one or two principal drawbacks that were disliked by many system users.

The microminiature hybrid-based package was considered the best of the current LOB designs because it uses intermodule connectors to implement the backplane where each slice, added to an LRU assembly, physically extends the backplane. However, it uses four long bolts to hold the “loaf” together. Thus, for every different length of loaf a separate set of bolts is required for final assembly. The LOB package using discrete parts originally developed for NASA was larger but its mechanical assembly had the same problem. The more recent European supplier’s system and the U.S. aircraft manufacturer’s packages use conventional PC backplanes with the modules plugging into and fastened to the backplane with two through-module threaded rods to tie the LRU together on the surface opposite the backplane. Thus, these systems not only require a large inventory of variable length bolts or threaded rods but they also require a large inventory of different lengths of backplanes for full modular flexibility at the LRU level. The European system supplier currently only offers 11-slot and 15-slot backplanes as standard and the system developed in-house by the U.S. aircraft manufacturer is not yet used by other aircraft manufacturers and to date is not being marketed commercially.

The U.S. aircraft manufacturer’s discrete component LOB and the hybridized LOB packages, both with slices less than 0.5 inches thick, require the use of subminiature D-series connectors for both the I/O and backplane connectors. These small I/O connectors require the use of 26 gauge signal wires. This, of course, is one of the principal problems users of the microminiature hybridized system complain about.

Without exception, no user wanted to have to use delicate 26 gauge wires from the sensors to the data acquisition units unless there was no other alternative. They also questioned the reliability of the subminiature connectors as compared to the MS connectors that accept 22 gauge wire. Some users, such as Boeing, Douglas and Rolls-Royce, preferred to use 20 gauge sensor cables to provide even greater cable reliability.

Finally, there was the problem of not having captive hardware in the assembly of the LRUs. This, of course, is not possible with the threaded rod or through bolt method of securing the slices of a loaf together longitudinally.

Thus, achieving a modular LRU package concept dictated an integral through-slice backplane connector so that separate PC backplanes of different lengths are not required, as is the case in two of the existing system designs. The slice-to-slice attachment hardware had to be captive and at the same time compress the interslice O-ring required for unit sealing during the engagement process. Finally, the endplate used at one end of the loaf and the power supply at the opposite end of the loaf, where the LOB assembly was bolted to the aircraft structure, also had to be able to be provided with conventional mounting holes or with captive hold-down bolts if desired by the user.

Software - Most PCM system suppliers do not presently emphasize software as an important part of the product. Until now this has not been too important as usually only one data cycle map was stored in onboard EPROM or EEPROM memories and many ground stations could not accept changes in the data cycle map size from program to program much less from flight-to-flight or during a flight. Recently developed ground stations, however, have more flexible hardware and software which permit multiple test scenarios to be prestored and selected dynamically for realtime data processing. Because of this ground station capability all recent PCM system requirements have specified storage of multiple PCM maps selectable during a test. Also, the larger number of channels being used in newer systems make the laborious process of manually programming data cycle maps into EPROMs or EEPROMs highly undesirable. Thus, software is now an important integral element of a new data acquisition system.

The programming problem is significantly increased with the advent of software Programmable Presample Conditioner Units (PPCUs). Each presample filtered channel has a gain, offset and knee frequency to select, in addition to the gain and offset programmed for each sample in the common GPA used in the multiplexer unit following the PPCU.

For the past few years the AIFTDS-4000 system has been supported by a multiplexer compiler which converts the ASCII string defining the characteristics of each time slot in a data cycle map into the object code to be loaded into the sampling format memory of the airborne data system. This compiler must now

be expanded to incorporate PPCUs which get downloaded from the PCM Central Controller (PCM-CC) Unit before a test flight.

Finally, most new data systems require realtime calculations of critical flight test data with the EU results displayed to the test pilot or onboard test engineer in realtime. The EU data must also be inserted in the telemetry stream for realtime observation on the ground plus being tape recorded onboard to provide a record of what the test pilot or test engineer actually saw during the flight. These requirements expand the functions and complexity of the airborne software to the point that it is not something the flight test engineer does in his spare time. The complexity and details of this software are too extensive for this paper and will be covered separately.

Built-in-Test - The ever increasing complexity of the airborne PCM system has brought a new meaning to Built-in-Test (BIT) which has, heretofore, been primarily restricted to complex military avionics packages. This problem is exacerbated by the need to install the LRUs in places such as wing and tail surface leading and trailing edges and crowded avionics boys where access during the test program by instrumentation engineers is difficult and time consuming, if not impossible.

The AIFTDS-4000 system had offered built-in calibration channels in all RMDUs functioning as BIT channels that could be programmed into a data cycle map for realtime diagnostic purposes. Individually addressable BIT channels previously included a power supply secondary output voltages test bit, high level calibration of the analog-to-digital converter, measurement of the offset of the common GPA at different gains and a precision low level to high level calibration channel on each 32-channel differential multiplexer module. Also, there was the classical R-Cal and/or Z-Cal of bridge type sensors to determine sensor health.

This comprehensive built-in-test capability has been expanded in the new system to include a shorted input to the A/D converter to permit separating end-to-end gain and offset errors between the common GPA and the ADC.

To permit in situ LRU testing in the aircraft a bus terminator module has been included as a part of the LOB endplate so that test equipment can be connected to the backplane during operation while the LRU is still installed in the aircraft.

The PPCUs can have their setup programs downloaded, inspected and changed from a single download/test connector using the same full duplex

communications bus used for data acquisition. The unique mode select word in the address structure permits both PPCUs and RMDUs to reside on the same party line bus so that only one set of bus cables need be routed to and through any zone of the aircraft. This also permits programmable I/O modules such GS a 1553B bus listener module in an RMDU to be downloaded and tested without physical access in the same manner as PPCUs.

CHANGES FROM CONCEPT TO FINAL DESIGN

There were many significant changes made in various areas of the system between the proposed concepts and the final mechanical and electrical designs. Some were architectural, others were driven by throughput requirements, while others were necessary to meet accuracy and environmental requirements. We will touch upon the highlights and tradeoffs in these key areas of the design.

System Bus Architecture - The original system bus architecture was established by the first user. It is a distributed star configuration with a PCM Central Controller (PCM-CC) acquiring data from up to 32 RMDUs and producing from 1 to 6 PCM streams with an IEEE-488 DMA interface to smart graphics terminals. As depicted in Figure 2, it supports up to eight communications buses and requires fiber optical communications between the PCM-CC and a Multiplexer Adapter Unit (MAU) that demultiplexes channel addresses and multiplexes returned data words from up to four RMDUs connected to the MAU by copper cables. Each bus is limited to the 125k wps throughput limit of the AIFTDS-4000 RMDU which must be able to be used concurrently with the new AIFTDS-8000 LOB RMDUs.

The original PCM-CC, designed by the first system user, has an aggregate throughput limit of 400k wps and requires round-robin demultiplexing of acquired data to generate from two to six slower PCM streams for onboard tape recording. It was packaged on 1/2 height VME cards installed in a VME card cage, eliminating the possibility of its use in a small aircraft with severe environments. This PCM-CC and the MAU being built to print for their application and were offered to Teledyne for use under license as a part of the AIFTDS-8000 system architecture. This capability, although a large improvement over previous system controllers, was not selected by Teledyne because it fell far short of some of the identified market applications.

The AIFTDS-8000 PCM-CC is modular and packaged using the same LOB hardware used by the RMDUs and PPCUs. It supports up to eight input or data acquisition ports and up to eight data output ports. The data input ports are designed as single RMDU buses, or, with a wider sampling format memory, they are multi-drop party-line buses. In the party-line bus configuration the PPCU filter characteristics can be downloaded and tested offline via the same bus that is used for full duplex communications to the RMDUs. During on-line operations the PPCUs do not accept addresses or output data on the bus. The multi-drop, party-line bus concept eliminates the cost of the MAU. The optional Electro-Optical Converter (EOC) modules are separate slices added to the LOB assemblies at both the PCM-CC and the RMDU and PPCU. Thus fiber optical buses are optional on a bus-by-bus case when needed either for high common mode voltage levels between zones of the aircraft and/or when the communication word rate or bus physical length cannot be satisfied with lower cost copper cables.

Synchronization signals between two PCM-CCs will permit synchronized master/slave controller operation to expand the number of input ports (party-line buses), the number of output ports and/or the aggregate system throughput.

PCM Central Controller - The PCM Central Controller (PCM-CC) design is still evolving even though proof-of-concept prototypes have been built and tested. The principal changes in design direction have resulted in the decision to produce two different versions of the PCM-CC to satisfy the wide range of market requirements. This is essential, so as to have a lower cost version for the less demanding system requirements with a higher performance, higher cost version for the most demanding requirements. Here again, the LOB package permits the PCM-CC to be developed in a phased manner so that functional capability can be upgraded without changing the entire concept and upgraded I/O modules may be used with different types of overhead modules. With the use of a Bus Terminator/Isolation slice, a small PCM-CC can be physically attached to an RMDU to produce a single LRU standalone PCM system.

The basic PCM-CC architecture is composed of three different overhead modules; (1) The Master Memory/Timing module, (2) The Controller module and, (3) The RMDU/ PCM-CC Power Supply Assembly. To this group of overhead modules may be added from one to eight data input modules and from one to eight data output modules. All versions of the PCM-CC use the

seven basic types of modules, but different dash numbers of the modules will provide the two basic subsystem performance capabilities.

The principal difference between the lower performance PCM-CC and its higher performance counterpart is limited to the number of I/O modules supported concurrently, the sampling format memory size and the aggregate throughput. Figure 3 is a functional block diagram of the higher performance, fully expanded PCM-CC.

The low-end PCM-CC supports up to four single RMDU communication buses as data inputs with up to five PCM encoder or other types of output modules. It is provided with 8k words of sampling format memory that can be configured as four 2k word blocks or two 4k word blocks to store larger data cycle maps. This PCM-CC has an aggregate throughput of 500k wps for 10- and 12-bit words and 250k wps for 16-bit words. It operates as a synchronous system generating 10-bit, 12-bit or 16-bit PCM words with or without parity and with four RMDUs will acquire data from up to 1920 differential analog inputs. It is provided with a master/slave capability where two PCM-CCs can operate from the same clock and double the number of I/O ports and the aggregate system throughput (i.e., support eight RMDUs' and output up to ten PCM streams with an aggregate throughput of 1M wps for 10- and 12-bit words and 500k wps for 16-bit words).

The high-end PCM-CC supports up to eight data input ports and up to eight data output ports. The RMDU communication buses are multi-drop party-line buses and the aggregate throughput is up to 1 M wps. With a single PCM-CC it, too, has master/slave synchronized capability supporting up to 16 input ports and 16 output ports. This enhanced system capability is depicted in Figure 4.

The principal data input module of the PCM-CC is the RMDU Communications Module (RCM). This module can be used with either the Memory/Timing Module (MTM) using the 32-bit wide format memory which supports a single RMDU bus with up to 4 buses per PCM-CC or the MTM with the 40-bit wide format memory which supports up to 8 inputs buses and up to 8 RMDUs and 8 PPCUs per bus. The MTM for the high performance PCM-CC is provided with either 32k words or 128k words of sampling format memory and the memory is contiguous for multiple map storage, as compared to fixed size memory block. This MTM provides the system with a 30,720 channel data acquisition capability based on fifteen 32-channel low level multiplexer slices/RMDU.

The PCM Encoder Output Modules (PEOs) for the high performance PCM-CC provide a programmable 256:1 bit rate ratio between output ports. The lower performance PEOs only generate a 64:1 programmable bit rate ratio between ports. A computer controlled PEO generates the extremely low bit rate PCM stream required by crash recorders. Either type of PEO can be used with either type of MTM.

The parallel bus architecture of the PCM-CC permits the use of other types of I/O modules than the basic RCM input module and the PEO output module. Other planned modules include a PCM Decommutator Input Module (PDI). The PDI will permit acquiring and merging of data from multiple PCM encoders to generate a single PCM stream for telemetry and/or recording on one of the new high bit rate rotary head recorders. The PDI(s), of course, can be mixed with the RCMs as inputs to merge data from AIFTDS RMDUs with data from other PCM systems. Other types of planned output modules include a 1553B RT module, an RS-422 (or -232) module or a Host Computer DMA module.

All PCM-CCs use three internal data buses: an Address Bus, a Data Bus and a Delayed Data Bus. The delayed data bus permits overhead words, such as frame synchronization patterns, subframe ID words and other overhead data, to be sent directly from Format memory to any or all of the output modules under program control. The delayed data bus is the path used to place computed results output by the Floating Point Computer module (FPC) onto the delayed data bus for insertion into any of the output data streams. The FPC can be used as one of the output modules in either the low-end or high-end PCM-CC. The FPC also has a DUART which provides two alternative methods of routing computed data to other display devices onboard the test aircraft. A functional block diagram of the FPC is presented in Figure 5.

Mechanical Package - The mechanical package concept proved to be the most important element of the system design. The Loaf-of-Bread (LOB) package concept was described mechanically in a paper presented in 1988[1] at the start of the design and it will not be repeated here. As with other elements of the system design, there were many changes and improvements in the LOB package design between the concept and the final design.

[1]"Software Control of a High Speed Modular Signal Conditioner and PCM System" ITC Proceedings, 1988, page 703

The principle package refinement at the slice level was the development of a casting with a high percentage of side wall and base overlap when mated to the casting of an adjacent slice. Another refinement was the A1 to A2 card spacing, which was selected to permit either of the two I/O connectors to be connected to either PC card, or one to each PC card. The intercard spacing also permits the IC devices to be located between the cards so that the back surfaces of both PC cards are available for testing when the slice is assembled.

Thermal analyses prepared during the design showed that power dissipation should be limited to less than 1.5 watts per module to safely meet the +85°C operational temperature requirement. Multi-layer PC cards were designed to permit Vcc power (+5V, and ±15V if used) and ground distribution to be implemented as copper layers instead of just traces for power distribution. The use of a significant amount of copper gives each PC a lower resistance path for heat transfer from the devices to the six casting attach points and thus to the aluminum frame. This also considerably reduces trace to trace capacitive coupling, as the power planes function as shields within the PC. A thermal layout of the PCs was used in place of a logical layout, with the hottest parts located closest to the edges of the cards and the coolest devices located in the center of the cards to normalize thermal gradients across the cards. A metal-core board is used for the one board whose total dissipation could not be kept below 1.5 watts by device selection. This package concept has demonstrated operability at temperatures up to +117°C. Figure 6 is a photograph of a 2-channel Programmable Presample Filter slice depicting how the daughterboard attaches to the motherboard, which in turn attaches to the slice casting with six machine screws.

The interslice attach pins are fabricated as two piece assemblies to reduce manufacturing cost while maintaining the required precision dimensions between the tapers at the base and at the head of the pin that draws the slices together when screwed into the steel fittings pressed into the top and bottom of the aluminum casting. Roll pins pressed into the casting bosses with shoulders on the taper pins preclude a pin from being removed too far and having the threads on the pin hamper the slice separation. The roll pins, of course, can be removed to replace a damaged or worn stainless steel taper pin assembly. On full insertion of the pins into the steel fittings of the adjacent casting, the interslice's electrically conductive O-ring compresses a minimum of 0.015 inches to provide a slice-to-slice seal.

Slot recesses were cast into the outside surface of each side of the base of the slice casting. This permits right-angle prying tools to be inserted between slices when the LRU is installed on its mounting surface. This permits easy separation of the slices when an LOB assembly is installed within 1/2 inch of a bulkhead in the aircraft and the loaf cannot be gripped by hand for separation of the backplane connector.

A bus isolation slice permits backplanes of different functional LRUs, such as an RMDU and a PCM-CC, or a Time Code Generator to be assembled as a single LRU. Bus isolation is achieved by cutting off all pins on the backplane connector of the isolation slices, except the power and ground pins, after the connector is soldered to the PC card and before installation of the pin shield. The isolation slice PC board permits termination of that functional subassembly's backplane, as well as bringing all functional pins to the two 44-pin test connectors on the slice so test equipment can monitor backplane operation without disassembling the loaf.

The carrying handle that originally was to be integral to the endplate costing has been made an optional feature. To make the handle protrude far enough to be gripped by large hands would make it extend 1.5 inches beyond the endplate. This, of course, would restrict the allowable length of the loaf by 2 slices in tight installation locations in the aircraft.

The use of either single or double density MS I/O connectors in either or both I/O locations on the slice casting provides from 25-pin to 88-pin I/O and/or test capability on a single slice. An external flat backplane assembly consisting of a shielded PC Card terminated in two floating I/O mating connectors provides a capability for an external private backplane between slices in complex dual-slice functional modules such as the Time Code Generator (TCG) or the Floating Point Computer Module (FPC).

Software Programmable Presample Filters - The software Programmable Presample Filters (PPSFs) presented the most difficult electrical design requirement because the low cost, mask programmable switching capacitor IC filters originally proposed proved to have too much offset drift across temperature to meet the tight accuracy requirements. Thus, this design had to be implemented using the classical multi-pole RC feedback type of filter with software selectable networks to implement the seven single octave knee frequencies between 10 Hz and 640 Hz.

Spare switches on the R-Cal switch device permitted the addition of a Z-Cal capability that is invaluable in measuring offsets. The large number of components to implement an instrumentation amplifier with eleven gains and seven offsets plus the seven knees, all under software control, only permitted two channels to be packaged on a single slice.

A microprocessor-based download overhead module is required to store in local non-volatile memory the gain, offset, and knee configurations of each of up to thirty-two channels (16 PPSF slices) in a PPCU. A power-on interrupt causes automatic downloading of each filter's characteristics from the overhead module to each PPSF channel.

Test data on the PPSF shows it meets its stringent accuracy requirements across an operating temperature of -55°C to +117°C, which is well beyond the +85°C requirement.

Wiring of the PPSF input stage is configured so that sensor excitation can be brought through the PPCU backplane to each slice or brought in through the module ID/test connector on top of the slice, providing each channel with a 6-wire input configuration. Filtered outputs are routed from each of up to 16 PPSF slices in an LRU to the backplane and output through the connectors on the bus termination module for connection via two cables to a 32-channel analog multiplexer in an RMDU. Both filtered and unfiltered outputs of each 2-channel assembly are also brought to the module ID/test connector on the top of the slice.

Remote Multiplexer/Demultiplexer Unit - The Remote Multiplexer/Demultiplexer Unit (RMDU) is composed of two or three overhead modules coupled to a number of I/O modules which is architecturally the same as the AIFTDS-4000 RMDU. The LOB package, however, permits a single LRU to have up to 15 I/O modules (the logical capability of both RMDUs) whereas the AIFTDS-4000 RMDU was limited to eleven or less modules by the fixed box size. The 15 module capacity is even possible with multi-slice modules, such as the 1553B Mux Bus Listener, because each module only uses one of the fifteen I/O logical addresses. Figure 7 is a photograph of three small RMDU configurations.

The Bus Interface Controller Module (BIC-M) for the RMDUs has been designed for 250k wps and 500k wps throughput (two dash numbers to the same assembly with different cost) so the individual or party-line serial bus data acquisition rate is not restricted to the 125k wps data acquisition rate of the

AIFTDS-4000 RMDU. The communications protocol is programmable to permit the use of 10-, 12- or 16-bit words in the RMDU. Although a given bus can operate to 500k wps, the PCM-CC throughput is limited to 1M wps by the speed of current advanced CMOS devices.

By having module select implemented via jumpers on an I/O connector as opposed to using dedicated module select lines in the backplane wiring, any I/O or overhead module can be located anywhere in the loaf. This should provide more flexibility in LRU assembly and in wiring the aircraft. The only module location restriction is that the power supply must be located at one end of the loaf and a bus terminator module must be located at the other end of the loaf. Module select via jumpers on one of the slice I/O connectors permits addressing to be changed without removing a slice so that “spare” slices can be included in the loaf at the time of LRU installation and addressed when required by adding/changing the logical address connector. It also permits visual verification of the logical number of the I/O module without disassembly of the LRU.

All of the Classical I/O functional modules were implemented including: a 32-channel differential Analog Multiplexer (AMX), a 48-channel Discrete Multiplexer (DMX), a 16-channel DC Bridge Multiplexer (DCB), a 4-channel Synchro/ Resolver to Digital Converter (S/RDC), a 4-channel Linear/Variable Displacement Transducer to Digital Converter (LVDT), a 4-channel ARINC 429 Bus Listener, a 4-channel Serial Digital Transducer (SDT) and a MIL-STD-1553B Mux Bus Listener. The only functional modules not yet carried forward from the AIFTDS-4000 RMDU I/O complement are the 16-channel Parallel Sample and Hold Multiplexer (PSH), and the 4-channel hardwire programmable Presample Filter/Multiplexer (PSF). These will be implemented in the near future.

The major technical advance in RMDU I/O modules was the development of a 4-channel multi-purpose Frequency to Digital Converter Module (FDC) which can perform any of three different pulse rate signal conditioning functions on a channel by channel basis. The new FDC thus replaces three classical pulse rate conditioner modules: the Frequency Counter, the Period Counter and the Pulse Totalizer. This was achieved by having a high speed microprocessor perform all three functions on all four inputs concurrently and buffer the results in RAM for sampling by the appropriate channel address. This module can accept inputs from either 5mV to 250mV or from 20mV to 100V at pulse rates from 0.1 Hz to 1.0 MHz. Each 20-bit data sample is output as two 10-bit PCM words giving the

pulse totalizer a 1,084,576 count full scale rollover period. The maximum input pulse rate of 1.0 MHz is also significantly greater than the output of any current pulse rate generator sensors. A functional block diagram of the FDC module is presented in Figure 8.

The fifteen I/O module capacity of a single RMDU produces a channel capacity of from a minimum of 60 channels using all 4-channel integrated signal conditioner modules to a maximum of 480 differential analog inputs or 720 discrete inputs. One RMDU with a 1553B mux bus listener can extract up to 2k bus words as 4k PCM words in addition to the up to 448 inputs from the other 14 I/O modules which could be configured as a single LRU. The dual-ported RAM buffer memory on the bus listener is 8k words by 20 bits. Therefore, by restricting the total number of I/O modules (including the 1553B bus listener) to either 7 or 4 modules, the one or two unused I/O module address bits can be used to increase the number of different bus words sampled from a single bus from 2k words to 4k words (8k PCM words) or 8k words (16k PCM words), respectively, in addition to the inputs from the other 6 or 3 I/O modules.

Accuracy - A 16-bit Analog Data Processor Module (ADP-M) has been built as a proof-of-concept demonstrator that shows that the RMDU can be used to achieve better than 0.08% accuracy across a narrow 10°C temperature range with low level inputs and a GPA gain of 1024 (excluding wild points) and can achieve accuracies exceeding 0.005% using a presample filter across the same temperature range (again, excluding wild points). The true noise within these limits was random and bipolar, so that oversampling of steady state data in the test aircraft and then averaging samples in the ground computer (which also throws out the wild points) permits one to achieve better than 0.001% accuracy. These proof-of-concept demonstration data were taken at a sample rate of 50k sps.

The normal 12-bit ADP-M has a guaranteed accuracy of better than 0.5% across the operating temperature range of -55°C to +85°C. It has not yet been evaluated across the narrower temperature range with which the 16-bit ADP-M has been tested. It is believed that the much better than expected accuracy achieved by the 16-bit ADP-M has been largely possible due to the superior module shielding offered by the LOB package and the fact that this package concept is less susceptible to the pickup of noise within the package.

The 16-bit ADP-M accuracy tests were conducted with 6 ft of unshielded twisted wire in series with 10 ft of TSJP cable driven by a low impedance precision

millivolt source simulating a thermocouple connected to a Thermocouple Compensator Assembly. Thus, it was not the classical unrealistic accuracy test with the signal input shorted at the input connector or the signal injected directly at the low level multiplexer input. In fact, it is estimated that these proof-of-concept accuracies in the measurement of steady state data can actually be improved by using a 15 Hz as opposed to a 150 Hz first order passive filter which is built into each low level multiplexer and selecting recently available MOS-FET gates which have 100 ohm “on” resistance and 150 nanosecond transit times to replace the 1500 ohm “on” resistance, one microsecond transit time switches used in the demonstration system. Along with these better devices, there is now available a 16-bit ADC with twice as good linearity (0.0015% versus 0.003%), three times better total harmonic distortion (0.001% versus 0.003%) and a better power supply noise rejection ratio of 84 dB.

Thermocouple Compensator Assembly - A dramatically improved Thermocouple Compensator Assembly (TCA) was developed in conjunction with the 16-bit ADP-M to be used for processing thermocouple inputs. The TCA is a passive, basemetal to copper conversion device that measures the unwanted junction temperatures in the TCA with a reference measurement channel using very linear, temperature sensitive, resistive type sensors. The TCA uses two sensors to measure the temperature of critical pins in the input connector where the unwanted junctions are created by crimping the thermocouple basemetal wire to the copper pins of the input connector. One of the key requirements in achieving high accuracy in measuring unwanted junction temperatures in the TCA is in tightly wrapping the first six inches of TC cable extending from the input connector with aluminum foil tape. The tight wrapping brings all TC cables in contact with each other to homogenize the temperature of the cable assembly before it reaches the input connector. The surface of the foil tape reflects heat radiated from the warmer TC cables to aid in homogenizing the cable bundle so that all unwanted junctions are the same temperature.

Three inch long thermal antennae of 22 gauge bare copper wires connected to the temperature sensor pins of the input connector permits them to better measure the input cable assembly and unwanted junction temperatures. Finally, the TCA is placed inside an isothermal sleeve that produces a greater than 5-minute thermal delay between any temperature changes applied to any portion of the outside of the isothermal jacket and the TCA itself. The proof-of-concept TCA installed in the isothermal cover demonstrated a 10-minute thermal delay when the assembly was placed inside an oven and the ambient temperature

was raised in a few minutes from +25°C to +60°C. An illustration of the TCA and its thermal jacket is presented in Figure 9.

CONCLUSIONS

Development of a completely new modular PCM system composed of nineteen different types of functional modules proved to be a much larger development effort than originally estimated. The successful design of the Loaf-of-Bread package concept eliminating the classical fixed size box was one of the most demanding of the design tasks. It was only possible by building and testing proof-of-concept models. This iterative process started with environmental testing of mechanical and electrical mockups of the package at the beginning of the program. These tests verified the electrical integrity of a variable length computer backplane, as well as isolating the best techniques for interslice assembly using captive hardware. Thermally driven PC layouts using multi-layer PC boards with copper planes for power distribution and heat transfer were essential in conservatively achieving the high-end operating temperature of +85°C with a significant margin of safety.

The LOB modularity applied to the PCM-CC design has permitted two different sets of overhead modules to be used with different quantities and types of input and output modules to produce a wide range of system capabilities, with correlative variations in cost. The use of isolation slices permits small LRUs with different functional backplanes to be integrated into a single assembly, resulting in lower costs and a smaller size IRU than can be achieved with separate assemblies interconnected by cables.

The LOB package permits achieving more than two times the channel density per cubic foot of installation volume than was achievable with the older fixed size box with pluggable PC card modules. The LOB concept has achieved lower production hardware costs with less noise susceptibility and greater accuracy than has been achievable with classical fixed box designs. Phased development of the modular design has permitted meeting initial customer requirements first with expanded system capability following core system availability. Development and testing of proof-of-concept versions prior to production releases has proven very cost effective as the best design is never the first design.

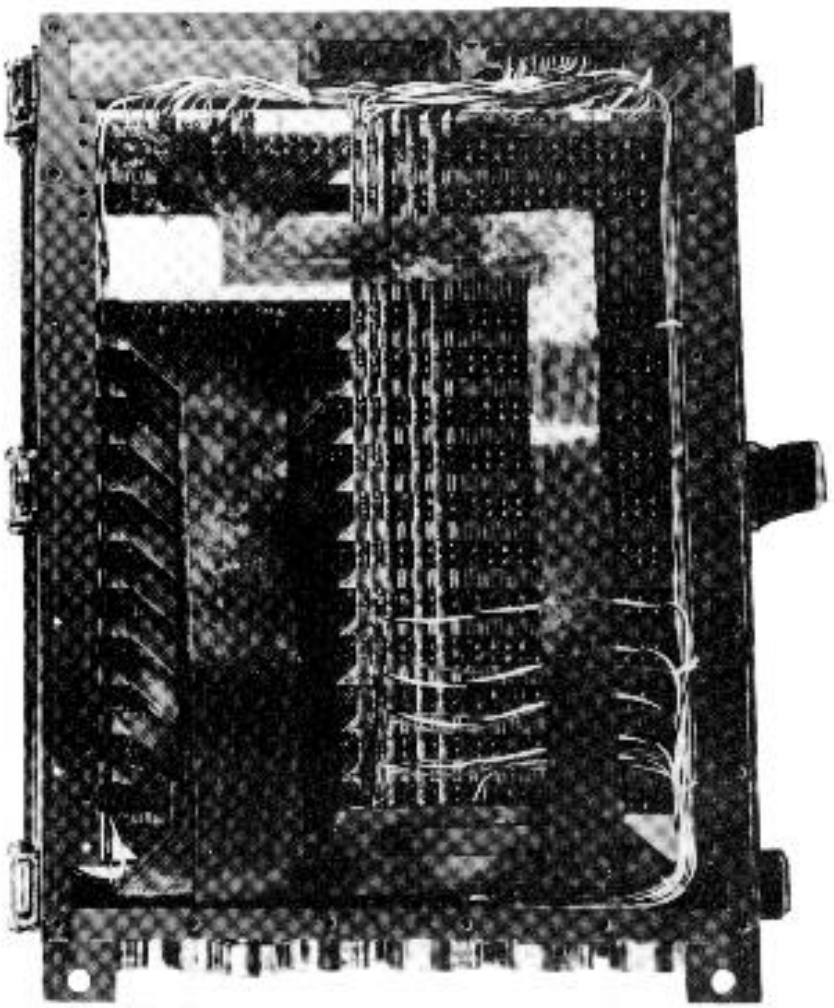

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Figure 1. AIFTDS-4000 RMDU Chassis

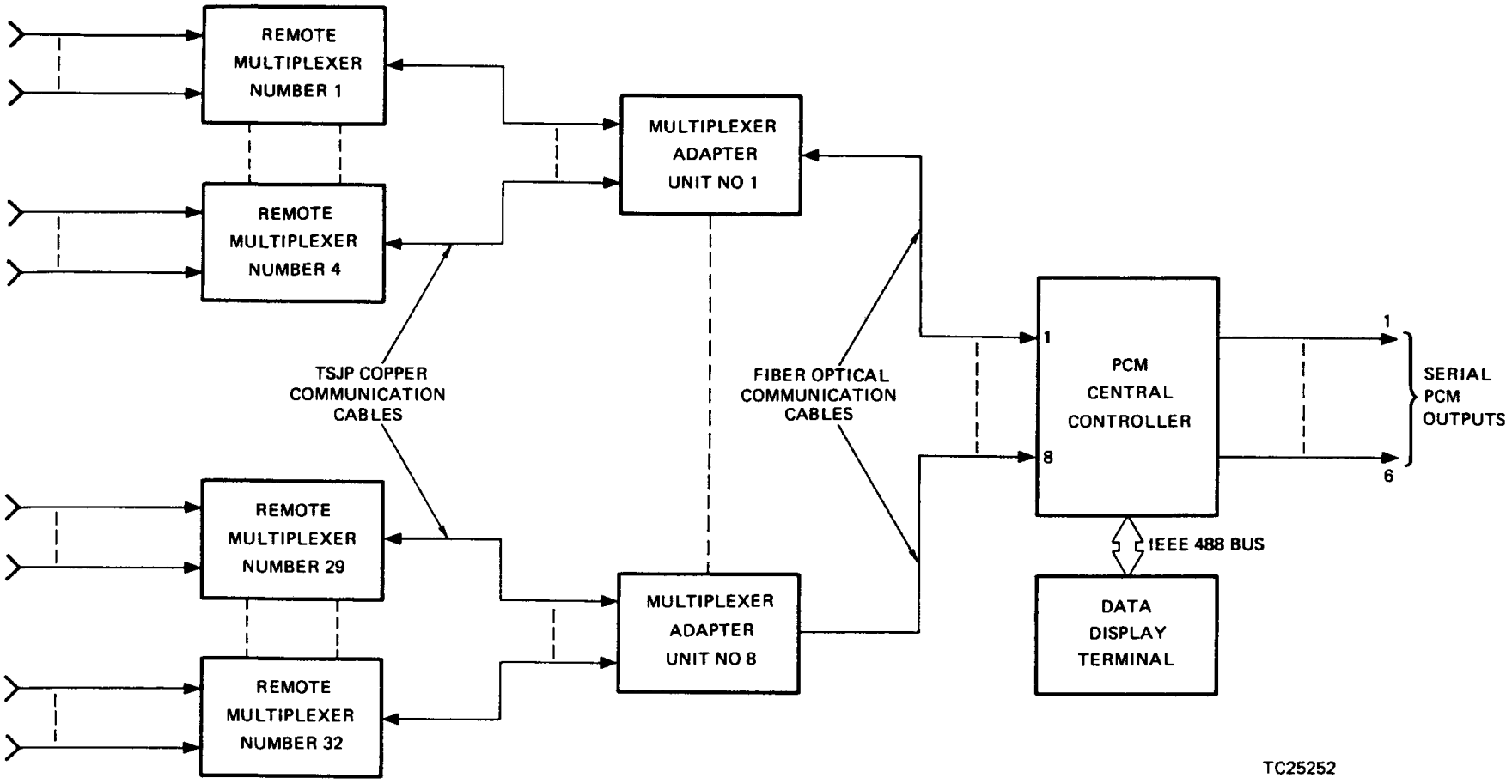

Figure 2. System Configuration Supported by Users' PCM-CC Design

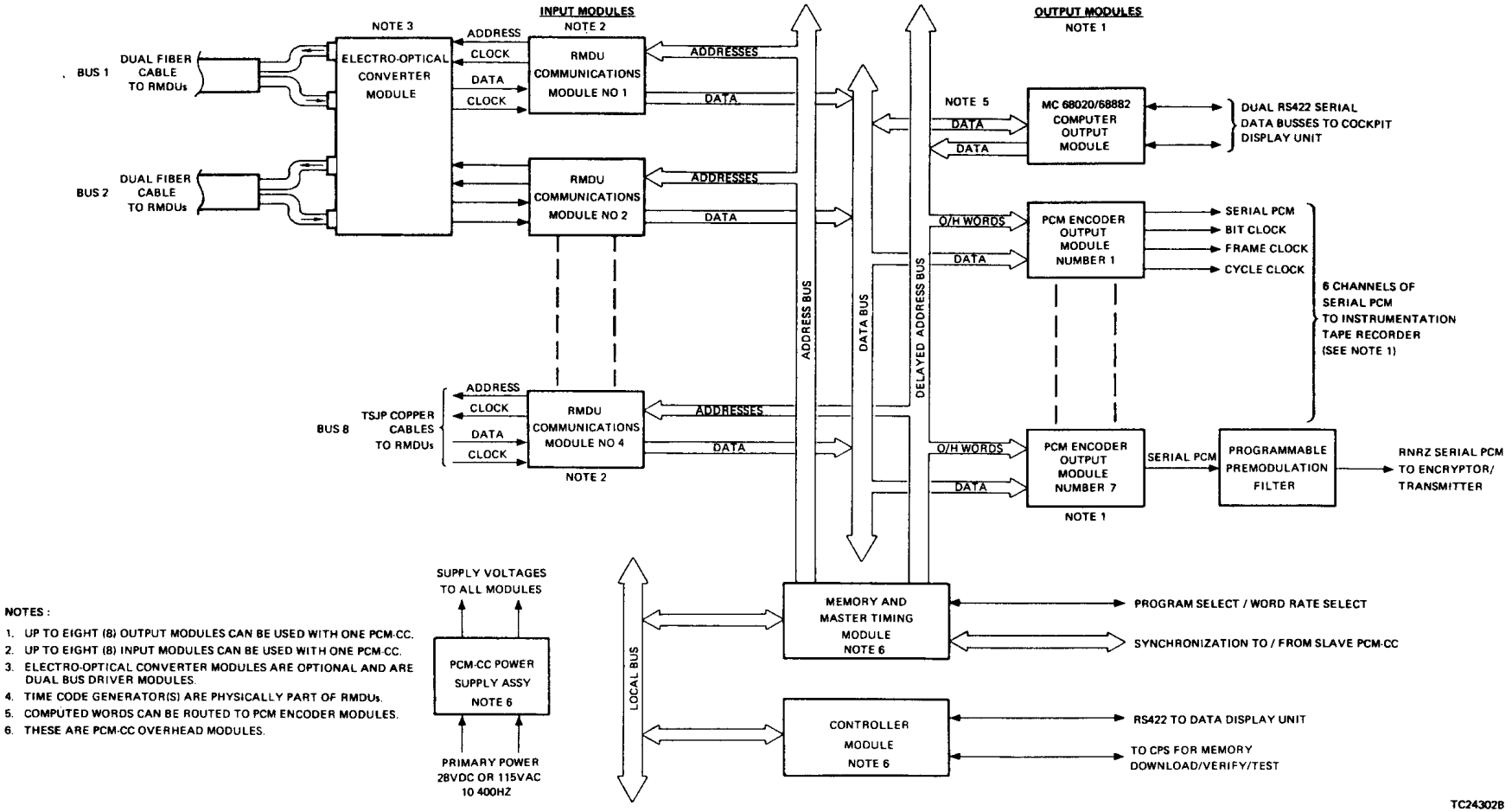

Figure 3. PCM Central Controller Final Design

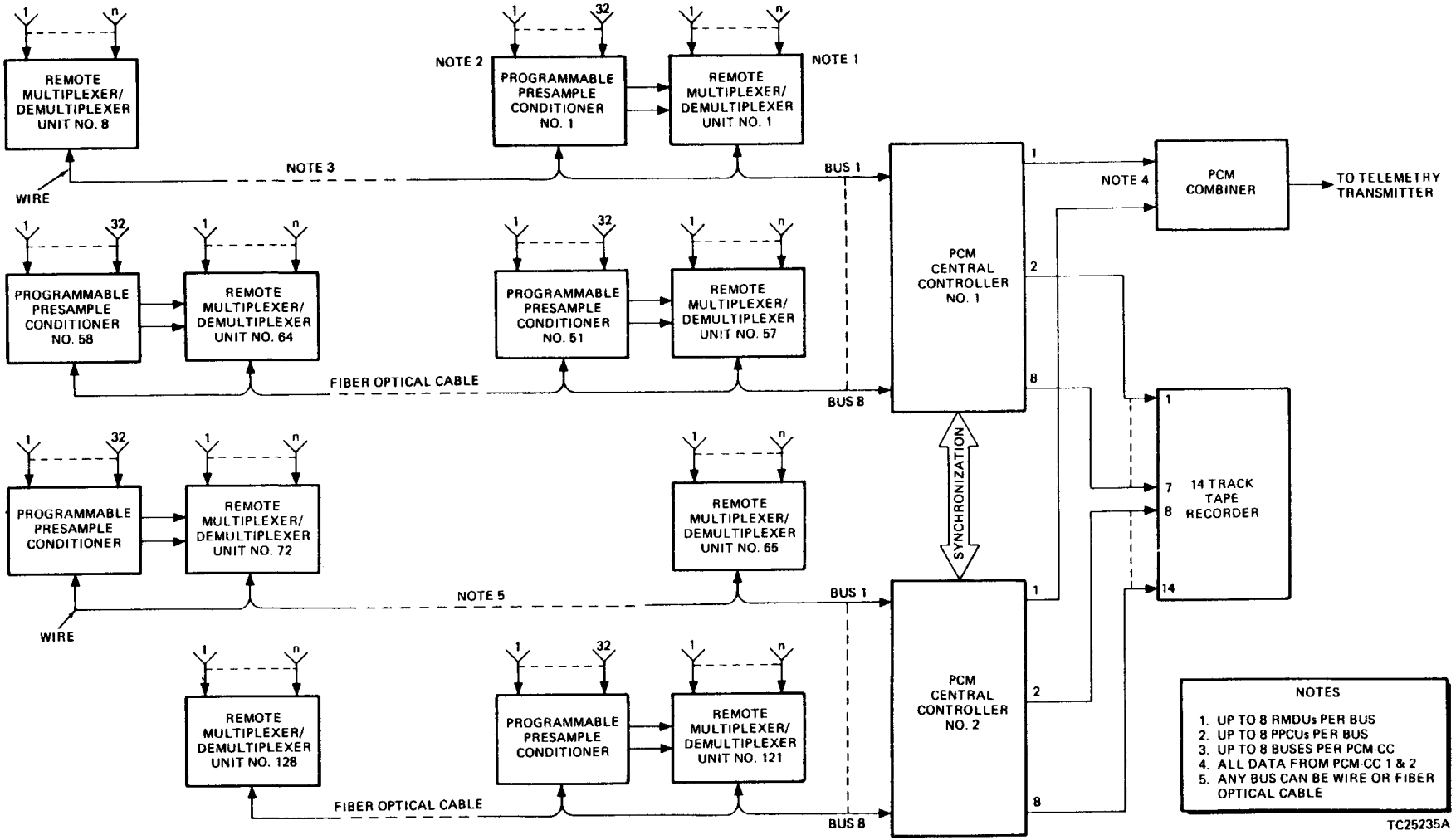

Figure 4. System Configuration Supported by Final PCM-CC Design

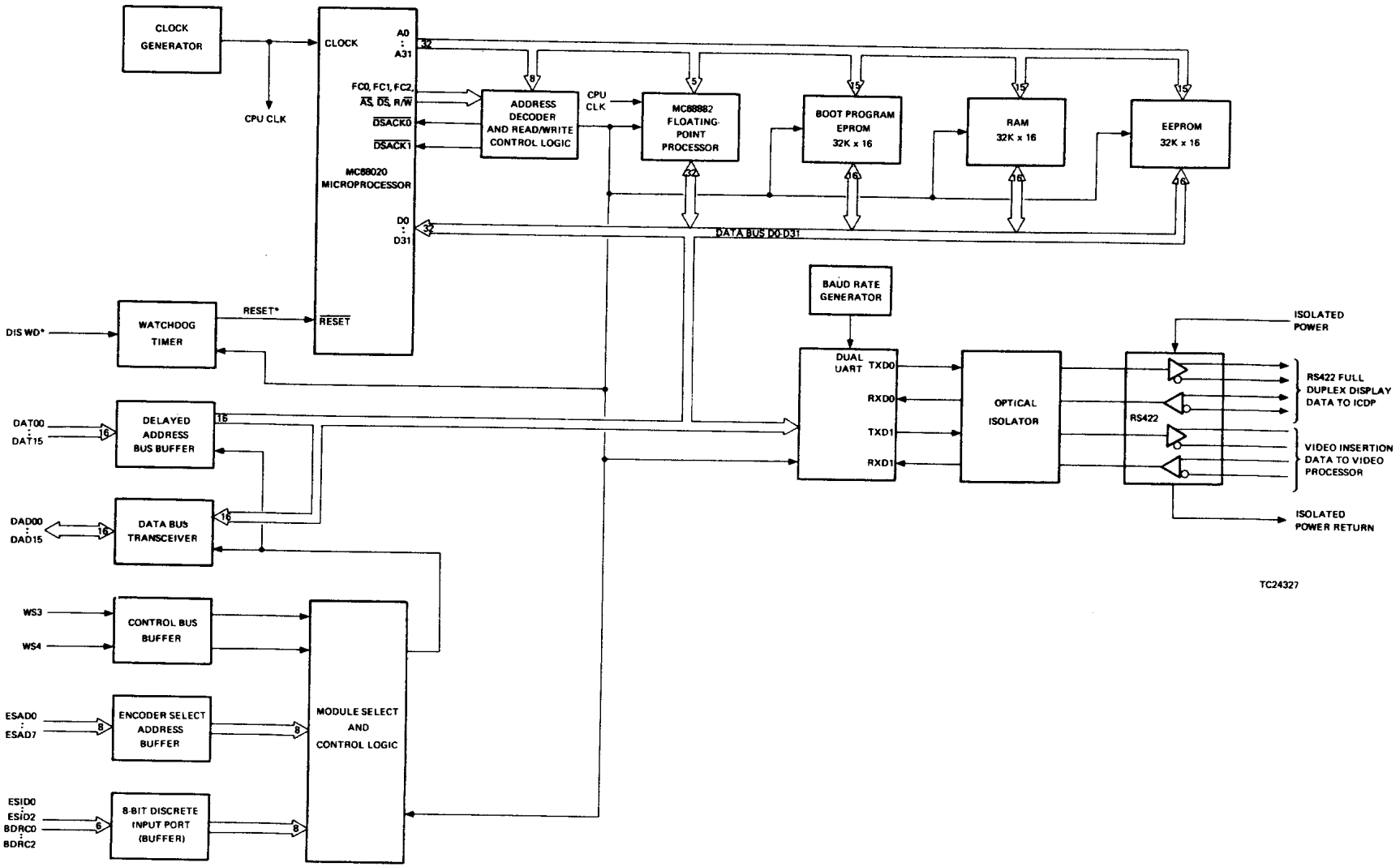

Figure 5. Floating Point Computer Module (FPC)

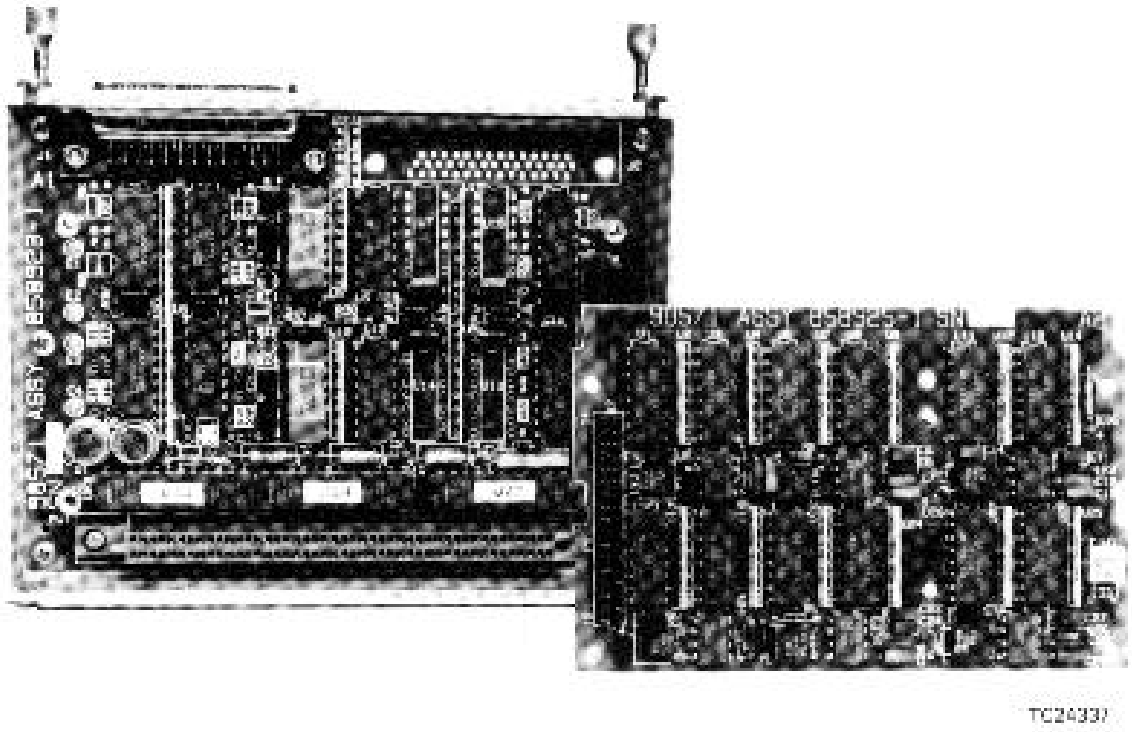

Figure 6. 2-Channel Programmable Presample Filter

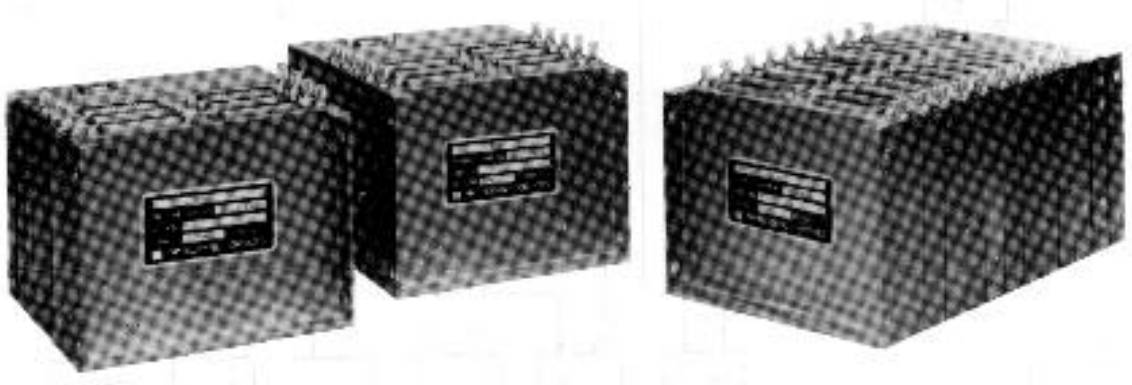

Figure 7. RMDU Configurations

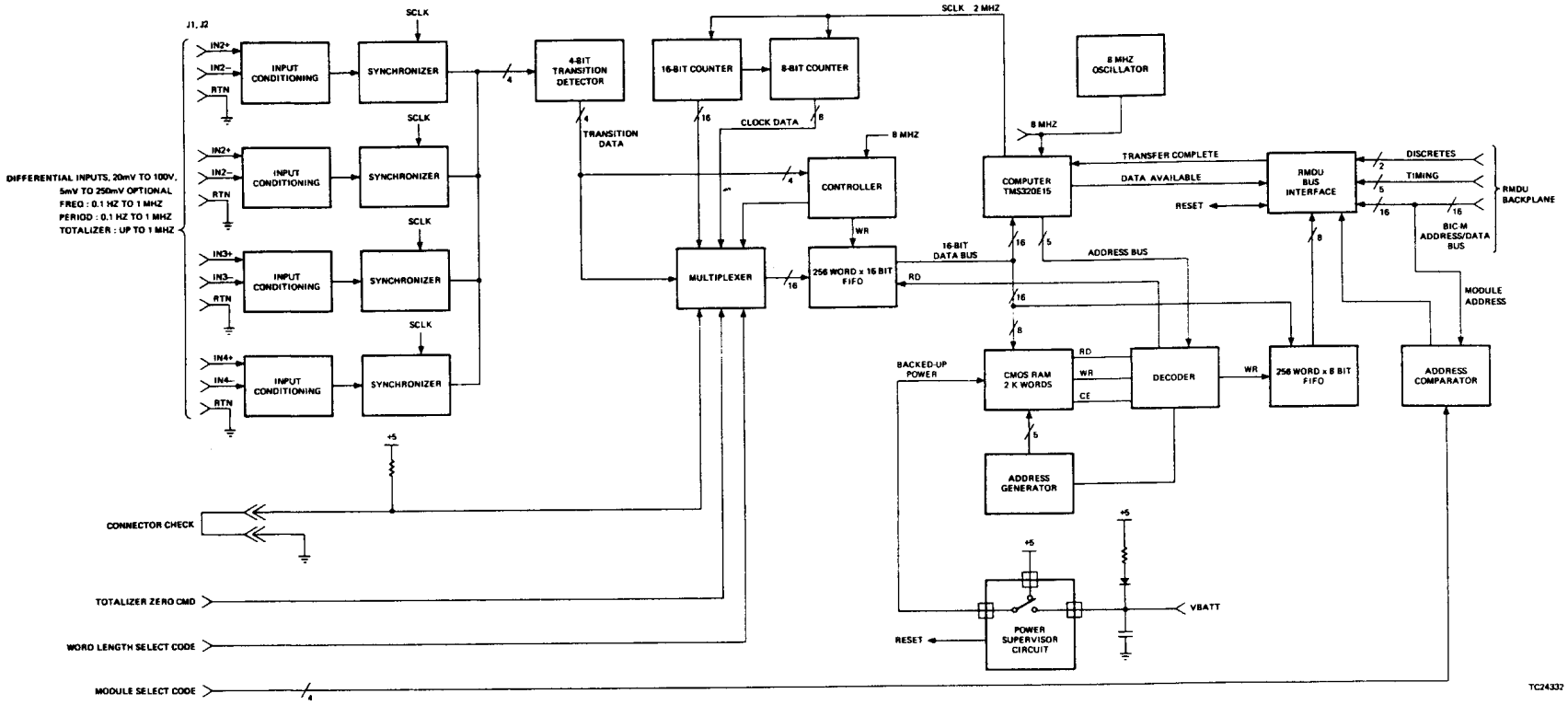

Figure 8. FDC Module Functional Block Diagram

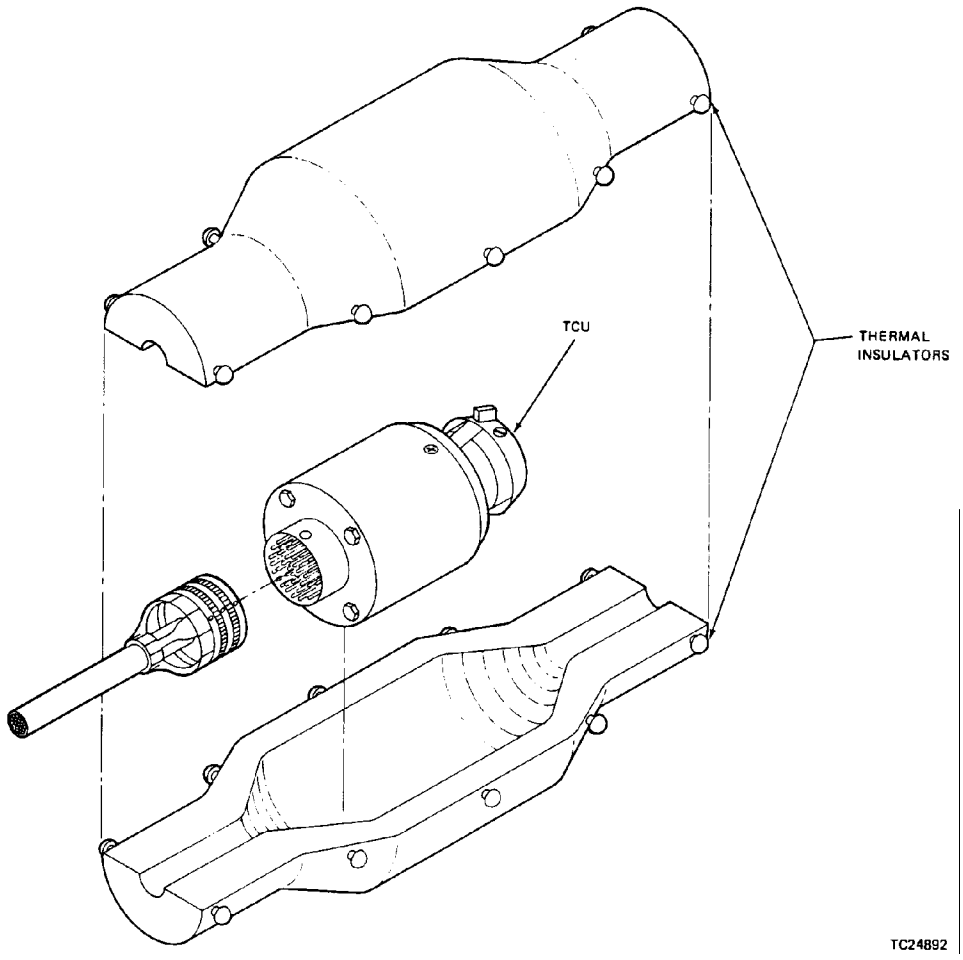

Figure 9. Thermocouple Compensator Assembly & Thermal Jacket