AN ARCHITECTURAL DESIGN OF AN FDMA/TDM BASEBAND PROCESSOR FOR 20/30 GHZ SATELLITE COMMUNICATIONS SYSTEM*

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ABSTRACT

An architectural design of a baseband processor to provide on-board processing for a 20/30 GHz communications satellite is presented. The operation of this processor is explained in some detail. Major assumptions, considerations and goals that shaped the design of the baseband processor are identified and discussed. Since a primary benefit of on-board processing is flexibility, systems employing a processing satellite system will need versatile network protocols. A two-level network protocol that permits users to specify various parameters of their message links and to use different routing protocols on a message-by-message basis is presented here.

INTRODUCTION

Due to the imminent saturation of the 4/6 and 12/14 GHz satellite communications bands, NASA is encouraging the development of the 20/30 GHz bands with possible provision for customer premises service (CPS). Under a NASA contract, MITRE has performed a systems study of a 20/30 GHz processing communications satellite with a total throughput of 4 Gb/s (1.6 Gb/s baseband processed traffic, and 2.4 Gb/s microwave-switched trunking traffic). In this paper we describe just the baseband processor section of a proposed communications satellite consisting of the following subsystems:

- 16 uplink beams (8 fixed, 8 scanned)
- 16 receivers
- 128 demodulators (8 per receiver)
- the baseband processor
- 16 remodulator/transmitter assemblies
- 16 downlink beams (8 fixed, 8 scanned)

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Each scanned regional beam dwells on eight subregions every scan period. The eight cyclic illuminations of the 64 subregions, together with the fixed-beam coverage of eight high-traffic centers, provides CONUS coverage. The use of 16 non-overlapping uplink and downlink beams permits a 16-fold frequency reuse. As a result, the proposed 1.6 Gb/s baseband processor throughput requires only 100 MHz bandwidth per beam using a nominal modulation efficiency of 1 b/s/Hz. The remainder of the allotted 2.5 GHz bandwidth is used for trunking traffic.

In a narrow sense, a baseband processor is the subsystem of the satellite communications payload that manipulates bits or sequences of bits (packets) of information obtained from the digital signals received on the uplinks [1]. The inputs and outputs of this subsystem are binary data only. In a wider sense, the baseband processor could also include the demodulators and remodulators because they are in part digital interfaces through which the on-board digital processor communicates with the outside world. In this paper, we describe the baseband processor in a narrow sense, but we also include overall system considerations that impact the design of the processor.

BASELINE SYSTEM ASSUMPTIONS

Some important features of an advanced domestic satellite communications system are: 1) multiple beam antennas for frequency reuse; 2) bandwidth-efficient modulation and coding for spectral and power conservation; and 3) on-board processing and switching for servicing the many different types of users. These features must be kept in mind while designing new generation communications satellites.

Near-future satellite weight and power constraints associated with the baseband processor portion of the communications payload are expected to be in the order of 400 kg and 2 kW. This includes the functions of uplink RF reception and demodulation, baseband processing of data packets, remodulation, and downlink transmission power; antenna weight is not included. With this weight and power budget, the system can be expected to support approximately 100 MHz per link of spectral bandwidth allocated to signals to be processed at baseband [2].

System resources such as fixed beams, dwell periods of scanning beams, bandwidth, and terminals are initially allocated according to a traffic model. This model is based on three assumptions: 1) there is to be full connectivity between all users in the network; 2) the distribution of terminals will be directly proportional to human population; and 3) traffic from area A to area B is proportional to the number of terminals in both areas A and B. This is contrary to normal telephone traffic where local calls are assumed to constitute a relatively fixed percentage of the total traffic of a region, regardless of the region’s population. The traffic model used here reflects the idea that most of the communications

to be processed by the satellite will be among private corporations, government agencies, universities, and other institutions generating high-volume, long-distance traffic. After the network is operational, resources will be allocated on a dynamic adaptive basis using the traffic model mainly for “system initialization”.

Due to considerations of terminal cost and power, timing synchronization difficulties, and signal interference/distortion, the uplink will operate in a scanned FDMA mode with DAMA, while the downlink will operate in a TDM mode. Uplink and downlink frame formats are given in figure 1.

A frame duration of one millisecond was selected for the following reasons. Considerations of routing and protocol versatility as well as error management necessitated packet header lengths of nearly one hundred bits. To keep packet overhead within 5 to 10 percent of the total, packet lengths should be in the range of one to two thousand bits. Since the traffic is expected to be predominantly voice, and the digital voice T1-carrier rate (1.544 Mb/s) is a domestic standard, then a terminal operating at a T1 data rate would generate 1544-bit data packets for a frame time of 1 ms. For complete (header plus data) packets, the terminal rate would then be about 1.64 Mb/s.

There are, as mentioned earlier, eight beam dwell periods (i.e., TDM slots) in each beam scan period (i.e., one frame), so that the duration of each dwell period is 125 μs. Further, within each slot, there are eight FDM uplink channels and eight TDM downlink sub-slots. Thus, during any beam dwell period (slot), the 16 beams can accomodate up to 128 terminals, and over a beam scan period (frame), up to 1024 different terminals. Since each T1-rate terminal is accessed for only one eighth of a frame, it must burst data up a rate of a little over (due to packet header bits) 8 times T1, and receive data bursted down at a rate of a little over 64 times T1.

This processing satellite should of course provide all user services currently supported by non-processing communications satellites. By virtue of the on-board processing power available, a variety of additional services can also be offered. These services will require the implementation of versatile protocols.

NETWORK PROTOCOLS

In the design of the baseband processor, a number of system requirements and goals must be defined. One major system requirement is the design of a network-wide protocol. This protocol must provide the users with a standard format to exchange messages, to maintain timing synchronization, to establish and terminate circuit connections, and to recover from message losses.

The network protocol developed for this system is organized as a two-level protocol. Each level is supported by a protocol which is custom tailored to meet the needs of the on-board processing satellite communications system. The protocol on the first level provides a DAMA reservation scheme. The second level protocol controls the transmission of messages between the terminals. This two-level structure allows each protocol to operate independently.

The protocol independence achieved by this two-level scheme affords the network considerable flexibility. Updating or replacing an existing protocol on one level does not necessarily require an adjustment on the other level. In fact, it is possible to offer more than one level-two (packet routing) protocol to the users simultaneously. Users can then select the protocol best suited for their needs on a message-by-message basis.

The primary function of the level-one protocol (Link Establishment Protocol) is straight-forward: the Link Establishment Protocol (LEP) must provide every user with the ability to request and to receive a channel assignment. In order to support this service, the protocol must provide a standard procedure in which channel requests, assignments and denials can be made in a format usable by all terminals. Since the network connects terminals that use different data rates, message types and special services, the protocol must be flexible in design and general in operation. One type of link establishment procedure (multipoint) handled by this protocol is presented in figure 2 in a transition-diagram format.

The orderwire system considered in this work allows a user to request a channel for the duration of his message. In addition, the user specifies the message type, length, priority and destination(s). He may also request special functions (e.g., broadcasting, conferencing, etc.) and/or special data rates. This flexibility allows every user to custom order a channel suited to his needs.

Although the function of this reservation system is to provide the users with a means of requesting contention-free message channels, the orderwire channel itself is not constrained to any particular accessing scheme. In fact, there are several accessing schemes which are suitable for use on the orderwire channel. The more popular schemes are Pure Aloha, Slotted Aloha and TDM [3,4]. The selection of one accessing scheme over another for the orderwire depends greatly on the characteristics of the network.

Use of the Pure Aloha accessing scheme for the orderwire is recommended for networks that do not require frequent channel assignments. One such network would consist of a large number of terminals that transmit short, bursty messages on an infrequent basis. Another network suitable for the Aloha scheme is one with a large number of terminals that only need access to the orderwire processor after long periods of time because they are constantly busy transmitting long messages. Slotted Aloha could be used in similar

networks to improve efficiency at the cost of additional complexity. In order for TDM to be efficient, the terminals must make use of their assigned slots as often as possible.

The reservation system proposed for this satellite may not serve all users efficiently. Low duty terminals that transmit only a few packets at one time will incur a large amount of LEP overhead while reserving a message channel. These terminals should be provided with an alternative accessing scheme. One possible alternative is to provide these users with a contention channel. Users could compete for this channel by directly transmitting their message-packets. A Pure Aloha or Slotted Aloha scheme could be implemented on this channel.

When a user has established a link to his sink(s) via the LEP, he begins the transmission of his message. The exchange of messages between the terminals is controlled by a packet-routing protocol (PRP). Since the network supports different users, data rates, message types and transmission modes, more than one PRP is needed to control the traffic. The proposed scheme requires the source to select the best suited protocol available from the network for each message he sends. The source must specify the protocol chosen when requesting the link so that the sink(s) can be notified. Thus, once the actual message transmission starts, both the source and the sink(s) are synchronized to operate under the same protocol.

The PRPs may be organized as either end-to-end protocols that are transparent to the satellite switching processor or as uplink protocols that require on-board processor capabilities. Due to lack of space, the wide variety of message types allowed can only be hinted at by presenting a few of the major message characteristics supported by these protocols:

1) Traffic types
- Voice
- Data
- Video
- Facsimile

2) Routing Mode
- One-to-one
- One-to-many (broadcasting)
- Many-to-many (conferencing)

3) Time Mode
- Real-time
- Non-real-time

4) Error Management (end-to-end and/or uplink)
- ARQ (Automatic repeat request)
- FEC (forward error correction

5) Circuit Type
- HDX (Half duplex)
- FDX (Full duplex)

THE PROCESSOR ARCHITECTURE

Figure 3 contains a simplified block diagram of the baseband processor. Each of the 16 on-board receivers is assigned to one of the 16 uplink beams. Each receiver separates and demodulates the eight FDMA channels arriving within the beam during each slot. The serial bit streams from each channel pass through an input switching matrix. The purpose of this matrix is to ensure that every channel can be connected to one of several possible switching processors. The paths through each matrix are established by the on-board system control computer. Generally, once these paths are established they remain fixed. However, if the need arises due to hardware failures, exceptional traffic conditions or related network problems, these paths can be altered on command from the network control center.

Since every switching processor provides service to one uplink channel and one downlink channel, the baseband processor employs 128 active processors. Thirty-two additional switching processors are available to the baseband processor, to provide 25% redundancy, bringing the total to 160. These switching processors are implemented via microprocessors that require local read only memory (ROM), random access (RAM) and external support hardware. The switching processors receive special control signals from an on-board system control (SYSSCON) computer. At the onset of each new message, SYSCON provides protocol information, message length data, routing procedures, and special handling instructions to the proper switching processors.

The switching processors have three principal functions. One function is to store arriving packets in available locations in the satellite's bulk memory (BM). The function of the bulk memory array is to hold all received packets until they can be routed and sent to the proper sink(s). A bulk memory controller (BMC) maintains a list of empty locations, full locations, and locations out of service. The BMC has three major tasks: 1) to monitor the status of every bulk memory module; 2) to accept the addresses of unneeded BM modules from the switching processors; and 3) to provide the addresses of available DM modules to the switching processors on demand.

While an incoming packet is being stored into an available bulk memory module, the switching processor begins its second function which consists of processing the packet's header. During the processing, the switching processor determines the packet's destination, determines if the packet has multiple destinations, carries out PRP-related functions, and when necessary, corrects the header. After determining the packet's destination, the switching processor sends this information to the first-in-first-out (FIFO) controller. The FIFO controller (FFC) is responsible for the routing of all packets that have been received by the baseband processor. In order to carry out this task, the FFC must be provided with the packets' destination and their module locations in the BM array. The

FFC routes each packet by placing the packet's bulk memory address into the proper FIFO list. Each microprocessor is responsible for eight FIFO lists (one for a specific channel in each of the eight downlink slots).

The switching processors' third function starts when the processor accesses the FIFO corresponding to the current slot. If the FIFO contains data, the processor fetches the oldest address in the FIFO. Using this address, the processor fetches the addressed packet from the bulk memory and sends it to one of the transmitters where it is beamed down to the proper sink.

PROCESSOR OPERATION (POINT-TO-POINT TRANSMISSION)

In order for a user to use the baseband processor, he must first communicate with the controller via the LEP. Once in contact with the controller, the user requests a satellite link to one sink. If the sink is free, the controller establishes the message link. After the user is allocated this link, he formats his message into packets and begins transmission. The operation of the baseband processor is explained by tracing the path of one of this user's packets through the processor.

After receiving notification that the satellite link has been established, the user prepares for transmission. Meanwhile, the switching processor assigned to receive the user's call is also preparing for the call. The processor carries out this preparation during a 10 μs second guard time in the 125 μs slot assigned to the user. During this guard time, the processor fetches the address of an available BM module from the BMC. The processor then places this address into its Input Address Register in the BM array, thereby reserving a memory module for the incoming packet.

As the packet arrives at the demodulator, it is converted into a bit stream. The packet enters the baseband processor serially through the input switching matrix. At the switching processor, the serial bit stream is collected in a serial-to-parallel shift register. When this shift register is full, a 32-bit word is transferred to the Data Input Register shown in figure 4. This is a 32-bit parallel-in-parallel-out register. Both the Input Register and the Input Data Register are connected to the bulk memory input address/data bus which serves 1320 memory modules. There are 160 dedicated register pairs servicing the switching processors. The switching processors send the packets to the BM array in the form of 32-bit words which arrive at the rate of one word per 2.45 μs. A hardware poller enables one input register pair onto the bus at one time. The BM address is decoded and used to enable a single bulk memory data latch. This latch fetches the packet word from the bus during an approximately 15 nanosecond slot. It then sends the slower bulk memory device eight four-bit blocks, one at a time. A block is sent to the memory device once every 300

nanoseconds, which is a quite reasonable access time for current memory devices. At the end of one slot, fifty-one 32-bit transfers have taken place for each incoming packet.

While each 32-bit word is being stored, the switching processor makes a copy of the packet's header and stores it in local RAM. After the entire header has been duplicated and stored, the switching processor processes it. This processing includes all PRP-related functions, error correction, and the decoding of the packet's destination address. After the sink address is decoded, the switching processor sends it and the packet's bulk memory address to a buffer in the FFC. As soon as the buffer is loaded, the processor sets a flag to indicate to the FFC polling circuit that the buffer contains valid routing information.

The FFC hardware poller scans the buffers of each active switching processor. The contents of an enabled buffer are gated onto the FIFO controller bus. The address of the BM module holding the packet is sent directly from the FFC to the FIFO data bus. The packet's logical destination address is sent to a RAM containing a routing table of downlink FIFO's. Thus the addressed RAM location contains the address of the FIFO list that corresponds to the packet's destination. (Since this translation is done in a RAM, routing updates can easily by made by SYSCON.) The selected FIFO address is then sent to the FIFO address bus which is connected to every FIFO list. When a list recognizes its own address, it latches the BM address data. Once a packet's BM address resides in a FIFO list, the packet is considered routed.

Every switching processor has eight FIFOs. Each FIFO corresponds to one unique channel in a unique downlink slot. During each guard time, the processors check the FIFO list corresponding to the channel they service during the next slot. If a processor finds that the FIFO list is not empty, the processor fetches the oldest BM address from the list. This address corresponds to a location in bulk memory where the oldest packet, destined to the sink being serviced next, is located. This address is placed in the Output Address Register by the processor. Working in conjunction with this register is a 32-bit wide parallel-in-serial-out register called the Output Data Register. On the output side of the BM array, there are 160 dedicated output register pairs servicing the switching processors. These register pairs are attached to the output address/data bus. Whenever a switching processor is required to transmit a packet, it must place the packet's BM module address into the register pair. A hardware poller enables one register pair onto the bus at one time. The address is decoded and used to select a single bulk memory output data latch. The latch places its contents (a 32-bit packet word) onto the bus. The word is then strobed into the data portion of the enabled output register pair. The data is then shifted our serially and is routed to the proper remodulator by the switching processor. After the contents of the latch are emptied onto the bus, the latch fetches the next eight 4-bit blocks from the memory. module. The latch is completely reloaded in 2.45 μs and ready to be accessed again as the poller completes its cycle. This operation continues until the packet-length shift registers in

the remodulators are filled and ready for the transmission cycle. Therefore, in order for a packet to be transmitted down on the desired channel within the proper slot, it must be sent to the remodulator shift register exactly one slot prior to its transmission.

Each switching processor is actually responsible for two of the serial-in-serial-out shift registers found in the remodulator sub-system -- one is being filled in advance by the processor while the other is being emptied by the remodulator. These registers must shift a packet into the remodulators at the rate of about 100 Mb/s so that the packets can be bursted down to their sink on the selected channel within the proper slot on a TDM basis.

The operation of the baseband processor is similar when routing message packets that have multiple destinations. The major difference is that a multipoint packet is kept in the bulk memory until a copy of it has been sent to each destination.

CONCLUSIONS

Although some elements of the design presented here assume state-of-the-art technology, such a system could at present be built, by reducing, if necessary, the throughput, the bulk memory, timing constraints, and some of the flexibility. In fact, under a NASA contract, Motorola Corporation is developing a baseband processor for near-future applications [5]. In order for future satellite systems to be competitive with terrestrial networks, they must offer the users new services, flexibility, low cost operation and reliability. In addition, the future satellite systems must make efficient use of dwindling bandwidth and orbital arc resources. It is hoped, accordingly, that on-board processing will lead to substantial contributions toward these goals.

However, a number of problems still remain to be solved if baseband processors are to reach their full potential. Improvements in gate delays, power consumption, radiation hardening, gate densities, and protocol flexibility and standardization are needed. Progress is being made in most of these areas by private industry and government sponsored research (e.g., the VHSIC program). As mentioned several times before, this design is intended for future applications in the 20/30 GHz bands. However, once the technology is developed and proven, there is no reason why baseband processors cannot be used in other frequency bands (both higher and lower than the 20/30 GHz band).

ACKNOWLEDGMENT

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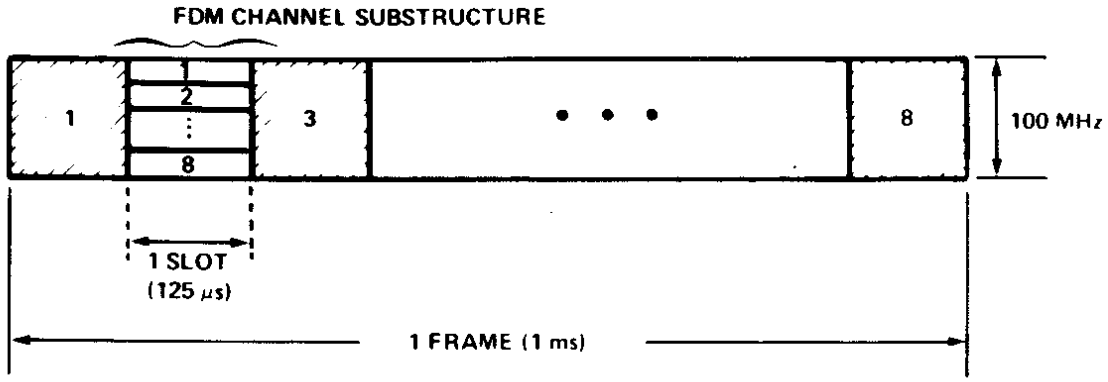
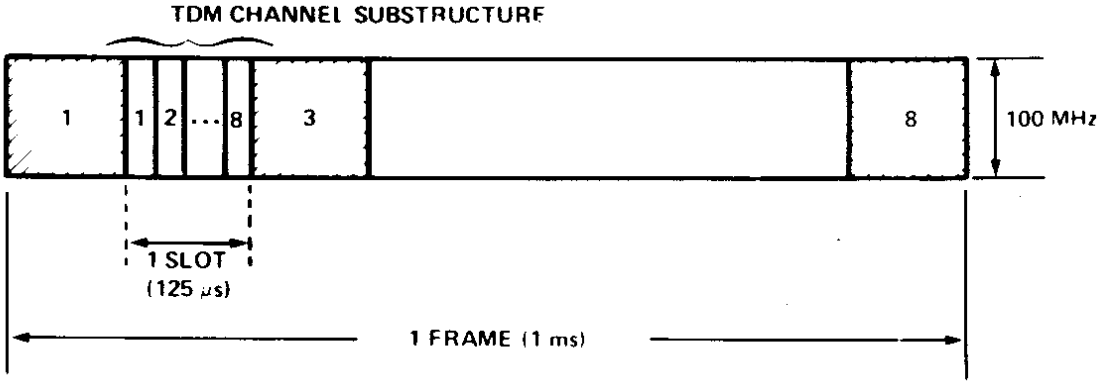
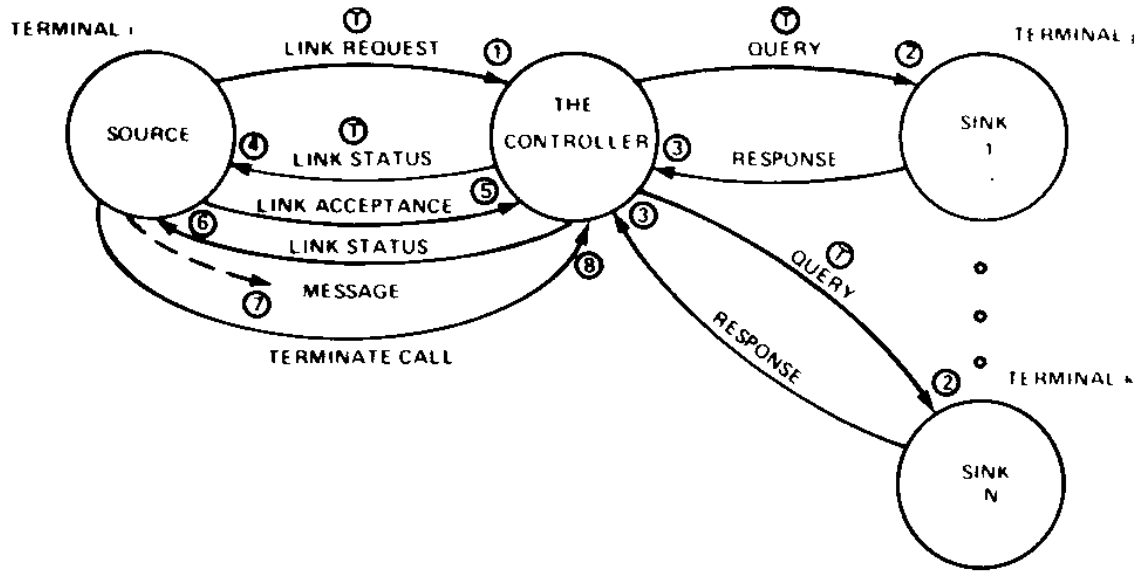


A. UPLINK FRAME FORMAT (30 GHz)



B. DOWNLINK FRAME FORMAT (20 GHz)

Figure 1. THE UPLINK AND DOWNLINK FRAME FORMATS FOR THE SIXTEEN RF AMS SERVING THE BASEBAND PROCESSOR



① THE SOURCE (TERMINAL i) TRANSMITS A LINK REQUEST TO THE CONTROLLER REQUESTING A MULTIPOINT LINK TO SINKS 1 (TERMINAL j) THROUGH N(TERMINAL k)

② AFTER RECEIVING THE LINK REQUEST THE CONTROLLER SENDS A QUERY TO EACH OF THE SPECIFIED SINKS

③ EACH SINK REPLIES TO THE QUERY BY SENDING THE CONTROLLER A RESPONSE

④ IF NOT ALL OF THE SINKS ARE ABLE TO RECEIVE THE SOURCE'S MESSAGE THE CONTROLLER SENDS THE SOURCE A LINK STATUS PACKET INDICATING WHICH SINKS ARE READY AND THOSE THAT ARE NOT NO OTHER ACTION IS TAKEN AT THIS TIME

⑤ AFTER RECEIVING THE LINK STATUS PACKET, THE SOURCE SENDS THE CONTROLLER A LINK ACCEPTANCE PACKET INDICATING WHETHER OR NOT THE SOURCE WANTS TO TRANSMIT TO ONLY THOSE SINKS CURRENTLY AVAILABLE

⑥ THE CONTROLLER WILL ESTABLISH CIRCUITS FROM THE SOURCE TO THE AVAILABLE SINKS AND IT WILL ALSO SEND THE SOURCE A LINK STATUS PACKET INDICATING THIS HAS BEEN DONE ONLY IF THE SOURCE SENT A POSITIVE LINK ACCEPTANCE PACKET IF THE SOURCE SENT THE CONTROLLER A NEGATIVE LINK ACCEPTANCE PACKET, NO CIRCUITS WOULD BE ESTABLISHED AND THE SECOND LINK STATUS PACKET WOULD NOT BE SENT

⑦ ONCE THE SOURCE RECEIVES THE SECOND LINK STATUS PACKET THE TRANSMISSION OF THE MESSAGE TAKES PLACE

⑧ THE SOURCE SENDS THE CONTROLLER A TERMINATE CALL PACKET AT THE CONCLUSION OF THE MESSAGE TRANSMISSION

Ⓣ TIME OUT CLOCK IS STARTED

N 15

Figure 2 THE LINK ESTABLISHMENT PROTOCOL (PARTIAL MULTIPOINT)

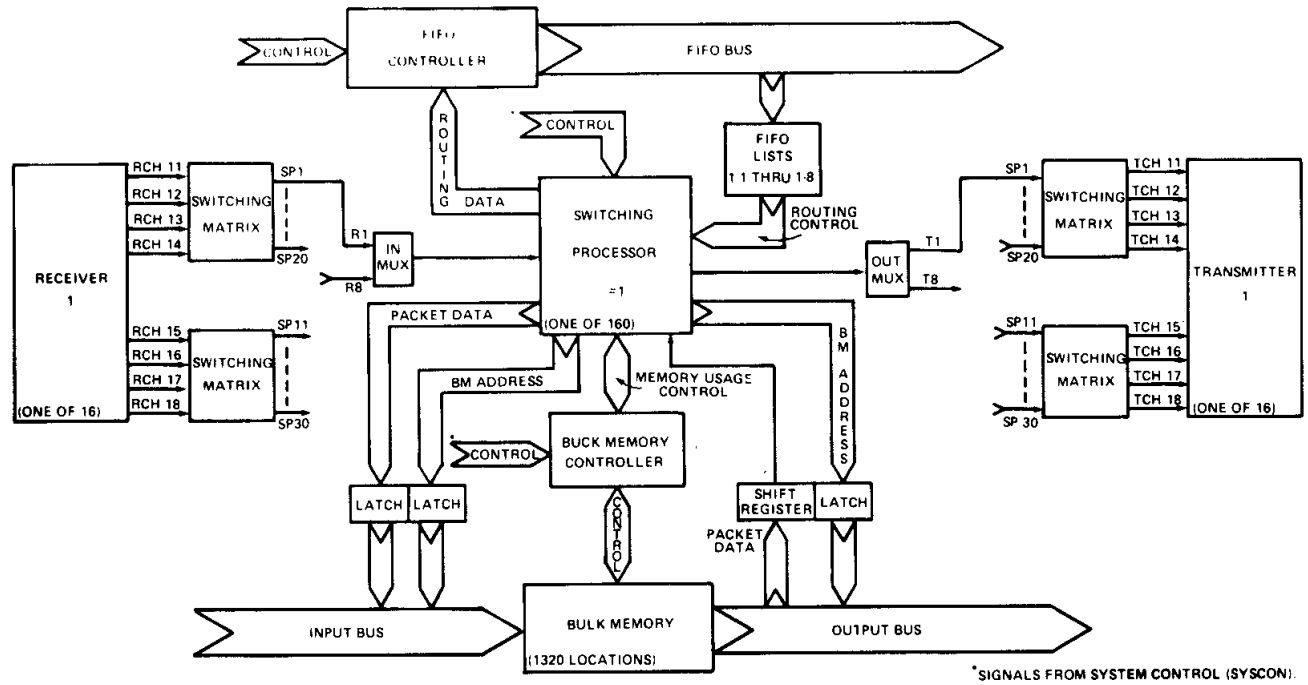


Figure 3 SIMPLIFIED BLOCK DIAGRAM OF THE BASEBAND PROCESSOR

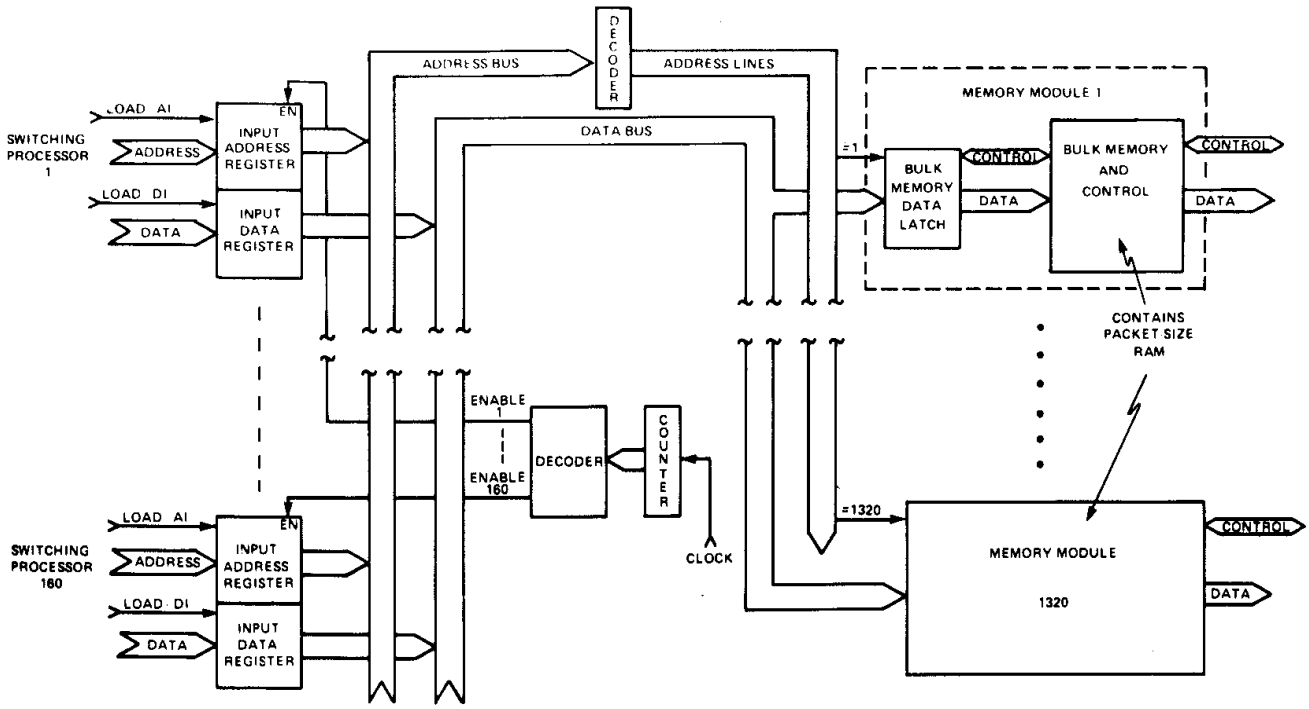


Figure 4 THE BULK MEMORY ARRAY (INPUT SIDE)