AN EHF (Q-BAND) RECEIVING SYSTEM

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Abstract

Operating communication systems at EHF offers the important advantages of the improved antijam performance (wider bandwidth availability) and low probability of intercept. However, space rated communication hardware for operation at EHF is not readily available. Using advanced MIC technology, low noise frequency synthesis techniques and a subharmonic mixing scheme, Rockwell International designed, developed and tested a frequency hopped, 8-ary FSK modulated, Q-band receiving system for satellite applications.

Detailed analyses were correlated with the experimental test data obtained in Rockwell's ASCOT Laboratory. These test results, along with key design approaches in hardware and synthesizer designs are presented in this paper.

INTRODUCTION

This paper describes an EHF (Q-band) Spread Spectrum Receiving System developed by Rockwell International. Special emphasis is placed upon development problems encountered because of the high receive frequency (approximately 45 GHz) and because of the Frequency Hopped spread spectrum requirement. Conventional receiver design concepts were adhered to, although these concepts are not stressed in this paper.

Three basic sections comprise this paper. The overall receiver design concept along with considerations for deploying the receiver in a military communications network are in the first section: SYSTEM CONSIDERATIONS. Critical design parameters affecting the receiver are noise figure, local oscillator phase noise and frequency synthesizer performance. These parameters are also covered in Section 1. Detailed functional descriptions of the hardware are contained in the HARDWARE DESCRIPTION section. Included are overall system design, EHF receiver front end, frequency synthesizer reference generator and UHF receiver. The last section consists of conclusions and test results, and also contrasts these measured results with theoretical predictions.

SYSTEM CONSIDERATIONS

A common requirement of modern military communication systems is the ability to perform in a hostile signal environment. In many cases, the antijam performance of the communications equipment is a measure of the equipment value simply because of the need to operate in a secure mode or in a hostile signal jamming environment.

Frequency hopping (FH) is one important means of providing jammer discrimination. The degree to which the jammer can be rejected is directly related to the hopping bandwidth. Consequently, the wide bandwidths available at high frequencies make a Q-band receiving system most attractive.

Because of the high frequency at Q-band, the small size of antennas and antenna beam width contribute significantly to the LPI (low probability of intercept). Hence, the communications operation at Q-band offers two important advantages: Increased antijam performance (increased rf bandwidth) and low porbability of intercept.

Conventional, as well as spread spectrum receiving systems, are characterized by the receiver performance with low level desired signals in the presence or absence of high level undesired signals. This receiving system design is based upon system and circuit analyses which determined the receiver performance requirements. Major parameters which contribute to the FH receiver performance are: receiver noise figure, local oscillator phase noise; frequency synthesizer acquisition time; and receiver and synthesizer spurious performance.

Receiver Noise Figure

In the absence of any jamming signals, the thermal noise generated by the receiver determines the low level signal performance of the system. Since the LPI performance of the system depends, to some degree, on the required transmitter power, receiver sensitivity (noise figure) is an important design parameter. At EHF frequencies, active devices are not as readily available as those at lower frequencies. So, to optimize the overall noise figure, it is required to choose the best frequency conversion scheme along with designing and building the low noise circuits.

The familiar noise figure equation

$$F_T = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_n} \qquad (1)$$

describes the overall system noise figure F_T as a function of the gains and noise figures for the cascaded stages. The obvious advantages of using a low noise, high gain input stage demanded that an EHF preamplifier be considered. However, as described in the section, EHF FRONT END, the low noise active devices are not readily available. A reasonable trade then is to utilize a low noise mixer at the input followed by a very low noise IF amplifier. The desired overall noise figure is 8.5 dB maximum; the best available IF amplifier noise figure (at the frequency of interest) is 2 dB with virtually unrestricted gain. From these known values, the maximum allowed noise figure of the input mixer (including the input filter) is determined to be 6.5 dB.

Local Oscillator Phase Noise

M-ary FSK modulation performance of the Q-band system depends upon the phase and frequency stability of the carrier and receiver local oscillator signals. The nominal operating frequency of the Q-band receiving system is 45 GHz, so that the noise level of lower reference signals will be increased by at least $20\log(45 \times 10^9) \div fr$ where fr is the reference frequency. When the local oscillator noise level is singificant compared to the thermal noise, then the system performance will be degraded accordingly. The effect of the "close-in" phase noise is to degrade the receiver signal-to-noise (or Bit Error Rate) performance. Local oscillator noise components farther away from the carrier degrade the antijam performance by allowing strong CW jamming signals to convert this broadband noise to the receiver intermediate frequency (IF) range.

To determine the performance requirement for the receiver, analyses were performed in which the L.O. noise contributions were considered. The effect of the phase noise depends on the particular energy-per-bit noise density ratio (E_b/N_o).

As stated, the reference oscillator phase noise (at the receiver frequency) will effectively be increased by the multiplication ratio. The following analysis summary assumes a reference generator using a 16 MHz signal as the basic reference frequency; (this is comparable to the 10 MHz reference used in the actual design). The objective of this task was to calculate phase noise degradation at 45 GHz given single side band measurements L(f) of a 16 MHz reference generator.

The L(f) at 16 MHz was raised to 45 GHz as shown in Figure 1. For M-ary FSK, the performance degradation due to phase noise can be shown to be:

$$\frac{y_0^2}{1 + \frac{C}{N_0 B} y_1^2} \qquad (2)$$

where $\frac{C}{N_0 B}$ is the signal-to-noise ratio, and y_0 and y_1 are determined as follows:

$$y_0^2 = 1 - \int_1^{BW} \left[1 - \left(\frac{\sin \frac{\pi f}{\Delta f}}{\frac{\pi f}{\Delta f}}\right)^2\right] S_\phi (f)\, df \tag{3}$$

$$y_1^2 = \int_1^{BW} \left(\frac{\sin \frac{\pi(f-\Delta f)}{200}}{\frac{\pi(f-\Delta f)}{\Delta f}}\right) S_\phi (f)\, df \tag{4}$$

where $S_\phi (f) = 2L(f)$, f is the frequency offset. Δf is the tone spacing and BW is the IF bandwidth

Figure 2 shows degradation versus E_b/N_o for the specific L(f) (single-sideband phase noise) of Figure 1.

Frequency Synthesizer Performance

Since the energy loss per frequency change (or hop) is directly related to the settling or synthesizer acquisition time, it is desirable to operate the system dehopping local oscillator at low frequencies where the carrier instabilities, frequency error or spurious signals will not be increased due to multiplication; on the other hand, to dehop wide bandwidth signals, a high frequency synthesizer output is desired, since the actual percentage bandwidth will be significantly less. Therefore, the overall receiver design implementation is affected by the frequency synthesizer design concept. Also, for space application, complexity, size, weight and power consumption are important considerations.

Key receiver requirements, as related to the synthesizer performance are:

frequency hopping increments
frequency acquisition time
spurious output levels
phase noise levels

To satisfy the relatively slow hopping rate, but very strenuous phase noise requirements, the indirect frequency synthesizer results in substantial reduction in weight and power consumption when compared to the direct frequency synthesizer. In this indirect frequency synthesizer, a single high performance phase lock loop and direct digital frequency

synthesizer were combined to obtain very small step size (< 2 Hz) along with small settling time (less than 500 microseconds).

The frequency synthesizer settling is actually composed of two parts: VCO sweep time τ_s, and the loop response time τ_1 τ_s is the time required to move the VCO frequency sufficiently close to the reference frequency so that the frequency error is about equal to the phase lock loop bandwidth, and cycle slipping ceases. The loop response time τ_L depends on the final frequency or phase error required after some given time Δt; ($\Delta t = \tau_L + \tau_s$). For the analysis, assume that after a time Δt, it is required to reduce the phase error to less than $\Delta\phi$ radians. Then,

$$\Delta\phi \doteq \omega_n t(\exp-\omega_n t) = (\omega_n \tau_L)(\exp-\omega_n \tau_L) \tag{5}$$

Using a phase/frequency detector in the loop eliminates the need to preset the VCO and the frequency scan time is approximated by:

$$\tau_s = \frac{\Delta F_o}{2N\omega_n{}^2} \tag{6}$$

N is the divider ratio;
ω_n is the loop natural radian frequency
ΔF_o is the maximum frequency increment over which the vco must tune.

From the first equation it appears that the larger the time τ_L and the loop radian frequency ω_n, the smaller the phase error $\Delta\phi$. But, the time to lock, τ_L is limited by the system requirement and ω_n is limited by the actual operational amplifier speed and desired reduction in reference or spurious frequency. For this system, the reference frequency is 3.2 MHz; the desired level at the L.O. output is at least 30 dB below the carrier. Since the level of feed through from the phase detector is known, and the cut-off frequency of the low pass filter used to filter this feed through can be determined. This cut-off frequency must be sufficiently high so that significant phase shift at the loop natural frequency is not added. The selected cut-off frequency for the present design was approximately 200 KHz; this provides 24 dB attenuation to the 3.2 MHz feed through and causes of phase shift of 5.7° at 20 KHz and 11.3° at 10 KHz. When phase shift resulting from other parameters was considered, a five degree maximum phase shift due to low pass filter was allowed--resulting in a maximum allowable loop frequency of about 20 KHz.

Having selected the natural frequency of 20 KHz (nominal) the lock-up time τ_L was determined.

From the system requirements, $\Delta\phi \leq 30^\circ$ (at 45 GHz) after time τ_L. Therefore,

$$\Delta\phi' \quad \frac{30^\circ}{32(44)} = 0.021^\circ = 3.7 \times 10^{-4} \text{ radian at the phase detector}$$

$N_{max} = 44$ and multiplication ratio is 32. For

$$\omega_n = 2\pi fn = 2\pi\ (20 \times 30^3) = 1.26 \times 10^5$$

from (5), and

$$\omega_n\tau_L = \Delta\phi' \exp(\omega_n\tau_L), \text{ and } \omega_n\tau_L \doteq 10.3 \text{ satisfies the above equation;}$$

$$\tau_L = \frac{\omega_n\tau_L}{\omega_n} = \frac{10.3}{1.25 \times 10^5} = 83 \times 10^{-6} \text{ second}$$

The sweep time is

$$\tau_s = \frac{(60 \times 10^6)}{(2)44\ (1.26 \times 10^5)^2} = 43 \times 10^{-6} \text{ second}$$

The total time to acquire a new frequency is

$$\tau_s + \tau_L = (43 + 83) \times 10^{-6} \text{ sec} = 126\ \mu\text{sec}$$

So, the maximum required lock-up time should be less than 200 microseconds.

HARDWARE DESCRIPTION

The Q-band receiving system consists of the EHF Front End frequency synthesizer/ reference generator and UHF receiver. Since the UHF receiver had been developed earlier, the most efficiency configuration for the overall EHF receiver was to provide coarse dehopping of the wideband FH input fignal. After coarse dehopping, the fine dehopping is accomplished in the UHF receiver section. Figure 3 is an overall block diagram of the complete receiving system. A photograph of the actual system in the test set-up is also shown in Figure 4.

The microwave FH signal at approximately 45 GHz is applied to the EHF Front End frequency converter. This frequency converted local oscillator signal is derived by the frequency synthesizer local oscillator chain. Since the EHF frequency converter uses a subharmonic mixer, the local oscillator input frequency is effectively multiplied by two in the mixer and the L.O. frequency is one half that required if a conventional mixer were

used. All the reference signals and L.O. signals are derived indirectly from the frequency standard by the reference generator.

The output of the EHF down-converter is applied to the UHF receiver (in the 2 GHz range). Here, fine dehopping is done and final IF filtering and dechannelization are accomplished in the IF processor. This processor provides I and Q outputs (analog signals) to the digital processor. Two channels are available.

As shown in the photograph of Figure 4, a transmitter simulator provides the 8-ary FSK modulation and develops the desired EHF output.

EHF Front End

Since the EHF receiver front end contributes most of the system thermal noise, considerable effort was devoted to selecting the design approach that would result in the best receiver noise figure. The basic considerations were: tradeoff between using low noise preamplifier preceding the mixer, or using a mixer as the input receiving element; utilization of conventional mixer or subharmonic mixer thus reducing the required output frequency of the multiplier chain by a factor of two; and IF amplifier configuration following the input mixer.

Some consideration was given to using an input preamplifier to obtain low noise figure, although these amplifiers are not presently available. The present state-of-the-art of low noise GaAs FETs was recently surveyed. Published data generally does not cover frequencies beyong 20 GHz, however, 30 GHz and above laboratory devices are beginning to appear. Steady progress is being made with reflection amplifiers, where a crucial problem is obtaining the necessary bandwidth. Uniform gain over the passband is achieved with reflection amplifiers. Gain uniformity appears to be a problem with the more conventional type of amplifier, so far. Wide variations in gain (> 5 dB) as well as in noise figure are seen over the passband. Because of the uncertainty as to the availability of adequate FET within the specified time constraint, the basic receiver design did not include the low noise preamplifier front-end.

Compared to Ka-band low noise amplifiers, mixer technology is more established and mature. Mixer-IF pre-amp combinations are usually constructed as a unit, and performance data are given for the unit as a whole.

The basic device in a mixer is the metal-semiconductor rectifying junction. The main features of this junction are a strongly nonlinear current voltage characteristic coupled with the inherently fast response time and negligible minority carrier storage in what is essentially a majority carrier device. To obtain optimum performance, the product of the

series resistance and junction capacitance of the device, which serves as a figure of merit, must be minimized. By employing a high conductivity semiconductor material for the active area, the series resistance is decreased although the capacitance per unit area increases. Thus, quite small junction areas, on the order of 10^{-7} cm^2 or less, are required in order to maintain a reasonable impedance at microwave frequencies at the doping levels yielding optimum semiconductor conductivity.

A tradeoff was performed to determine the desirability of using a subharmonic mixer, where the local oscillator is effectively multiplied by two in the mixer. When power, weight and performance were considered, the subharmonic mixing scheme offered greater advantages. This approach was chosen over the conventional mixer. Figure 5 is a photograph of the subharmonic mixer along with the rest of the EHF section of the receiver.

Frequency Synthesizer/Reference Generator

Figure 6 is a functional description of the coarse-hop frequency synthesizer and reference generator. A reference signal that is a submultiple of stepsize (frequency multiplication following the synthesizer multiplies the stepsize as well as output frequency). Other signals are also required to drive the synthesizer and frequency converter. The reference generator uses a very low noise VCO/phase lock and frequency dividers to generate all these reference signals while maintaining the ultra-stability requirements of frequency standard. To synthesizer multiple or submultiple frequencies from a given reference signal the direct frequency synthesis method (mix-divide-multiply) and the indirect synthesis method (phase lock loop in conjunction with dividers) were considered. For both the synthesizer and reference generator, the indirect method was chosen because of its reduced complexity and power consumption and improved performance.

The block diagram of Figure 6 shows that a single phase lock loop is used to generate 400 MHz. The divider chain provides the desired 3.2 MHz reference needed by the synthesizer. This same divider also provides the reference signal needed to control the phase lock loop. A X3 multiplier generates the 1200 MHz reference/local oscillator signal. Spurious signals which are multiples of 3.2 MHz and/or 10 MHz are essentially non-existent since the baseband analog components in the phase lock loop can provide essentially unlimited attenuation as long as the phase shift introduced into the loop is sufficiently small for loop stability. Photographs of the frequency synthesizer and reference generator are shown in Figures 7 and 8, respectively.

Circuits requiring special development effort to obtain high level of performance were the X16 multiplier (approximately 1300 MHz to 20.8 GHz) and the low noise voltage controlled oscillators (VCO’s). Critical parameters for the multiplier are filter responses

(spurious outputs) output power and high output frequency. The VCO must provide noise levels (outside the phase lock loop bandwidth) sufficiently low that system performance will not be degraded by a strong CW jammer converting the VCO broadband noise to the IF frequency. Within the phase lock loop bandwidth, the noise level must be low enough such that bit-error-rate performance is not adversely affected. The nature of the phase lock loop operation provides noise reduction proportioanl to the offset to the loop natural frequency. So, the most critical noise performance area is at or near the loop corner frequency

K-Band X16 Multiplier Chain

The multiplier chain consists of a one watt power amplifier (at L-band) driving two cascaded X4 multipliers. Three microstrip circulators are used to obtain isolation between these circuits. A uniquely designed, low loss transition couples the energy from microstrip to waveguide.

The K-band X4 multiplier uses a shunt mounted step recovery diode. The circuit was fabricated on a 15 mil Duroid* 5880 substrate which was bonded on a 60 mil thick aluminum plate to prevent warping. The Duroid has several advantages over alumina substrates in that it is less costly, it is easier to machine, and it has a lower dielectric constraint (2.2 versus 10 for alumina). The lower dielectric constant results in less transmission line loss and less sensitivity to line width errors. One problem with Duroid substrates is that the copper metalization oxidizes if not properly treated. To eliminate this problem, the copper was plated with a thin layer of gold or coated with a tin solder. Minimizing the ground plane path between adjacent substrates caused an additional problem due to the thickness of the aluminum plates. One method used to minimize the ground-path length was to grind away part of the Duroid so that the other substrate would overlap onto the aluminum base.

Voltage Controlled Oscillator (VCO)

An important requirement established early in the system development was that the frequency standard noise level (when multiplied up to 45 GHz) must be low enough so that the system is not degraded. In the phase lock loop used, the noise generated by the VCO outside the loop bandwidth is contributed almost solely by the VCO. Within the loop bandwidth, the frequency standard noise would dominate. Therefore, low noise VCOs were necessary for the Q-band receiver. Two VCOs, were required, one for the synthesizer and the other for the reference generator.

* Durois is a registered trademark of Rogers Corporation.

The synthesizer vco is a cavity stabilized bipolar transistor oscillator. The cavity is a foreshortened coaxial cavity 0.7 inches square whose output is lightly coupled to maintain a high loaded Q. The electrical length of the cavity is tuned by a series parallel capacitor and varactor combination in series with the open end of the cavity. A low noise voltage regulator is also incorporated. Since the reference generator VCO output frequency was relatively low (400 MHz) to accomodate the frequency divider operating range, a distributed parameter low noise VCO was used in this circuit. The noise performance of this VCO, was comparable to that of the cavity VCO.

CONCLUSIONS

System and subsystem level test results indicated performance consistent with the initial goals. However, the analytical determinations, in some cases, were not in complete agreement with measured results. At the time of preparation of this paper, the system bit-error-rate tests had not been completed. Table I in conjunction with the graphs of Figure 9, shows the initial system specifications (or goals) along with final results and predicted performances.

The measured noise figure was 10 dB maximum compared to the desired 8.5 dB. In the receiver design, a low noise (≈ 2 dB) IF amplifier follows the low noise mixer. During tests, a failure in the preamplifier stage (low noise stage) resulted in a necessity to bypass this low noise stage, thus raising the noise figure by about 2 dB. The overall system noise figure was increased accordingly.

Frequency hopping bandwidth, synthesizer settling time, phase noise level and power consumption goals were achieved. Predicted frequency synthesizer settling time (200 microseconds) however, was much less than the measured value of 500 μsec. It has been determined that the power dissipation of the VCO (voltage controlled oscillator) tuning element changes very slightly according to the actual output frequency--the larger the frequency increment, the greater the power change. Consequently, the VCO post tuning drift could account for some of the frequency error. Also, the lock-up time is determined by the loop parameters and the divider ratio parameter changes by a factor of 1.76 for the maximum step size. This large divider ratio change causes the loop natural frequency and damping factor to change accordingly. So, it is possible that this change in loop parameters contributed to the discrepancy in computed versus measured values of settling time.

To measure the local oscillator phase noise, two identical synthesizer/reference generator and multiplier chains were offset in frequency, down converted, and measured on the Hewlett Packard 5390A Frequency Stability Analyzer. As shown in Table I, the measured noise levels are well below the required values. However, there are significant

discrepancies between the analytical and measured results. Two major contributions to these discrepancies were found to be the phase lock loops and frequency multiplier chains. Measurements of the free-running VCO phase noise characteristics were compared with the VCO noise characteristics when in the closed loop configuration. Increase of 10 to 15 dB in noise level at some offset frequencies were observed. Analysis and test showed that operational amplifier, frequency dividers and phase detectors could have caused the noise degradation. Although not evident in this receiver design, previous measurement showed some degradation in noise level (above the theoretical values) due to the frequency multiplier excessive gain and high noise figure of the active devices.

Table I EHF Receiving System Performance

Characteristics

CHARACTERISTIC	PERFORMANCE		
	GOALS	MEASURED RESULTS	PREDICTED RESULTS
	8.5 dB Maximum	10 dB	8.5 dB
Frequency Range and Hopping Bandwidth	As Required	Same	Same
Frequency Synthesizer Settling Time	Less than 0.5 millisecond for phase error less than 30°	0.5 millisecond for largest step	200 microseconds for largest step
Phase Noise	See Figure 9	See Figure 9	See Figure 9
Power Consumption	15 watts Maximum (EHF Section)	12.16 watts	12.16 watts
	6 pounds Maximum	5.3 pounds	5.3 pounds

ACKNOWLEDGEMENTS

The authors wish to express their appreciation to Mr. Russell Shoho for the microwave integrated circuit design and to Mr. Raymond Vasta and Mr. Herbert Moore for the synthesizer development.

68.8 db ADDED TO EACH POINT OF THE ORIGINAL CURVE MOVED UP FROM 16 MHz TO 45 Ghz

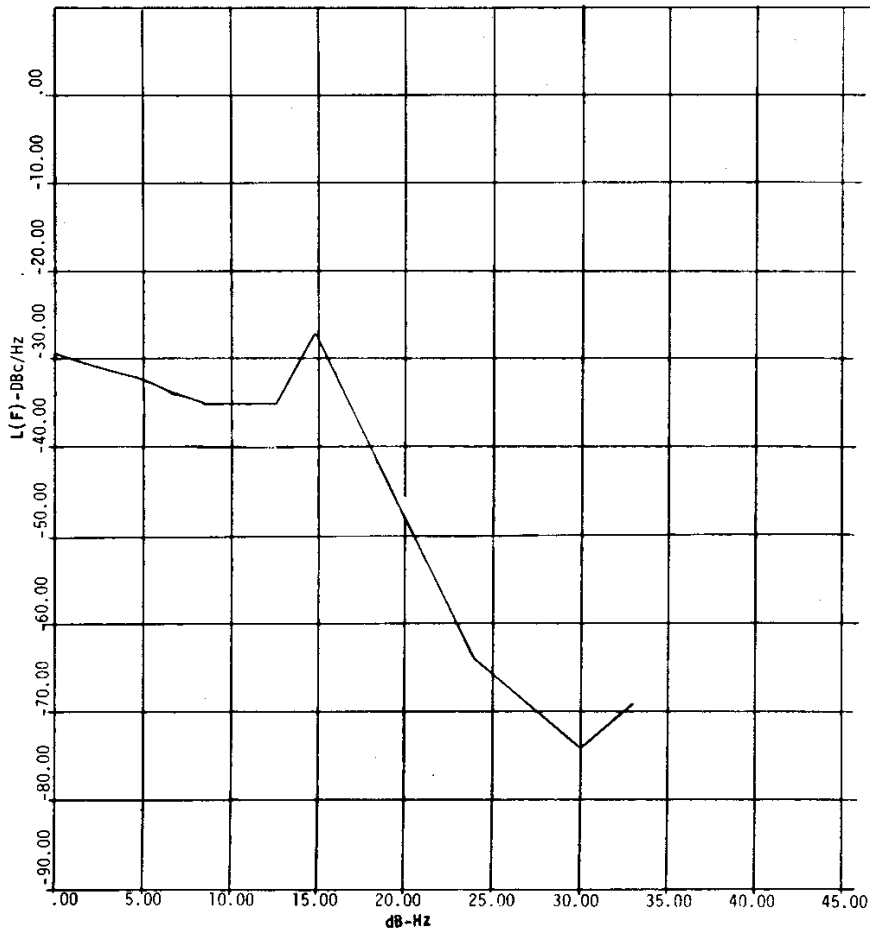

Figure 1. Single Sideband Phaze Noise at 45 Ghz

L(F) IS MEASURED AT 16MHZ AND RAISED TO 450HZ

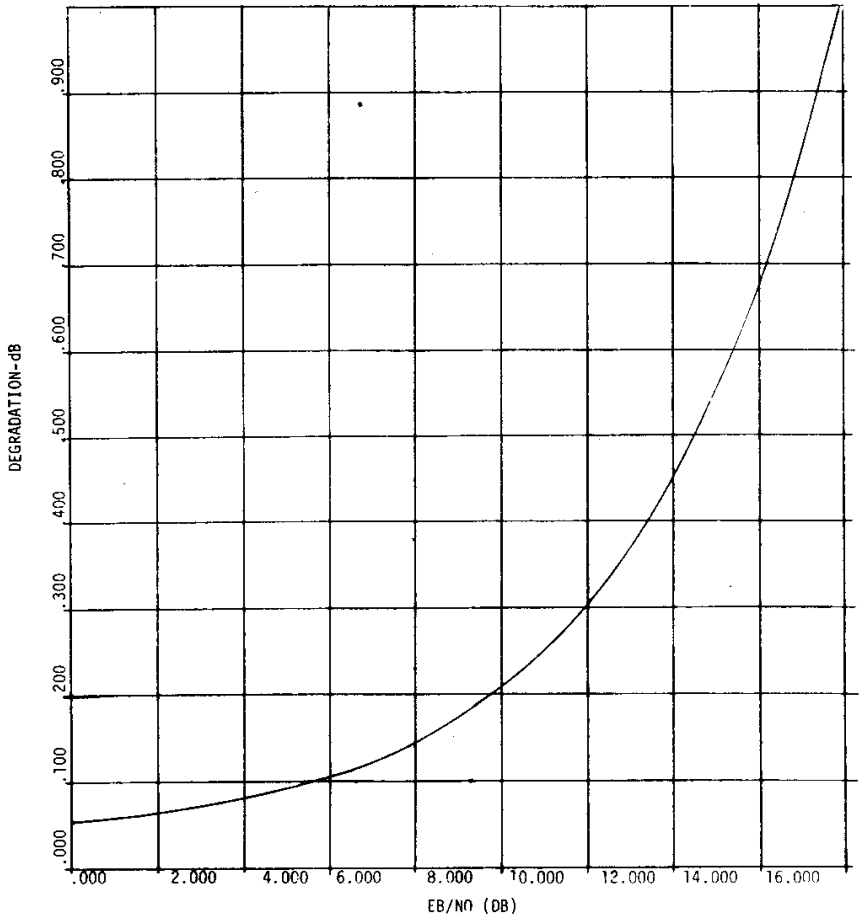

Figure 2. Degradation in EB/NO as a function of EB/NO for given L (f)

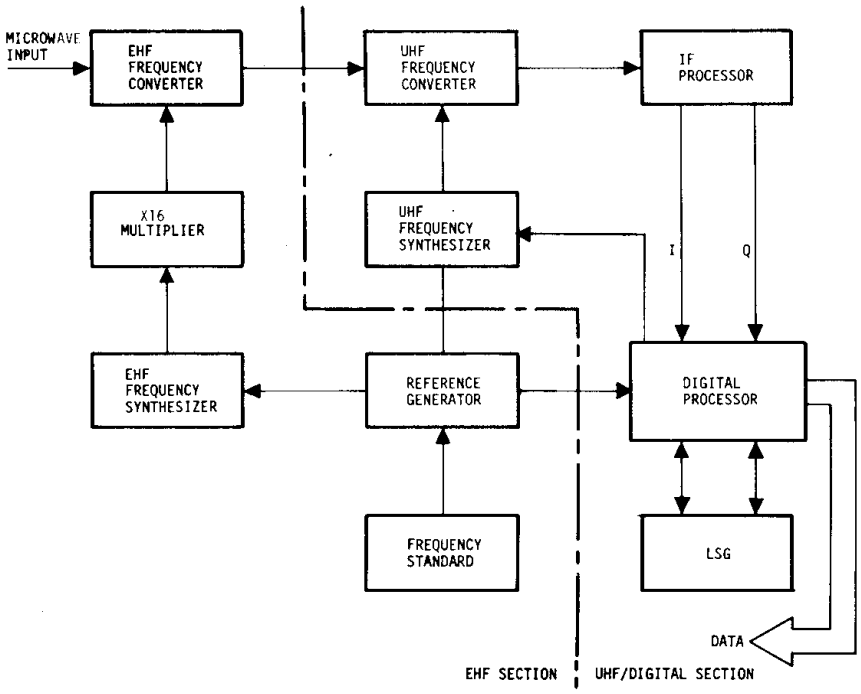

Figure 3. Q-Band Receiving System Block Diagram

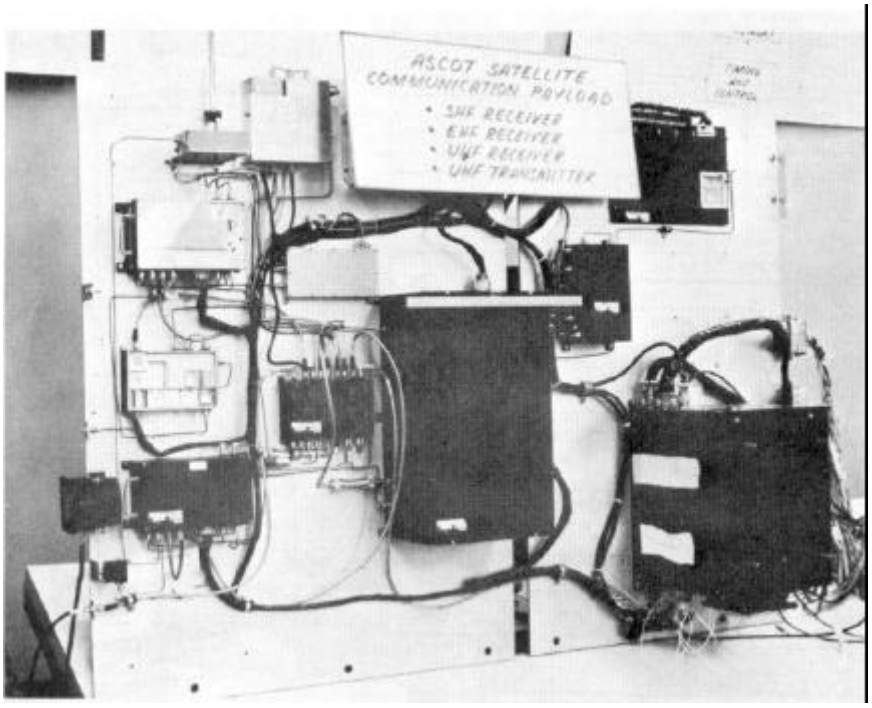

Figure 4. Q-Band Receiving System in Test Configuration

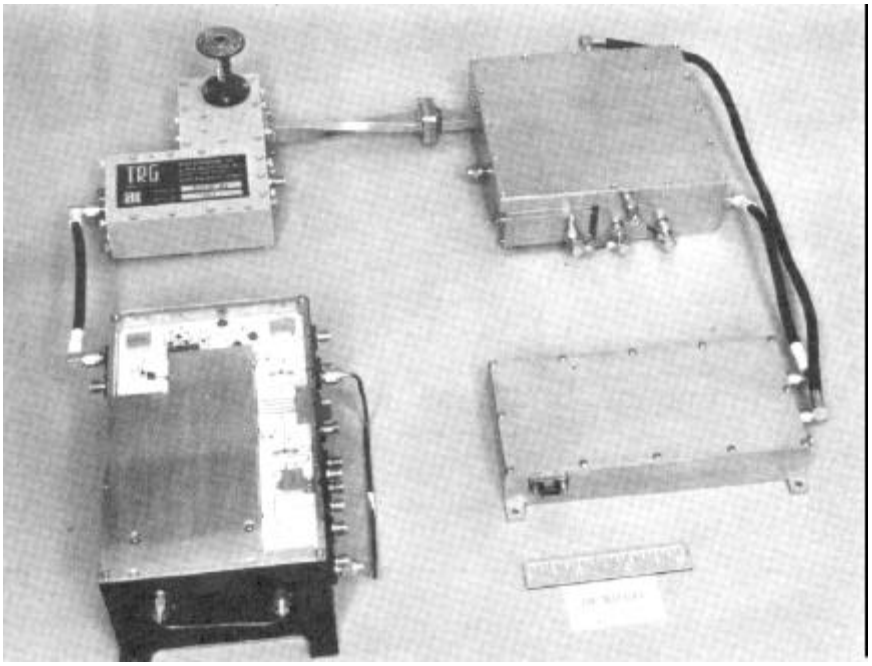

Figure 5. EHF Section of Q-Band Receiver

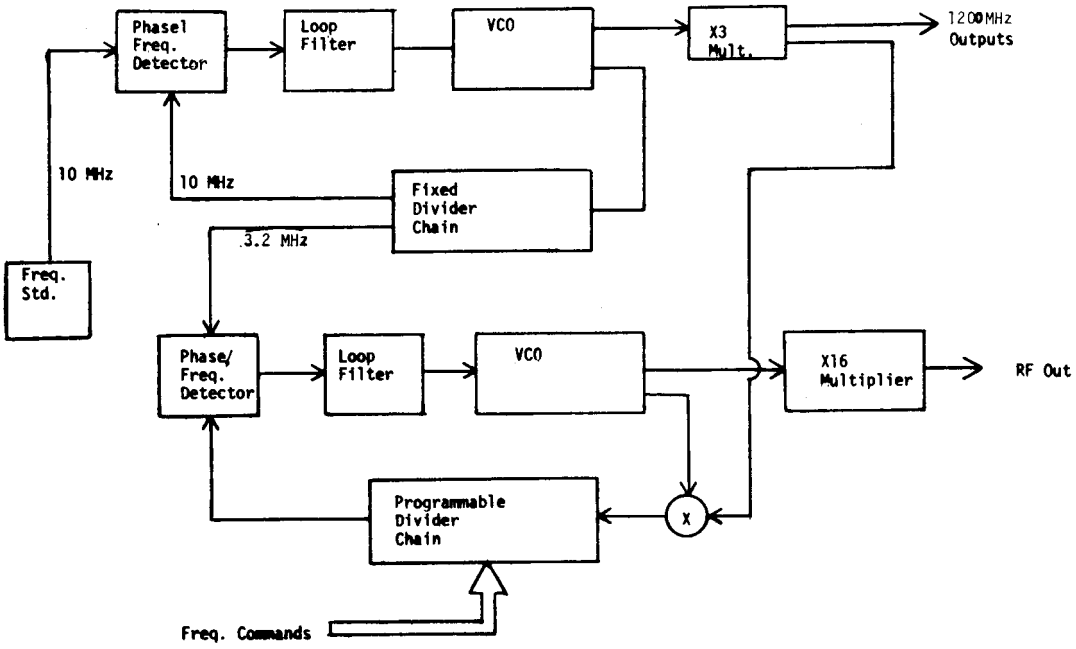

Figure 6. Frequency Synthesizer/Reference Generator Block Diagram

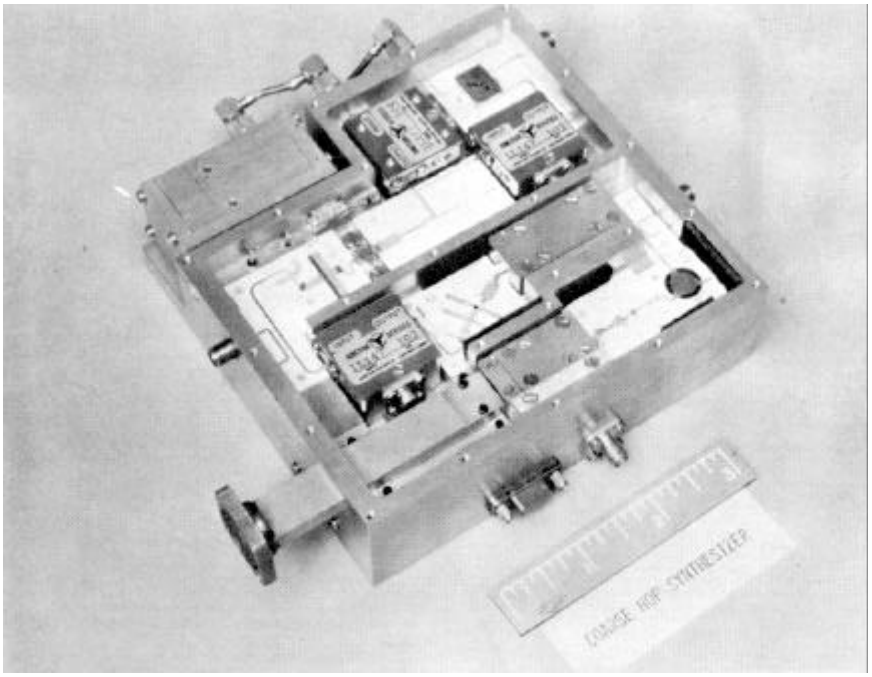

FIGURE 7. FREQUENCY SYNTHESIZER

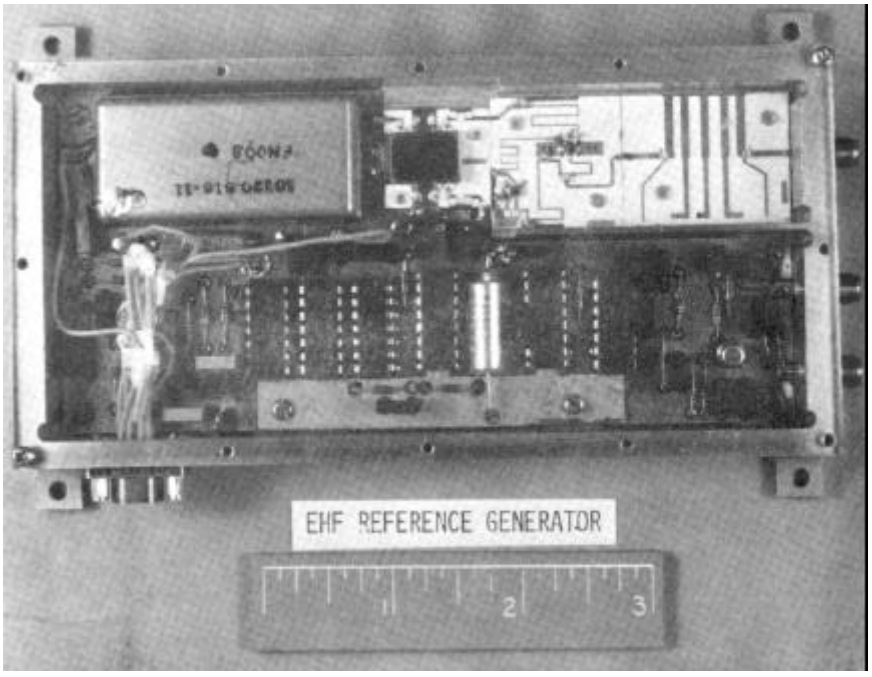

FIGURE 8. REFERENCE GENERATOR

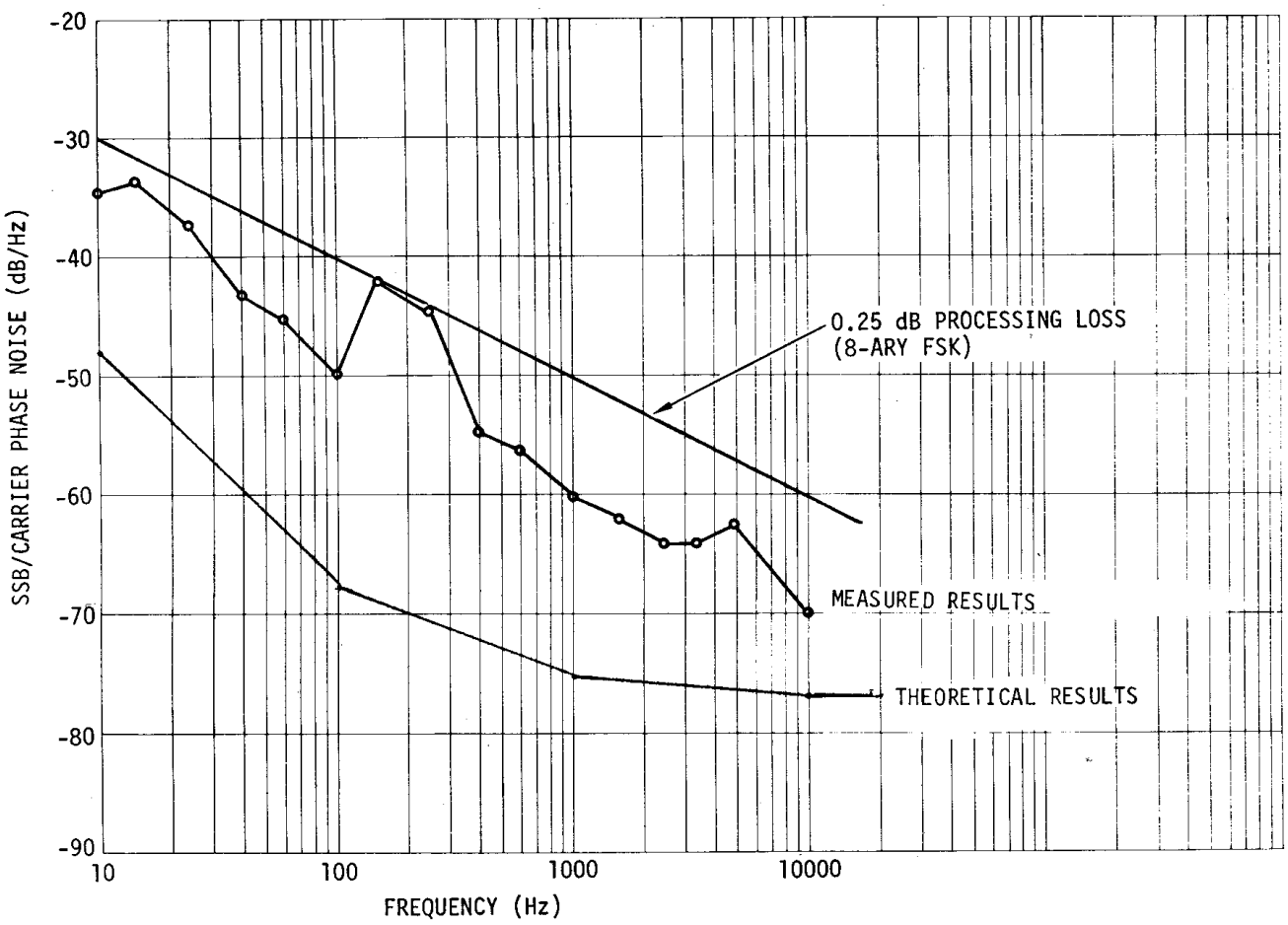

FIGURE 9. LOCAL OSCILLATOR PHASE NOISE VS. 0.25dB PROCESSING LOSS SPECIFICATION