

A SELF-SYNCHRONIZING PSEUDO-RANDOM BIT ERROR DETECTOR

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ABSTRACT

A synchronous pseudo-random bit error detection strategy, incorporating a novel sync acquisition feature, is shown to detect both data and time base errors and to recover sync following such time base errors with no apparent delay, subject to certain error rate constraints. The discussion applies generally to any 2^N-1 pseudo-random sequence. An appendix expands on the linear sequential properties of pseudo-random sequences germane to the implementation of the detection strategy discussed.

INTRODUCTION

Bit error rate (BER) measurements utilizing a pseudo-random sequence (PRS) as test data are commonly used to assess the performance of digital data systems. Such pseudo-random sequences are classically generated by feeding back to the input of a shift register, the weighted Modulo-2 sum of its outputs. This process results in an output sequence 2^N-1 bits in length, where N is associated with the number of shift register stages.

A synchronous PRS bit error detector is one which compares an input PRS against an internally generated reference. The reference is obtained from a PRS generator which has been synchronized to the input data.

Many digital systems encode data in a PCM format either for transmission or storage on magnetic media. Subsequent decoding of the received or reproduced PCM format frequently gives rise to time base errors in addition to data errors. Unless the PRS bit error detector employed to assess the BER of such a system includes means to resynchronize its reference, the occurrence of a single time base error can prohibit further error detection.

A conventional strategy commonly employed to detect the occurrence of a time base error exploits the sudden increase in BER attendant upon loss of sync. The resolution and accuracy of the resulting BER measurement is compromised however, in that accurate error detection is prohibited during the sync loss period.

The following discussion offers a simple alternative to conventional PRS error detection, incorporating a sync detection feature which assures the reacquisition of sync in time to accurately error detect the next bit in succession, given certain error rate constraints. To the user it appears as if sync has been regained with no apparent delay.

The specific bit error detection strategy discussed includes means to count time base errors as distinct from data errors.

OPERATING PRINCIPLES

The operating principles of the error detector to be discussed are based on the linear sequential properties of a PRS. The attached appendix expands upon these properties and presents a simple procedure by which specific weights can be calculated.

A functional block diagram of the synchronous PRS error detector under discussion is shown in Figure 1. Basically, the error detector consists of a Sync Detector, M Bit Delay Register, PRS Reference Generator, and M Bit Delayed Reference Modulo-2 Summer. The Sync Detector monitors the input PRS data for errors manifested as invalid PRS state transitions. Should an input error occur, the Sync Detector provides the PRS Reference Generator with an N Bit sample of error free input bits on which to synchronize. The M Bit Delay Register and N Bit Delayed Reference Summer respectively buffer the input data and reference to permit the Sync Detector sufficient time to synchronize the Reference Generator prior to actual error detection.

Specifically, input PRS data applied to the Sync Detector is shifted through an N bit register whose outputs are weighted and Modulo-2 summed to function as a linear sequential inverse to the original PRS generator from which the input PRS was obtained. So long as the input PRS state transitions occur sequentially, the output of the sync detector remains false.

Assuming the occurrence of a single bit error, the output of the Sync Detector transitions to the true state, indicative of an invalid input PRS state transition. Such invalid state transitions, in general, will continue to be detected until such time as the bit in error is shifted clear of the N bit register.

The first true state output of the Sync Detector arms an M bit Delay Counter/Sync Latch to issue a sync pulse to the Reference Generator M bits delayed from the last true to false transition of the Sync Detector. The sync pulse applied to the Reference Generator parallel loads the contents of the Sync Detector N bit shift register into the Reference Generator shift register.

Since the sync pulse is issued M bits delayed with respect to the last true to false transition of the sync detector, the output of the Sync Detector must be false for M consecutive bit times. For the Sync Detector output to remain false for M bit times implies that M consecutive valid input PRS state transitions have been detected. The Sync Detector shift register thus must contain, with a high probability of success, N error free bits with which to synchronize the reference generator.

The M bit delay associated with acquiring sync is compensated by the signal path delay provided by the M Bit Delay Shift Register. The reference is compensated by the Delayed Reference Modulo-2 Summer which issues a reference PRS M bits delayed with respect to the state of the Reference Generator at the instant of sync acquisition.

The data output of the M Bit Delay Register is Modulo-2 summed with the delayed reference for detection of data errors. Time base errors are detected by an N Bit Magnitude Comparator which compares the sync state or the Sync Detector to the sync state of the Reference Generator at the instant of sync acquisition.

So long as input errors occur no closer together than $N + M$ bits, the M bit signal path delay assures that sync will be reacquired in time to accurately error detect the next bit in succession. Externally it appears that sync is regained without delay, rather than the $N + M$ bit times actually required.

The obvious limitation on this detection strategy is that no more than one input error occur within any $N + M$ period. A calculation of the value of M necessary to establish a given probability of success that valid sync has been acquired is beyond the scope of this discussion. In practice however, a hardware implementation of this detection strategy for $N = 8$, $2^N - 1 = 255$ PRS yielded exceptional results with $M = N = 8$. Thus, the value $N + M$ can be small without appreciable degradation in BER measurement accuracy.

SUMMARY

The operating principles of a synchronous PRS error detection strategy have been discussed, which have been shown to overcome the inaccuracies associated with conventional sync reacquisition techniques in response to time base errors.

APPENDIX

The specific properties of a pseudo-random sequence, german to the design of the synchronous error detector discussed in the text, derive from the study of linear sequences.

It can be shown that for any 2^N-1 pseudo-random sequence, the current output bit is linearly dependent upon the weighted Modulo-2 sum of the N previous bits. That is:

$$1. \quad Y_m = A_1 Y_{m-1} \oplus A_2 Y_{m-2} \oplus \dots \oplus A_N Y_{m-N}$$

where Y_m represents the current bit, Y_{m-i} represents the i^{th} past bit and A_i represents the i^{th} weighting factor. Since there are N weighting factors, an equal number of linearly independent equations must be generated to permit their evaluation. These equations will be identical in form to that of Equation 1, differing only in which set of N bits of the sequence is used. The set of N equations thus generated can be represented most compactly in the following matrix form:

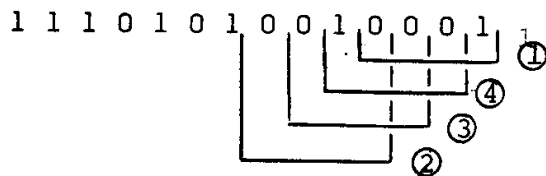
$$2. \quad \bar{Y}_m = |Y_{m-i}| \bar{A}_i$$

where Y_m is an N dimensional vector whose elements are the values of Y_m corresponding to the N sets selected from the sequence. Matrix $|Y_{m-i}|_n$ is an $N \times N$ matrix representing the N sets of coefficients Y_{m-i} of A_i .

Equation 2 can be solved for Y_i very simply. Let the N sets selected from the sequence consist of those containing a single 1 in an order such that $|Y_{m-i}| = I_n$, an $N \times N$ identity matrix. Then $|Y_{m-i}| = |Y_{m-i}|^{-1}$ and equation 2 reduces to:

$$\bar{A}_i = \bar{Y}_m$$

This result provides for a simple procedure by which the weighting factors of any given 2^N-1 pseudo-random sequence can be determined. For example consider the $N = 4$, $2^N-1 = 15$ pseudo-random sequence.



The weighting factors of this sequence can be determined by inspection. First, select 4 sets of 4 bits, each set containing a single 1. Identify these sets corresponding to the columns of identity matrix I_n

$$I_n = \begin{matrix} & \begin{matrix} 1 & 2 & 3 & 4 \end{matrix} \\ \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \end{matrix} & \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \end{matrix}$$

Then simply find the value of Y_m , that is the value of the next bit in the sequence following each set.

$$\bar{A}_i = \bar{Y}_m = [1001]$$

Thus;

$$\begin{aligned} A_1 &= 1 & A_3 &= 0 \\ A_2 &= 0 & A_4 &= 1 \end{aligned}$$

Should a determination of the weighting factors associated with the generation of the sequence in reverse be required, the process is identical except that the order of selection is reversed. By inspection,

$$\bar{A}_i = \bar{Y}_m = [0011]$$

Thus;

$$\begin{aligned} A_1 &= 0 & A_3 &= 1 \\ A_2 &= 0 & A_4 &= 1 \end{aligned}$$

By virtue of the same reasoning that permitted the current bit to be determined by the weighted Modulo-2 sum of the N previous bits, any bit within the sequence can be similarly determined by any consecutive set of N bits. Suppose that it is desired, as in the design of the synchronous error detector discussed in the text, to generate two pseudo-random sequences one displaced from the other by an arbitrary amount. The procedure is identical to that discussed except that Y_m is replaced by Y_{m+j} , where j is the displacement in bits. Referring again to the first example, let $j = 8$, then by inspection

$$\bar{A}_i = \overline{Y_{m+j}} = [1101]$$

Thus,

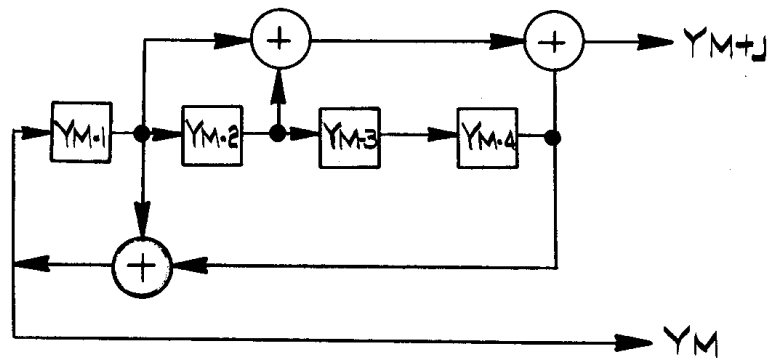
$$A_1 = 1 \quad A_3 = 0$$

$$A_2 = 1 \qquad A_4 = 1$$

The following is a realization of this calculation:

Where;

$\leftarrow j = 8 \rightarrow$
 $Y_m:$ 1 1 1 0 1 0 1 1 | 0 0 1 0 0 0 1
 $Y_{m+j}:$ 1 0 0 1 0 0 0 1 | 1 1 1 0 1 0 1



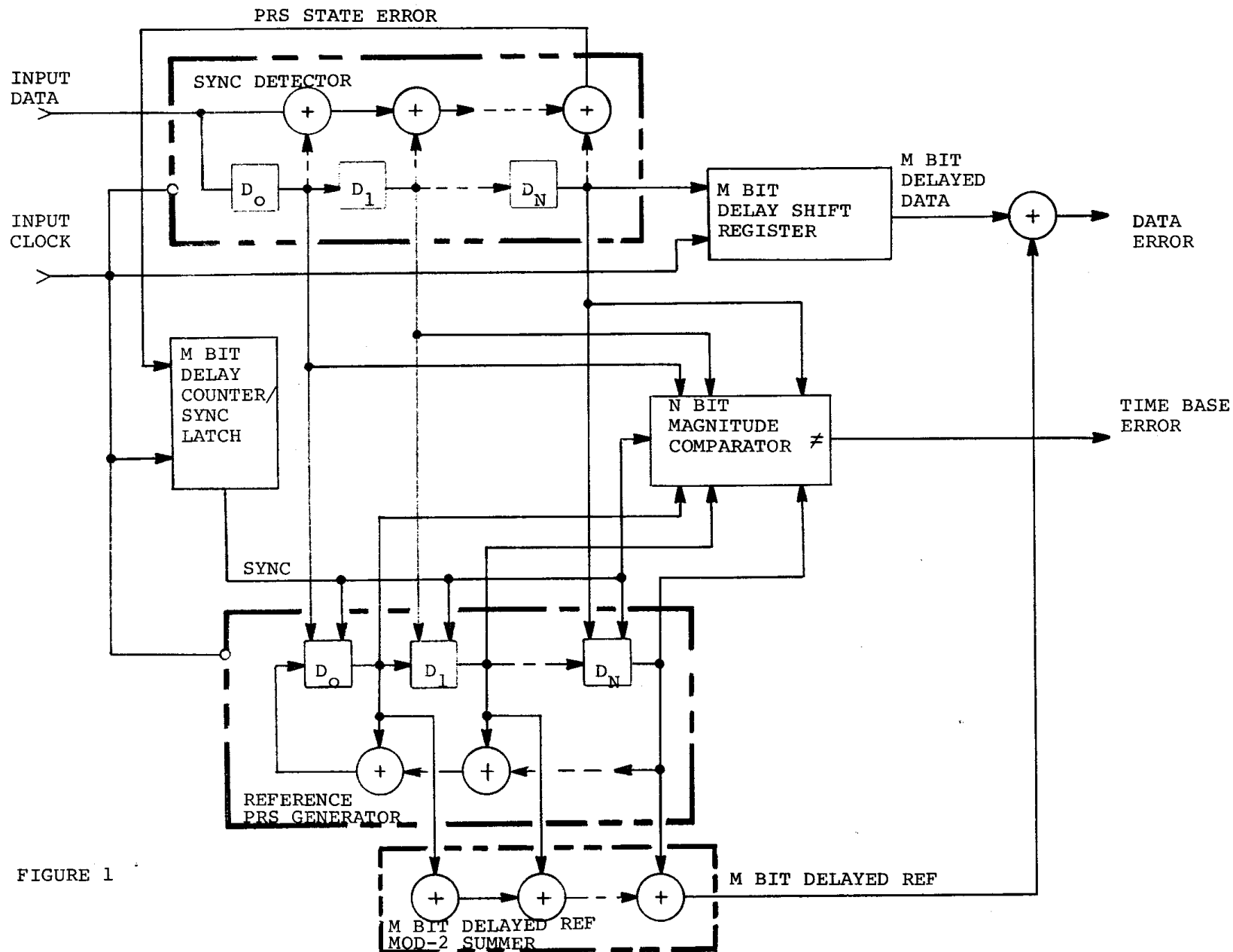


FIGURE 1