# A HIGH SPEED MINIATURE PULSE CODE MODULATION SYSTEM

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## ABSTRACT

Increasing speed and complexity of guidance and target acquisition systems being developed for SDI missile interceptors mandate new performance standards for today's airborne telemetry systems. High bandwidth video data merged with a myriad of high sample rate analog and digital channels have pushed bit rates to 10 MBPS (Mega Bits Per Second) and beyond. These bit rates which are an order of magnitude beyond most telemetry systems in use today, result in the need for a new architecture which facilitates data transfer at these higher rates.

## INTRODUCTION

Format constraints placing analog channels in adjacent word locations complicate the task of acquiring these signals and converting them into digital values. Multiple ADCs (Analog to Digital Converters) and distributed instrumentation amplifiers become necessary to alleviate settling time conflicts resulting from such formatting.

Another trend in today's telemetry systems is decreasing size and weight while accommodating an increasing number of signals to be processed. A higher level of integration becomes necessary to attain these goals, resulting in the combination of hybrid microcircuits and high speed CMOS (Complimentary Metal Oxide Semiconductor) gate arrays packaged on space efficient printed circuit modules.

As encryption of the PCM (Pulse Code Modulation) bit stream becomes more prevalent, users have expressed their desire to integrate the ESP (Encryption Support Package) into the PCM encoder. Traditionally, these packages were stand-alone units requiring the volume of a small PCM encoder.

Resulting from these diverse requirements is the design of a PCM encoder which embodies these characteristics. This paper describes the architecture and design of such a system.

## MEASUREMENT REQUIREMENTS

The High Endoatmospheric Defense Interceptor (HEDI) program has generated a diverse list of measurement requirements which have been accommodated by the Modular PCM Data Processor (MPDP). A summary of the MPDP capabilities follows:

- 160 High Level Analog Signals ( > 5.1 V span)
- 192 Low Level Analog Signals ( 5.1 V span or less)
- 48 Bilevel (Event) Signals
- 48 High Speed Analog Signals
- 112 +10 V Excitation Outputs
- 6 +1 V Excitation Outputs
- 3 Asynchronous Serial Digital Channels
- 1 Synchronous Video Channel
- 6 Precision Analog Buffers
- 2 Independent Power Supplies Providing Red/Black Isolation
- 24 Constant Current Excitation Outputs for Selected High Speed Signals
- 1 Self-contained Encryption Support Package with 10 MBPS Cipher Text Output
- 1 Fiber Optic output with 10 MBPS Plain Text Output

## SYSTEM BLOCK DIAGRAM

A functional block diagram of the HEDI MPDP is given in Figure 1. It should be noted that a single master module controls all other data-gathering modules. The system is expandable with up to 31 modules controlled by a single bus.

The master module contains EEPROMs (Electrically Erasable Programmable Read only Memories) that are programmed by an IBM AT which includes a custom plug-in card for unit interfacing at distances up to 50 feet. All data collection modules are connected to common address and data busses. Two power supplies provide electrical isolation of red and black power while mechanical partitioning provides isolation of radiated signals between the two sections. Excitation power is derived from the black supply.

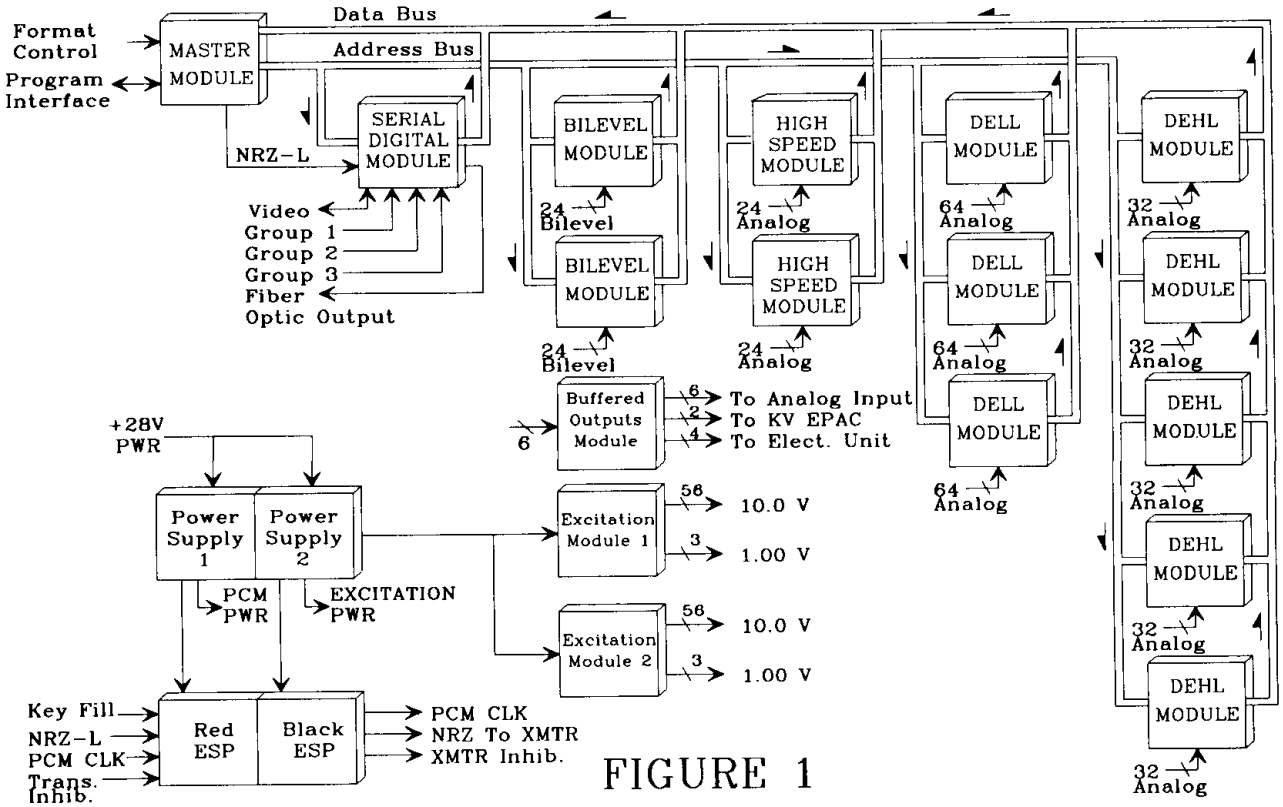


FIGURE 1

MPDP BLOCK DIAGRAM

**DATA BUS ARCHITECTURE**

Originally the HEDI PCM system was specified as processing analog and digital signals utilizing small individual PCM encoders distributed throughout the vehicle stages. This requirement was eliminated as the system design evolved, but not before a unique and flexible master/remote protocol was developed to simplify data transfer at relatively high bit rates. Figure 2 illustrates the bus message structure and request/response protocol developed for this purpose.

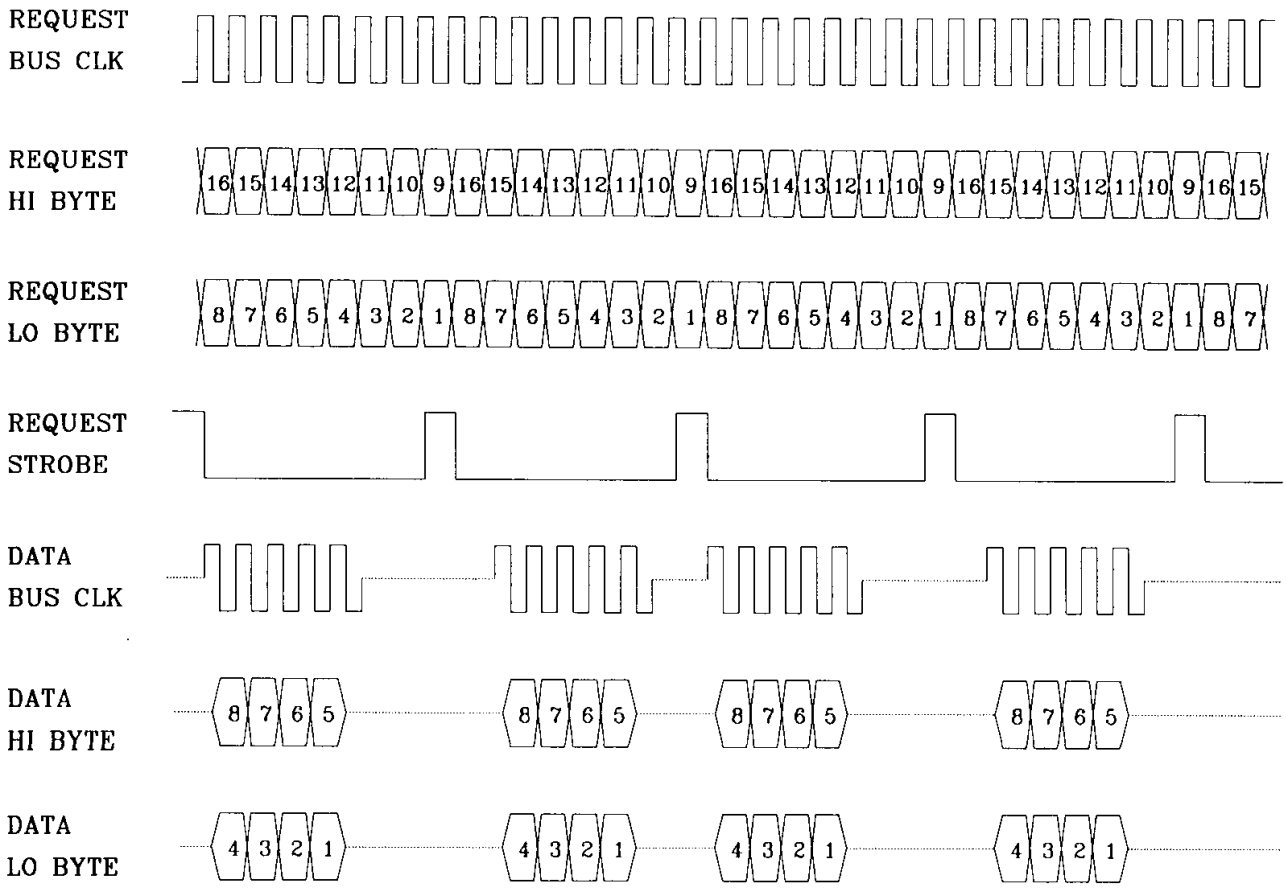


FIGURE 2
BUS PROTOCOL

The request and reply busses each consist of 4 lines; high-byte, low-byte, clock and word strobe. The request bus is connected to all modules. Continuous requests are transmitted from the master to every remote module. The data rate of the request bus is synchronous to the PCM bit rate resulting in eight-bit bytes per PCM word time on each bus. Combining the high and low bytes results in a sixteen-bit request word.

All addressed modules are independent data acquisition systems which derive their system timing from the request bus clock and word strobe signals. Modules containing ADCs are referenced to a common 5.120 V source internal to the unit.

Every module responds to it’s unique ID following a fixed common delay with two data nibbles, each containing four bits of data. Tagging each response with a module ID is not necessary as the processing delay is uniform and predictable throughout all modules.

Due to unequal address and data path lengths between modules, responses from the various modules occur out of phase with the request bus clock and each other. These phase differences between various responses and the request bus have been exaggerated in Figure 2 for illustrative purposes. At high bit rates the delays can become a significant portion of a bit period. For this reason, the data bus was split into two busses, each transmitting four bits per response. This architecture assures that no overlap occurs between responding modules which could garble messages received by the master module. The clocks and word strobes which transfer the data into the master module are local versions generated by each responding module to guarantee no skew due to varying distances from the master to remote modules.

By utilizing this bus architecture, remotes can communicate with a master module over lengths of cable with round-trip delays approaching 2 PCM bit intervals. Alternately, with all modules contained within one unit, proper protocol can be maintained at bit rates beyond 20 MHz.

**MASTER MODULE**

The master module controls all addressed modules over an address bus as previously described. The heart of the module is the master control gate array. This array utilizes over 4000 gates to provide the following functions:

A) Program 32K X 24 EEPROM format memory

B) Read format memory and generate address bus requests for the appropriate data collection modules

C) Receive data responses from the addressed modules via the data bus

D) Generate a PCM output stream from the information contained by the EEPROM memory and the data responses from the addressed modules

In addition to the logic contained in the master control gate array, the master module incorporates an EPLD (Electrically Programmable Logic Device) to translate mission mode control lines external to the unit into format address fields and unique mission mode words which are inserted into the PCM bit stream. Eight formats, each

containing 4K of EEPROM data are available to satisfy diverse mission requirements from ground checkout through flight termination. Jumper options are available to accommodate 4 formats, each containing 8K of EEPROM data, 2 formats of 16K length or 1 format which occupies the full 32K block of memory. The EPLD was chosen to satisfy mission-specific format mapping requirements rather than incorporating the mapping in the master control array logic.

**ANALOG PROCESSING**

Analog signals processed by the MPDP fall into three categories with the following characteristics:

I High Level ( voltage span > 5.1 V )

II Low Level ( voltage span < 5.1 V )

III High Speed ( sample rate > 7000 samples / second and voltage span < 5.1 V )

Category I signals are handled by 5 DEHL ( Double Ended High Level ) modules. Each module has a capacity of 32 channels giving the MPDP a total high level analog capability of 160 channels.

Category II signals are processed by 3 DELL ( Double Ended Low Level ) modules. Total DELL unit capacity is 192 channels, each module accommodating 64 high level signals.

Category III signals comprise all shock, vibration and pressure measurements. The shock and vibration channels are unique in that they provide the hybrid transducers with a constant current excitation. The transducers superimpose an AC signal onto the constant current source lines. Capacitors block the DC excitation while passing the AC component on to the amplifier for further processing. Pressure channels are straightforward multiplexed differential inputs feeding an instrumentation amplifier. These two types of inputs are present on each high speed module, 12 AC coupled and 12 DC coupled per module. Two high speed modules accommodate a total of 48 channels.

## CUSTOM HYBRID DEVELOPMENT

Volume and weight constraints placed upon the MPDP, along with the large number ( more than 400 ) of analog channels require the utilization of hybrid microcircuits to perform the analog processing tasks. Two hybrid types were developed for this purpose, a 16 channel differential multiplexer / amplifier and a 4 channel multiplexer / amplifier / ADC (Analog to Digital Converter).

Figure 3 is a block diagram of the 16 channel multiplexer / amplifier. All channels are overvoltage protected with resistor/diode networks. Two 8 channel differential multiplexers comprise the front end. A second tier multiplexer selects between the two front end multiplexers. The second tier is arranged such that any differential pair of 16 channels can be selected, or any of the 32 individual channels can be selected and referenced to ground. A monolithic instrumentation amplifier follows the second tier and is software programmable with four gains. The output of the amplifier can be offset by a bipolar DAC (Digital to Analog Converter) within a ± 5 V range. All address, gain and offset bits are latched and share a common bus on each module.

Once the high level and low level analog input signals have been multiplexed and conditioned by the 16 channel multiplexer / amplifier, the single-ended PAM (Pulse Amplitude Modulation) stream is directed to a 4 channel multiplexer / amplifier / ADC for further processing. Figure 4 depicts the block diagram of this hybrid microcircuit. Unlike the 16 channel hybrid, the 4 channel device offers no input overvoltage protection. The rationale for this omission is the increase in performance necessary to process high speed analog signals, along with the fact that an overvoltage condition can not exist at the inputs of the 4 channel device when it follows the 16 channel hybrid. Since both hybrids operate from a common supply it is not possible to exceed a supply rail on an amplifier input.

High speed modules eliminate the 16 channel hybrids, utilizing 6 of the faster 4 channel hybrids per module to accommodate 24 high speed signals per module. Each channel is capable of sampling up to 140K SPS (Samples Per Second) due to a settling time of 7 microseconds between channels.

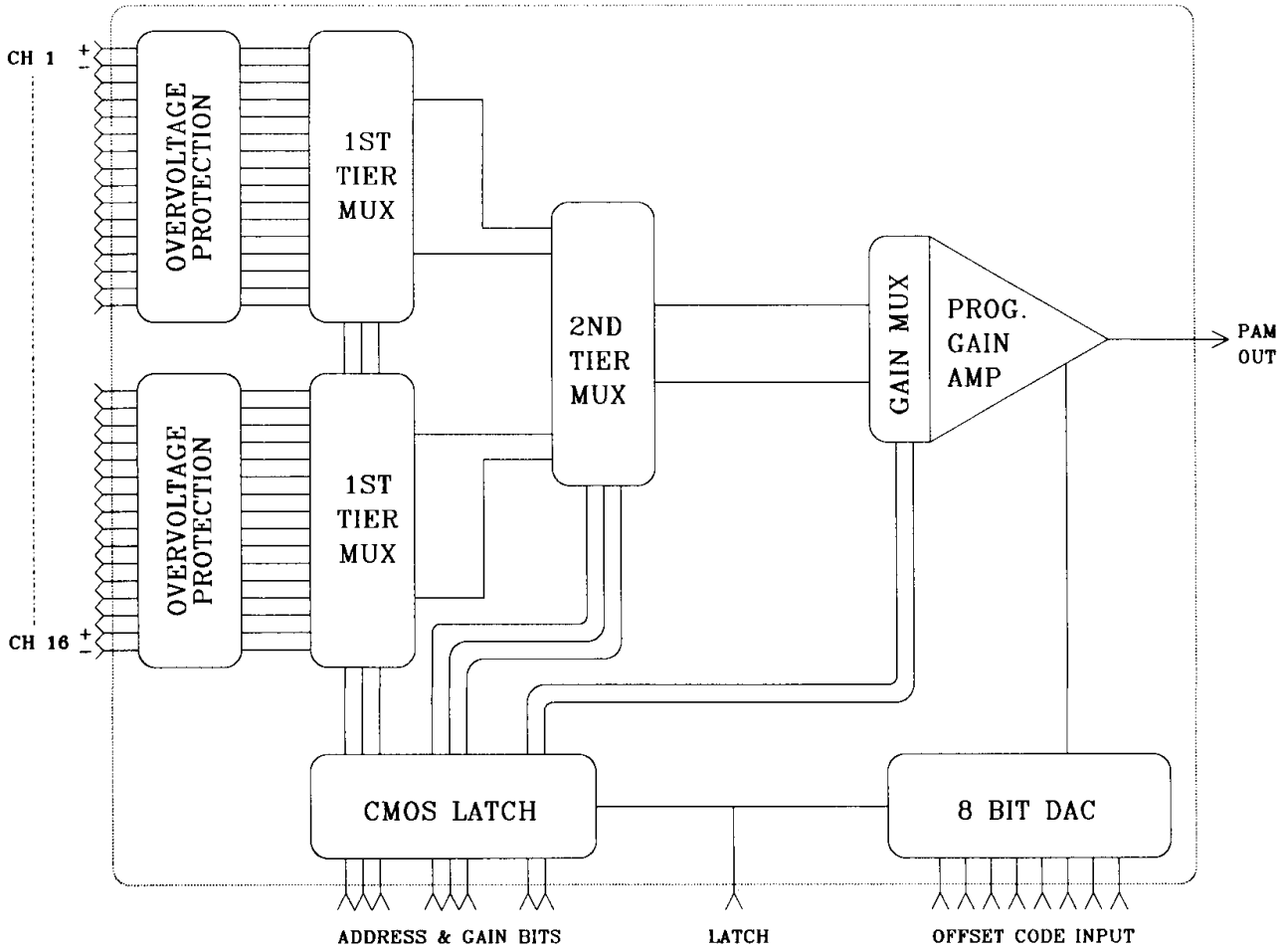


FIGURE 3
16 CHANNEL MUX/AMP BLOCK DIAGRAM

**BILEVEL PROCESSING**

Bilevel (or event) channels are processed by two modules, each accommodating 24 discrete channels. The channels are arranged in groups of 8 per PCM word. The threshold of each channel is independently set via select resistors arranged in a Wheatstone bridge configuration. Firm logic (an EPLD) is incorporated on each module to provide either tracking or latching operation for each individual bit. The latching feature is particularly useful in detecting the occurrence of a glitch, as any pulse above the preset threshold which is 20 nanoseconds or more in duration is permanently captured. The event is erased only by returning to Format 0, or by removing prime power.

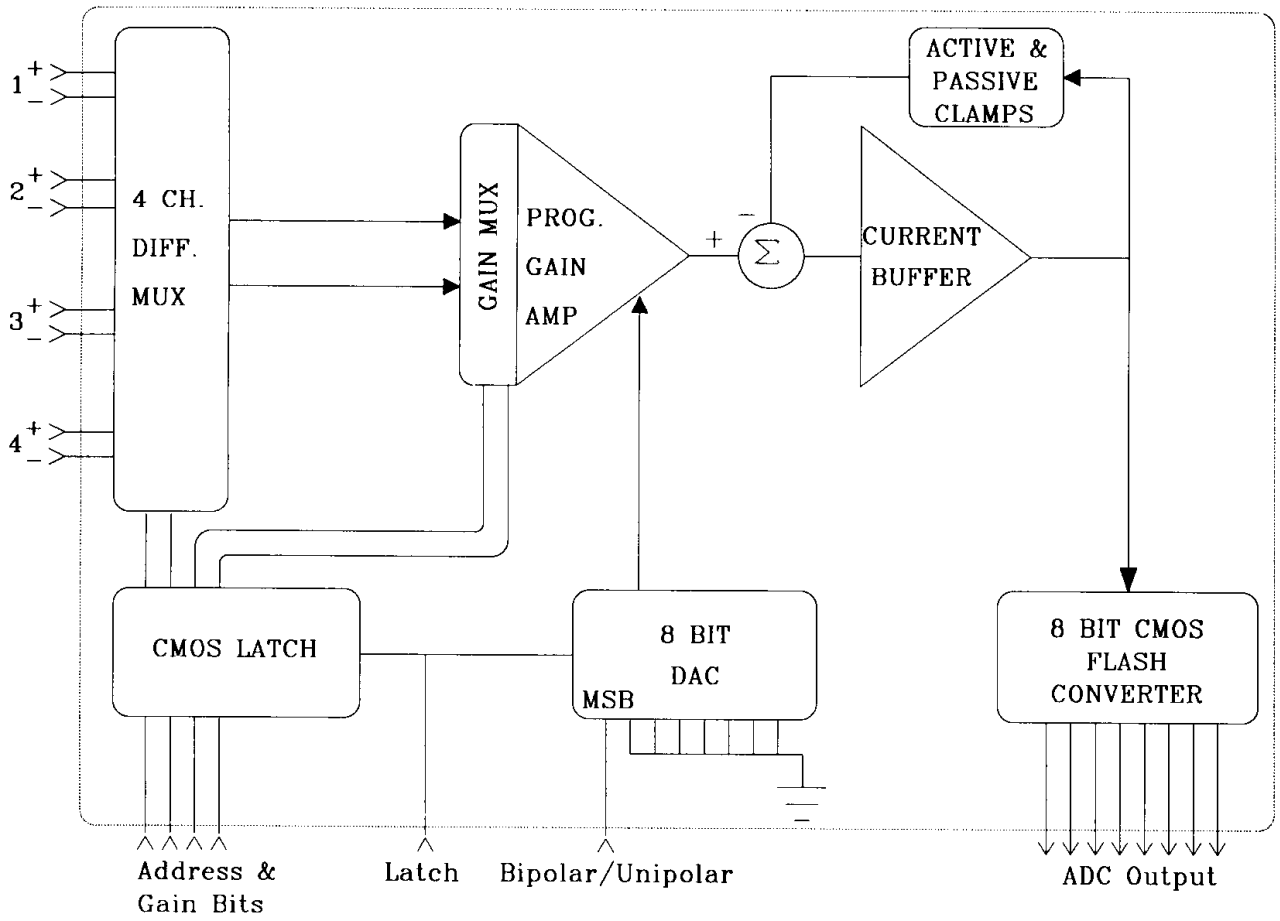


FIGURE 4
4 CHANNEL MUX/AMP/ADC BLOCK DIAGRAM

**SERIAL DIGITAL MODULE**

The serial digital module depicted in Figure 1 accommodates 4 serial digital inputs, 3 of which are asynchronous and one which is synchronous. The asynchronous sources originate from the guidance computer onboard the kill vehicle, while the synchronous data is produced by an IR (Infra-Red) seeker. All asynchronous data is inserted into the PCM bit stream slightly faster than it is received, eliminating the possibility of data loss. Three asynchronous subframes result within a PCM major frame. Video data is synchronously transferred to the MPDP at one-half the PCM bit rate, and is output in a synchronous subframe within the PCM major frame.

A non-related function resides on the serial digital module, namely a fiber optic transmitter. Plain text is transmitted over a fiber optic link to facilitate vehicle checkout prior to launch. Implementing a fiber optic link for plain text transmission greatly simplifies TEMPEST requirements for

non-emanating secure data transmission. An added benefit is the capability of monitoring the data output from a distance of over 1.6 kilometers (1 mile).

**ENCRYPTION SUPPORT PACKAGE**

The encryption device is physically resident within the MPDP ESP, and receives plain-text data from the master control module. Encrypted data crosses the RED/BLACK boundary, and is pre-mod (pre-modulation) filtered prior to interface with the S-band transmitter. The pre-mod filter is a four-pole linear-phase filter constructed as a two-stage L/C filter network with equal input and output terminations.

The crystal oscillator circuit has been physically located in the BLACK section of the ESP to simplify the TEMPEST requirements of the support package. Locating the clock circuitry in the BLACK section eliminates the need for special circuitry (phase-lock techniques) in crossing the RED/BLACK boundary, since the clock source is physically resident in the BLACK section.

A transmitter-inhibit function has been incorporated into the ESP to preclude operation of the S-band transmitter during key-variable load operations, and under control of an external-inhibit interface line.

The ESP also contains a pair of lithium batteries used to maintain the key-variables and checkword loaded during a fill operation. The batteries are located external to the ESP section, and a separate unit connector allows the batteries to be externally activated or deactivated under external jumper control.

**SUMMARY AND CONCLUSIONS**

To meet today’s demands for high-speed, compact telemetry systems, an approach which embodies ASIC (Application Specific, Integrated Circuit) and hybrid microcircuit technologies becomes necessary. Assembly time and board-level checkout for each unit is greatly reduced, primarily due to troubleshooting being performed by the hybrid vendor. Functions once performed by printed circuit assemblies are now the domain of the hybrid microcircuit.

As analog ASICs mature to the performance levels of discrete components available today, most hybrid microcircuits employed for analog functions will be displaced much the same as digital hybrids were earlier in this decade. This evolution will greatly reduce the cost of analog signal processing, as monolithic solutions are almost always less expensive than their hybrid counterparts.