VERSATILE 1553 MUXBUS INTERFACE

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ABSTRACT

This paper presents a 1553 Muxbus Interface which can acquire data, selectively, from up to 3 redundant busses and process it for different airborne or ground test applications.

The Interface is built using up todate electronic technology in order to overcome the problems encountered in 1553 protocol decoding and to insure proper data integrity.

INTRODUCTION

Modern Aircraft testing requires data acquisition of large quantities of parameters from airborne electronic systems such as weapon delivery, navigation and flight control. Generally these systems communicate through serial links, using complex protocols such as the Mil 1553 and require special equipment for data recording, transmission and decommutation.

I.A.I. Engineering Test Center has developed a special Muxbus Interface which can be connected to up to 3 1553 Muxbuses. Its main functions are: data reception and protocol decoding, programmed data selection and output formatting for various communication schemes.

SYSTEM APPLICATIONS

This interface can be configured to operate in various applications, see figures 1 and 2A through 2C.

- As a slave unit to an existing PCM encoder

This configuration is suitable for Muxbus data transmission or recording, after it has been merged with data issued from various devices within a main PCM data acquisition system.

- As a synchronous PCM stream for separate 1553 data recording or transmission.

- As a universal PCM decom. type stream for data acquisition and processing using a Telemetry Computer.

In the last two configurations, data can be selected dynamically. This allows the playback of tapes, where Muxbus has been recorded either during flight simulation or during real flight tests. They can also be used for Avionics Systems Integration and debugging, where the user is interested in monitoring and analysing different sets of data and requires fast setups between runs.

SYSTEM DESCRIPTION

The block-diagram im fig.3 depicts the basic functions of the Interface.

A 1553 Front-end is dedicated to each set of buses (primary and redundant) and includes receivers, protocol decoding circuits, a message preselection Microprocessor and a message dual port buffer.

The Front End uses a Z8000 16 bit microprocessor and special gate arrays for protocol decoding. The microprocessor uses preselection tables in order to filter all unwanted messages. This is important for example, in the elimination of all the overhead traffic used in the polling protocol.

The message buffer is a dual port memory accessible by both the preselection and the message sorting microprocessors. It is filled on a cycling basis, with the first location always containing a command word. As part of this process, an index register, pointing to the current address, is continually updated.

MESSAGE SORTING MICROPROCESSOR (MSM)

The MSM, which is an Intel 80196 with 8k EPROM and 8k RAM, tracks the message buffer pointer and locks on message

boundaries. Every command/status word is checked and if the corresponding location in the look-up sorting table includes a destination address, the current message is transfered to the output buffer.

Sorting can be carried out using either a single command word as a key or through a combination of a command and a single data word. The latter type of data selection is used to decode 1553B extended protocols, where a message is identified by two keys: the command word and the first data word in the message, which is used as a subaddress.

When the interface is used in the gated clock communication type configuration, the sorting microprocessor carries out word selection, in addition to message sorting. Using a word selection setup in its shared memory, it only sends selected parameters, from selected messages to the output buffer.

Data Integrity is maintained by treating each message as an indivisible unit during its transfer from the message buffer to the sorting microprocessor and by disabling interrupts during the transfer.

Messages selected by the message sorting processor are stored in the output buffer at pretermined locations. Each output message is structured as per fig. 4

Each message is preceded by an eight word header which completely identifies the message, including the word count, the bus origin(primary or backup), the mode command, the transmit or receive status and any information about errors encountered.

A 32 bit real time clock, with microseconds resolutions, provides proper time synchronization.

The output buffer is composed of dual ported random access memories accessed by the sorting microprocessor and by the PCM interface and data is therefore available to the PCM Encoder whenever it needs it.

PCM INTERFACE

According to the required application, either a slave or master or PCM decom. interface can be used.

SLAVE INTERFACE

This option allows selected data stored n the output buffer to be routed to a host master PCM encoder for transmission and/or recording together with other types of parameters. Data transfer is under control of the host device. Different timing schemes can be accomodated including the serial address/serial data format of the AYDIN VECTOR PDS 7000 series or the gated clock/serial data format adopted by many manufacturers of PCM encoders.

If the first approach is employed the host PCM encoder can randomly address any location in the output buffer, whereas using the other approach the output buffer is emptied, sequentially, by the host device from the first location to the last. In either case the interface requires the PCM frame pulse as a command to the sorting microprocessor to refresh the output buffer.

The Slave Interface is implemented using a serial to parallel converter for the serial address input and a parallel to serial converter for the serial data output.

If the gated clock type of communication is selected, the output buffer is emptied using a sequential address from a counter which is incremented by a derivation of the gated clock, and reset by the frame pulse.

The bit rate for data transfer to the PCM encoder is up to 1 Mbit per second.

MASTER INTERFACE

This interface was designed for applications where 1553 Muxbus data has to be transmitted/recorded separately, and decommutated using standard telemetry equipment.

It includes a data formatter which empties the output buffer sequentially to a FIFO, adding synchonization words at the end of each frame. An internal timing circuit provides the PCM bit rate and a generated frame pulse interrupts the message sorting microprocessor, initializing the output buffer refresh cycle.

PCM DECOM. INTERFACE

This option is similar to the master interface option. The only difference is that data is outputted as parallel words accompanied by both the word and frame strobes. This simulates the output timing of a standard telemetry PCM decommutation for processing by a host computer or data handling using telemetry demultiplexers and displays.

The master and PCM decom. type interfaces output data to external devices at up to 50 kwords per second (16 bits words) with higher rates available if required.

SETUP/DISPLAY MICROPROCESSOR

The Master and decom. type interfaces use an Intel 8751 microcontroller for the the following tasks:

- Receiving setup records from an external device, through an RS232 line.

- Passing this setup to the message sorting microprocessor, using shared memory.

- Logging on selected data for local monitoring, using an external device, such as a CRT or computer.

PACKAGING

The airborne slave/master versions are packaged in rugged boxes as shown in fig. 5.

The ground versions can be assembled in rack mount units.

CONCLUSION

Aquisition and decommutation of data from the 1553 Muxbus has become a major need in ground systems integration and flight test of aircraft avionics systems. The 1553 Muxbus Interface, described above, can be used as a versatile tool to implement the data handling tasks required in these type of projects. It uses state of the art technology in order to insure proper protocol decoding and data integrity, retaining the data formats and communication schemes well known by PCM systems users.

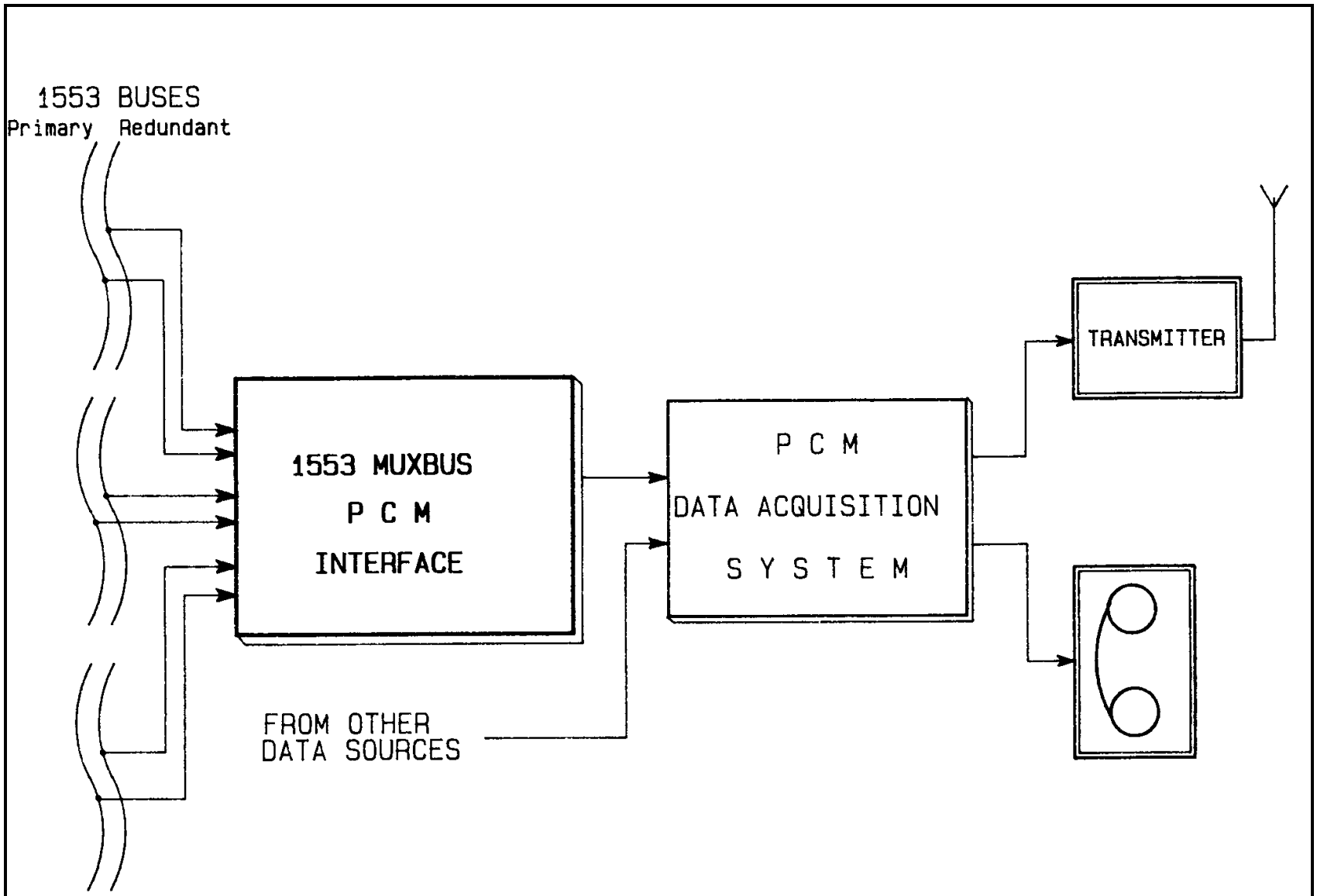
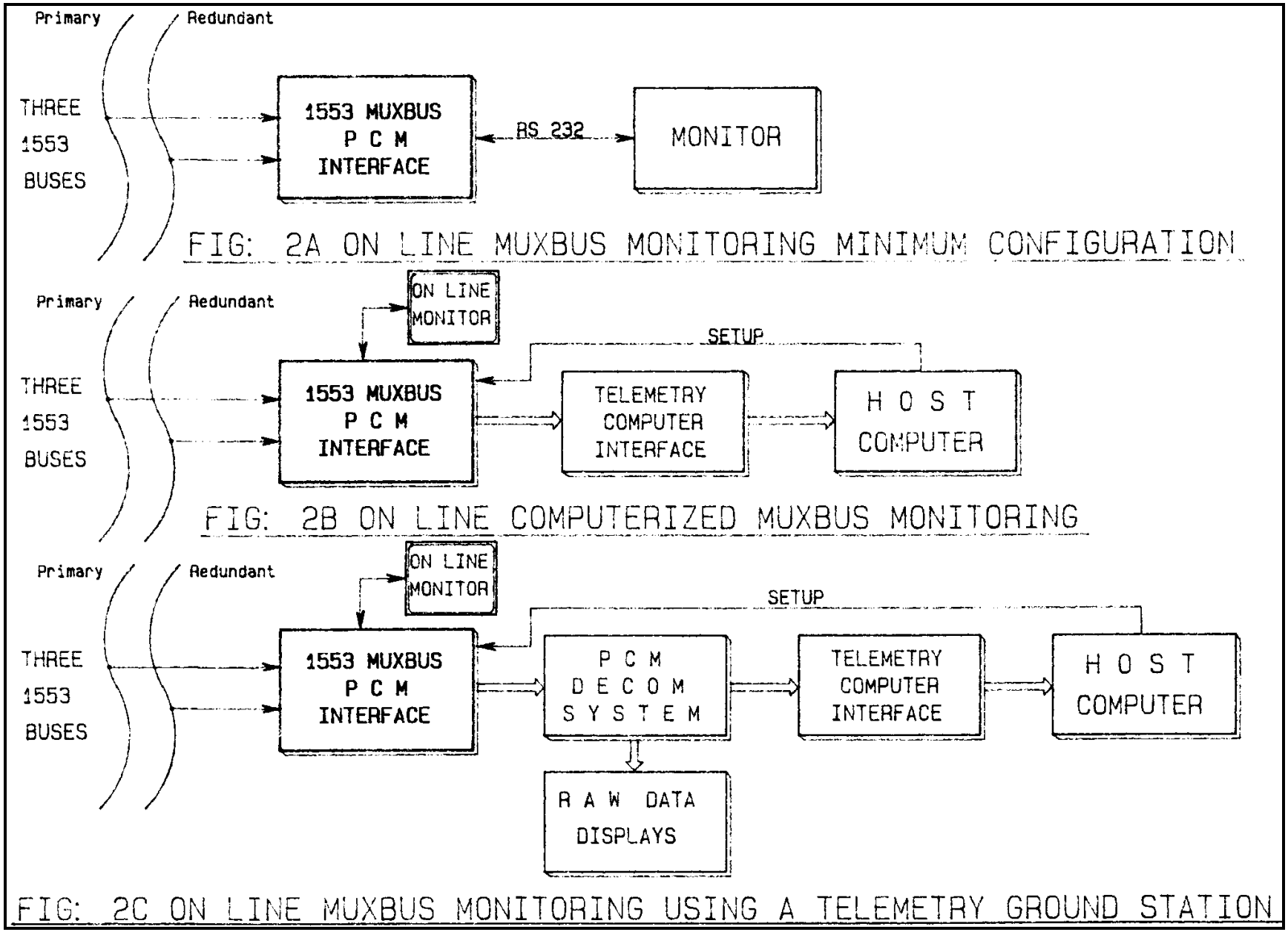


FIG: 1 1553 MUXBUS FLIGHT TEST AIRBORNE DATA ACQUISITION SYSTEM


Primary
Redundant
THREE
1553
BUSES
1553 MUXBUS
P C M
INTERFACE
RS 232
MONITOR
FIG: 2A ON LINE MUXBUS MONITORING MINIMUM CONFIGURATION
Primary
Redundant
ON LINE
MONITOR
SETUP
THREE
1553
BUSES
1553 MUXBUS
P C M
INTERFACE
TELEMETRY
COMPUTER
INTERFACE
H O S T
COMPUTER
FIG: 2B ON LINE COMPUTERIZED MUXBUS MONITORING
Primary
Redundant
ON LINE
MONITOR
SETUP
THREE
1553
BUSES
1553 MUXBUS
P C M
INTERFACE
P C M
D E C O M
S Y S T E M
TELEMETRY
COMPUTER
INTERFACE
H O S T
COMPUTER
R A W DATA
DISPLAYS
FIG: 2C ON LINE MUXBUS MONITORING USING A TELEMETRY GROUND STATION

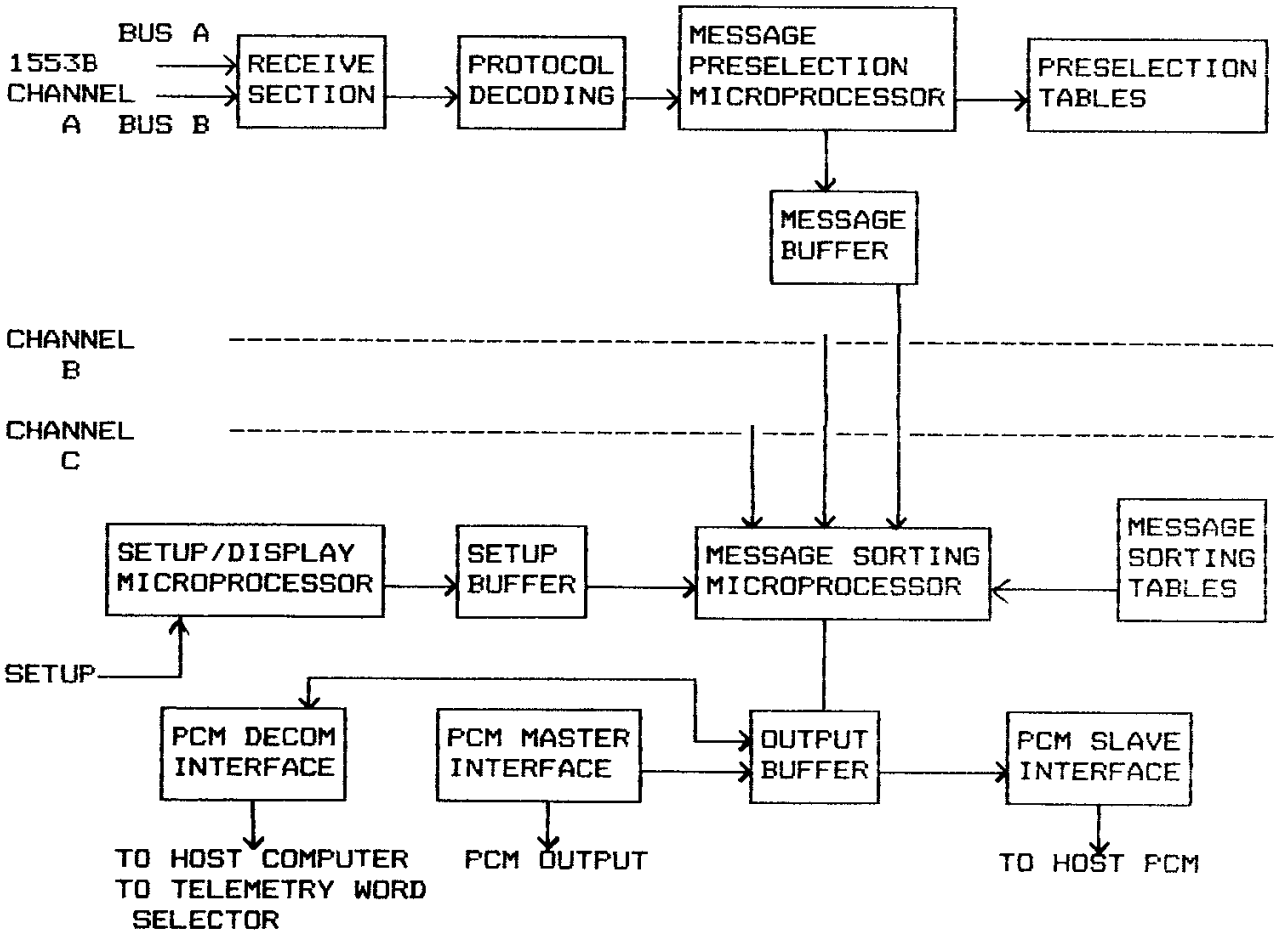


FIG.3 1553 MUXBUS INTERFACE SYSTEM BLOCK DIAGRAM

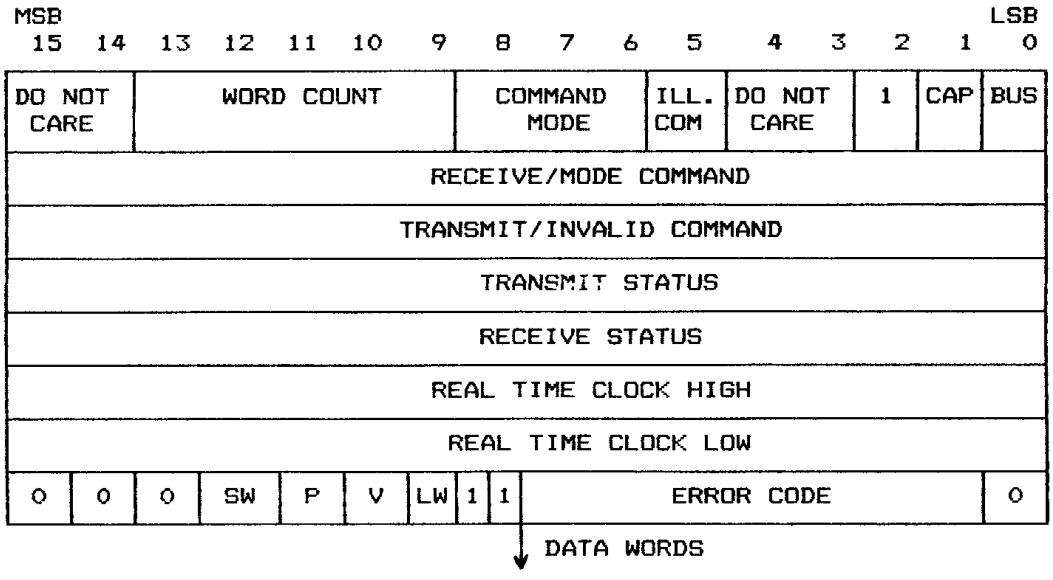


FIG. 4 STRUCTURE OF MESSAGE IN OUTPUT BUFFER

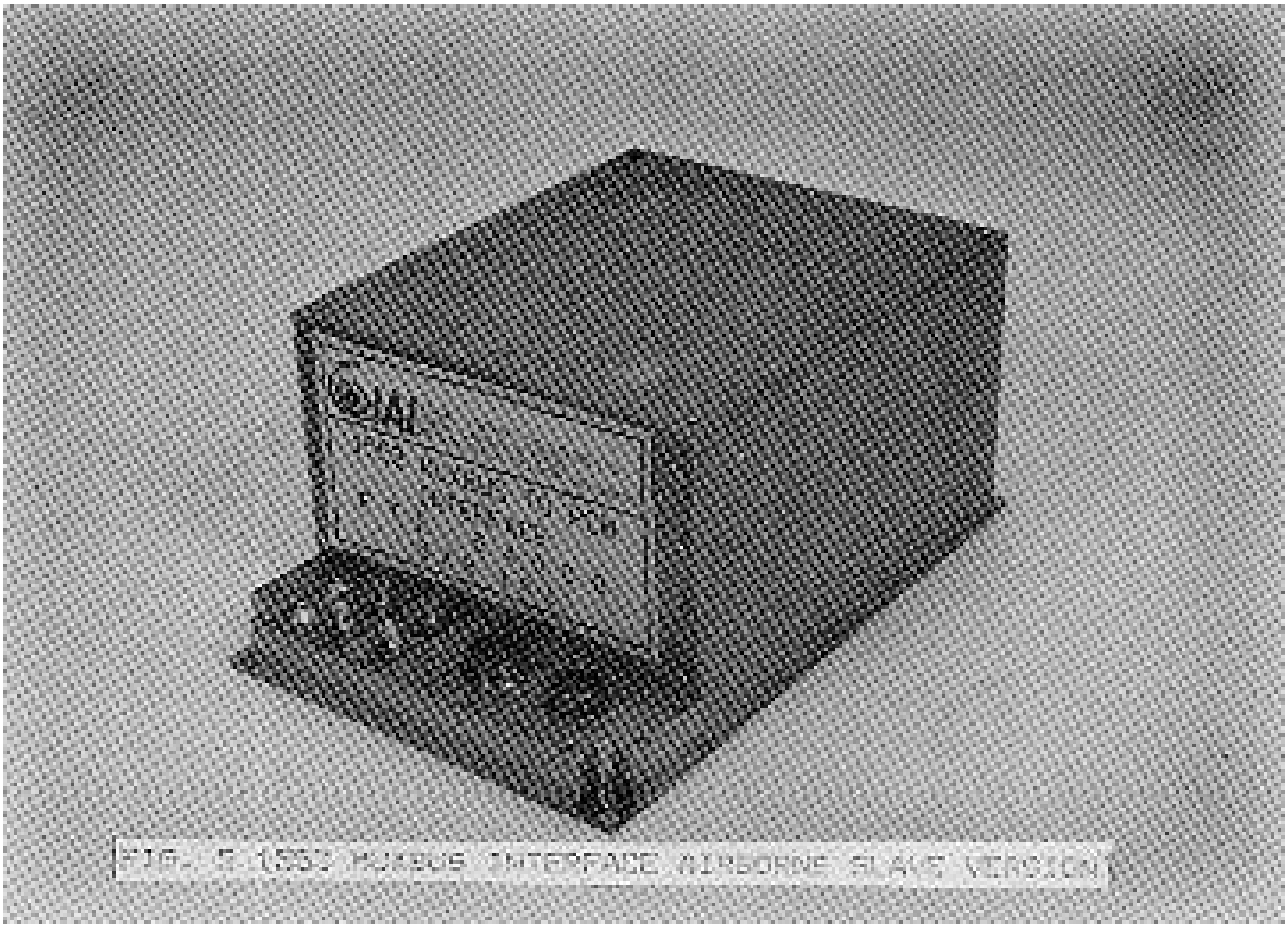


FIG. 5 (ESS) FUSEUS INTERFACE AIRBORNE SLAVE VERSION