SINGLE CHIP FIXED FREQUENCY BIT SYNCHRONIZER

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ABSTRACT

Over the past several years programmable logic devices have become a very attractive alternative to the application specific, Very Large Scale Integrated (VLSI) design approach. This trend is mainly due to the low cost and short design to production cycle time. This paper will describe a single chip, fixed frequency suboptimum bit synchronizer design which was implemented utilizing a programmable logic device. The bit synchronizer presented here is modeled after a Digital Transition Tracking Loop (DTTL) for symbol estimation, and employs a first-order Incremental Phase Modulator (IPM) for closed-loop symbol synchronization. Although the material presented below focuses on square wave subcarriers, with the appropriate modifications, this synchronizer will also process NRZ symbols. The Bit Error Rate (BER) and tracking performance is modeled and compared to optimum designs. The bit synchronizer presented here was developed for the Space Transportation System program under contract NAS5-27600 for meteorological data evaluation from the European Space Agency's (ESA) METEOSAT Spacecraft.

INTRODUCTION

Here we assume that our sampled subcarrier is composed of a sequence of independent and identically distributed random variables Y_1, Y_2,....., each containing a signal plus noise sample. We next define a random variable

$$X_i \quad \begin{matrix} 1 \text{ if } Y_i > j \\ -1 \text{ if } Y_i < j \end{matrix}$$

where j is chosen as the decision or transition region of the comparator, and the noise samples can be represented as white, band-limited, Gaussian random processes. The resultant sequence of X_i's will be used throughout this paper to control the addition or subtraction of our "one bit" accumulators. Thus, the accumulation process we refer to, in what follows, is no more than an up/down counter. The probabilities we compute are no more than the number of arrangements of X_i's times the associated probability which

results in a particular value of the counter given a prescribed initial condition over some interval;

e.g. P[S>0]= P[S=1] + P[S=2] +.....,+ P[S=m] .....,

Additionally, the phase relationship between the internally generated subcartier, which we will refer to as the reference subcarrier and the incoming modulated one, will be represented by 2N discrete states. Thus, the loop's current state k is contained in the closed interval [-N,N].

Updates to the Timing Generator causes the loop to transition to a new state, k, by an amount t/2N, where t=0,1,-1. The transitional behavior of this loop can be viewed as a Markov Chain, [1] and [2]. In the following paragraphs we will present the probability of a symbol error and the transition probabilities for this design.

SYNCHRONIZER OPERATION

The input to the bit synchronizer is a biphase modulated squarewave subcarrier. This input is conditioned by a low-pass filter of B Hz to prevent aliasing, then quantized to one bit by a comparator. Output samples from the comparator are then processed by the Data Transition Detector, the In-Phase Data Accumulator, and the Mid-Phase Tracking Accumulator.

The Data Transition Detector generates an output upon detecting the presence of a data transition from the incoming samples. The output from the Data Transition Detector is a three-state update vector which directs the Timing Generator to advance, retard, or maintain its current phase. The Mid-Phase Tracking Accumulator accumulates samples across the subcarriers mid-phase transitions to form an output like the Data Transition Detector. However, outputs from the Mid-Phase Tracking Accumulator are modulo two added with the current data symbol to correct the update direction. Both update vectors are accumulated over M bit periods to increase the sample signal-to-noise ratio before being presented to the Timing Generator. Additionally, increasing M, reduces the loops tracking bandwidth. The In-Phase Data Accumulator accumulates samples of the incoming subcarrier sequence modulo two added with the Timing Generator's subcarrier to generate NRZ symbols. Every 2N samples, this accumulator is sampled and then zeroed much like an "integrate and dump" circuit.

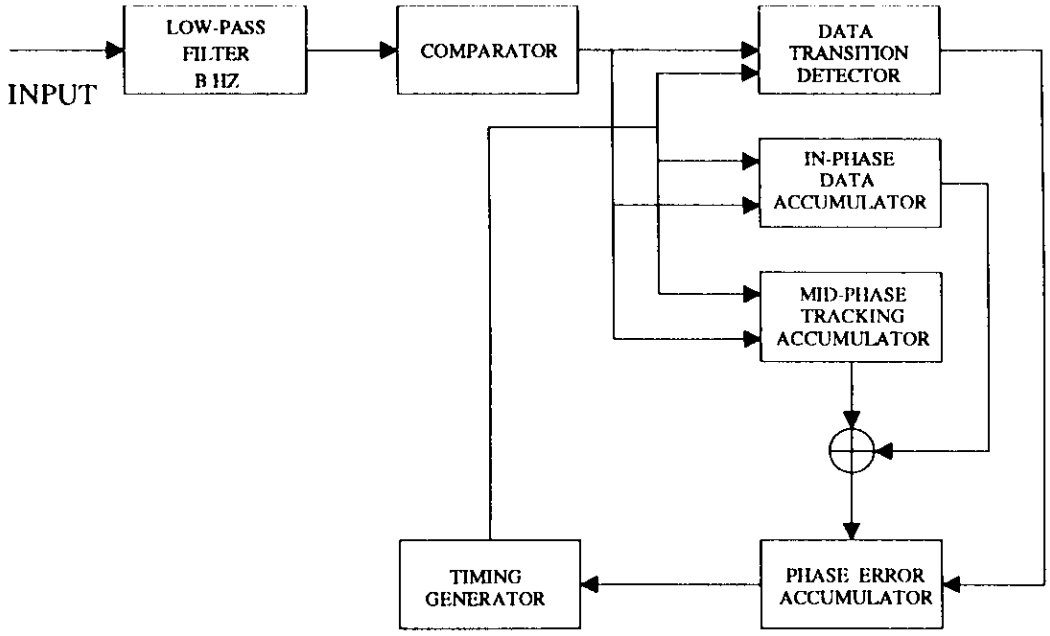

FIGURE 1 Simplified Bit Synchronizer Block Diagram.

SYNCHRONIZER ANALYSIS

The In-Phase Data Accumulator generates NRZ symbols from samples accumulated from the modulo two addition of the Timing Generator's reference subcarrier, and the incoming modulated subcarrier. When the loop is in state k=0, and given the In-Phase Accumulator accumulates 2N samples per subcarrier cycle, the magnitude of the value obtained at the end of the accumulation period is S(0)=2N - 1, where 1 is the number of error samples contained in the accumulation period. From Figure 2, we see that the maximum value obtainable by this accumulator is also reduced by the loop's state k. In fact, the magnitude of the value obtained by this accumulator is reduced by 2k with no data transition, and by k, with a data transition. Thus, the magnitude of the value obtained at the end of the accumulation period can be no greater than 2N-1-k with a transition, and 2N-1-2k with no transition. However, when the error samples are located within the phase error interval, the magnitude of the value obtained by the accumulator is actually increased. At the end of the accumulation period, the sign of the accumulator is used to determine the data value. Thus, the probability of error given the current loop state k, is computed by determining the number of arrangements of 1 error samples, plus the required k, accounting for a transition, times the associated sample probabilities, which changes the sign of the accumulator. Thus, the probability of a data error given the current loop state k, is

$$PE_k = P\sum_{l=\frac{2N-k}{2}+1}^{2N}\binom{2N}{l}p^l q^{2N-l} + Q\sum_{l=N-k+1}^{2N}\binom{2N}{l}p^l q^{2N-l} - P\sum_{l=\frac{2N-k}{2}+1}^{N+k}\sum_{i=1}^{k}\binom{2N-k}{l-i}\binom{k}{i}p^l q^{2N-l} - Q\sum_{l=N-k+1}^{N+2k}\sum_{i=1}^{2k}\binom{2N-2k}{l-i}\binom{2k}{i}p^l q^{2N-l}$$

where P is the probability of a data transition, Q=1-P is the probability of none, p is the probability of a sample error, and q=1-p.

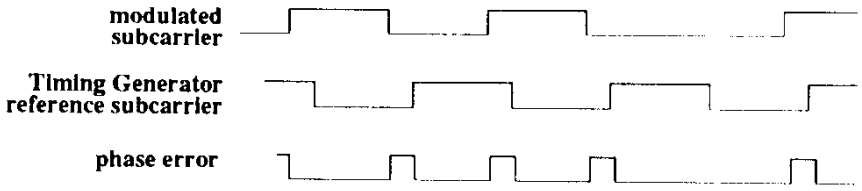

FIGURE 2 Phase Error Generated by Loop State k.

In this design, the Mid-Phase Accumulator is only allowed to accumulate samples across one subcarrier transition which the loop assumes is the mid-phase transition. The accumulation period starts at the Timing Generator's state -N/4 and ends at state N/4. The output from the accumulator is utilized to provide the Timing Generator's update when the loop's state k is between the range of -N/4, N/4. When the loop's state is outside this range, Timing Generator updates are provided by the Data Transition Detector. We now wish to obtain an expression for S(k) given k is within the above defined range. For k=0 this accumulator will contain an equal number of samples on either side of the subcarrier's mid-phase transition. Additionally, if the accumulator samples contain zero error samples, then its value will be zero at the end of the accumulation period. Now we will consider what happens to S(k) when k is non-zero. In this case, the accumulator will contain more samples from one side of the subcarrier's mid-phase transition than the other. Thus, the sign of the accumulator after the accumulation period modulo two added with the data value will indicate the loop's update direction, while an accumulator value of zero implies no phase error. However, in the presence of noise, the accumulator's value is modified by the presents of error samples. The probability that the update provided to the Phase Error Accumulator reduces the loop's phase error; i.e., the loop transitions to a new state k which decreases loop error, is computed by evaluating the number of arrangements of error samples on each side of the subcarrier mid-phase transition, given the current loop state k.

Let’s assume the Mid-Phase Tracking Accumulator accumulates across a negative-to-positive transition containing no noise samples. If the current loop state k is contained in the half open interval [-N/4,0], then the resultant accumulator sign will be positive and its magnitude is a function of the current state k; i.e., S(k)=k.

If we view the intervals on both sides of the mid-phase transition as disjointed, then an incorrect update will be generated if k+i< j where k is the loop’s current state, i represents the number of error samples in the first interval, and j represents the number of error samples in the second interval. Thus, the probability of generating the incorrect sign given the current loop state k, is

$$\sum_{i=0}^{N/4-k} \sum_{j=k+i+1}^{N/4+k} \binom{N/4-k}{i} \binom{N/4+k}{j} p^{i+j} q^{N-i-j}$$

where p is the probability of a sample error and q=1-p.

Since this loop requires a three-level update, we also need to inquire about the probability the loop will generate zero correction, given the current loop state k.

$$\sum_{j=k}^{N/4-k} \binom{N/4-k}{j-k} \binom{N/4+k}{j} p^{2j-k} q^{N-2j+k}$$

where p and q are defined as above.

The Data Transition Detector is composed of a one bit wide finite impulse response filter (FIR), a threshold accumulator, and a subcarrier phase counter. The FIR has N taps, with the output samples form by the modulo two addition of taps zero and N. Since the modulated subcarrier has a period of 2N samples, the FIR output samples will contain the same sign in the absence of noise and modulation. Output samples from the FIR are processed by the threshold accumulator which generates an output pulse who’s width is a function of the accumulator’s value. The subcarrier phase counter uses the generated output pulse as an enable, which allows the counter to count up during one phase of the reference subcarrier, and down during the other. The value of this counter is sampled at the end of this operation to generate the loop’s update vector. Analysis of the threshold accumulator will allow us to compute the probability the Data Transition Detector generates the incorrect sign given the current loop state k.

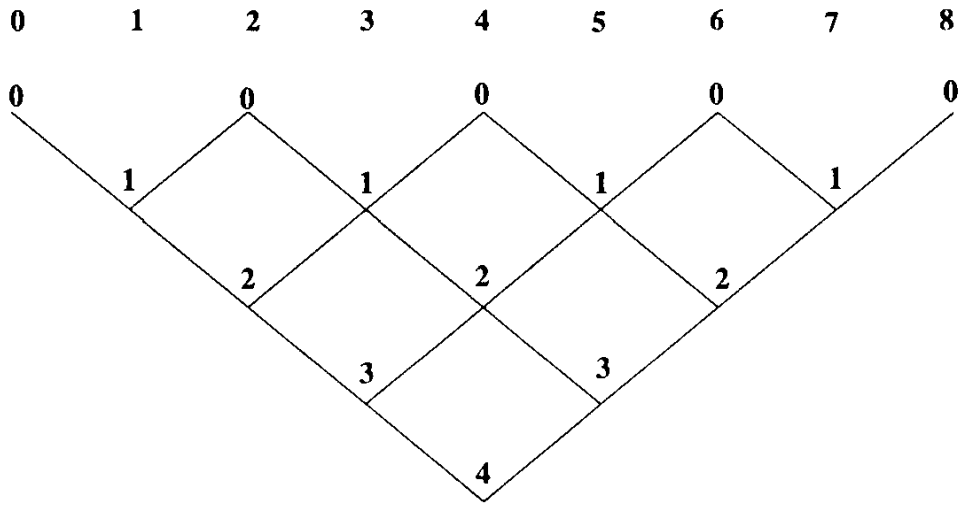

FIGURE 3 An Example of The Threshold Accumulator States.

The threshold accumulator used in this synchronizer design, is not permitted to obtain a negative value; i.e. if the current value of the accumulator is zero and we add a -1, the resultant accumulator value will be zero. If we elect to set the threshold value at j, then an output will be generated once the accumulator has obtained a value of j + 1 and will terminate when it reaches a value of j. To determine the number of arrangements of "1", "-1" which generate a given pulse width 2t, we note this requires 2t sample with "t" ones, and "t" minus ones. Additionally, the pulse start requires the first sample to be a plus one while the pulse ending requires a minus one sample. Thus, the minimum pulse width requires two samples. In order to generate pulse widths greater than two samples in length, we find the pulse start requires a minimum of two consecutive plus one's, and the pulse ending requires two consecutive minus one's. Because of the preceding requirement, we only need to compute the number of arrangements of the remaining 2t-4 elements. We are now able to compute the probability of a pulse width of 2t samples given the threshold accumulator equals j. In the absence of noise, given the current loop state is k=0, the threshold accumulator generates an output j samples before the mid-phase transition of the reference subcarrier, and terminates j samples afterwards. Thus, the subcarrier phase counter's finial value is zero since the counter increments or decrements depending on the subcarrier's phase. For non-zero k, the sign of this counter will determine the update direction. However, in the presence of noise, error samples will affect the pulse start time and duration. Given the current loop state is k, we only need to determine what pulse start time and duration will generate the incorrect sign from the subcarrier phase counter, thus increasing loop phase error. If we separate the threshold pulse into two intervals, (I_1,I_2) about the mid-phase reference subcarrier transition, then the size of each interval is the number samples contained in each one, and I_1,I_2 equal the pulse duration expressed in samples. Choose a loop state $k=k_1$ such that $I_2>I_1$ in the absence of noise, thus in the presence of noise, an incorrect update sign will be generated if $I_1>I_2$. The probability the

Data Transition Detector generates the incorrect sign given the current loop state is k, is defined as

$P[\ S(0)=j-m\ ]\ P[\ S(m)=j\ ](P[\ I_1>I_2\ |\ k\ ]+P[\ I_1=I_2|\ k\ ])$

where

$$P[S(m)=l] = \sum_{i=0}^{m-l} \binom{l+i}{i} p^{l+i} q^{m-l-i}$$

$$P[I_1>I_2|k] = \sum_{m=0}^{N-k-2} \sum_{i=0}^{N-m-k-3} \binom{2i}{i} p^{i+2} q^{i+2} + pq$$

$$P[I_1=I_2|k] = \sum_{i=0}^{N-k-m-2} \binom{2i}{i} p^{i+2} q^{i+2} + pq$$

and $P[\ S(0)=j-m\ ]$ is defined as the probability the threshold accumulator initial value is j-m, $P[\ S(m)=j\ ]$ is the probability the threshold accumulator value is equal to j after m samples, and

$P[\ I_1>I_2|\ k\ ]$ is defined as the probability the number of samples contained in interval I_1 are greater than I_2, given k. Similarlly, $P[\ I_1=I_2\ |\ k\ ]$ is interpeted as the probability of generating zero given the current loop state k.

The Phase Error Accumulator accumulates loop updates from both the Data Transition Detector and the Mid-Phase Tracking Accumulator to form an average update sign. The probability the resulting update reduces loop phase error is computed by determining the number of arrangements of M update “1”,“-1”, and “0”, times the associated probabilities which results in a reduction of loop phase error. Thus, the probability of generating the incorrect update given the loop’s current state is k, is

$$\sum_{j=1}^{M} \sum_{i=j}^{M} \binom{M}{i} \binom{M-i}{i-j} p_k^i q_k^{i-j} r_k^{m+j-2i}$$

where M is the number of update samples accumulated per update.

P_k - probability of generating the incorrect update given k.

q_k - equals $1-p_k-r_k$ where r_k is the probability of generating zero loop correction.

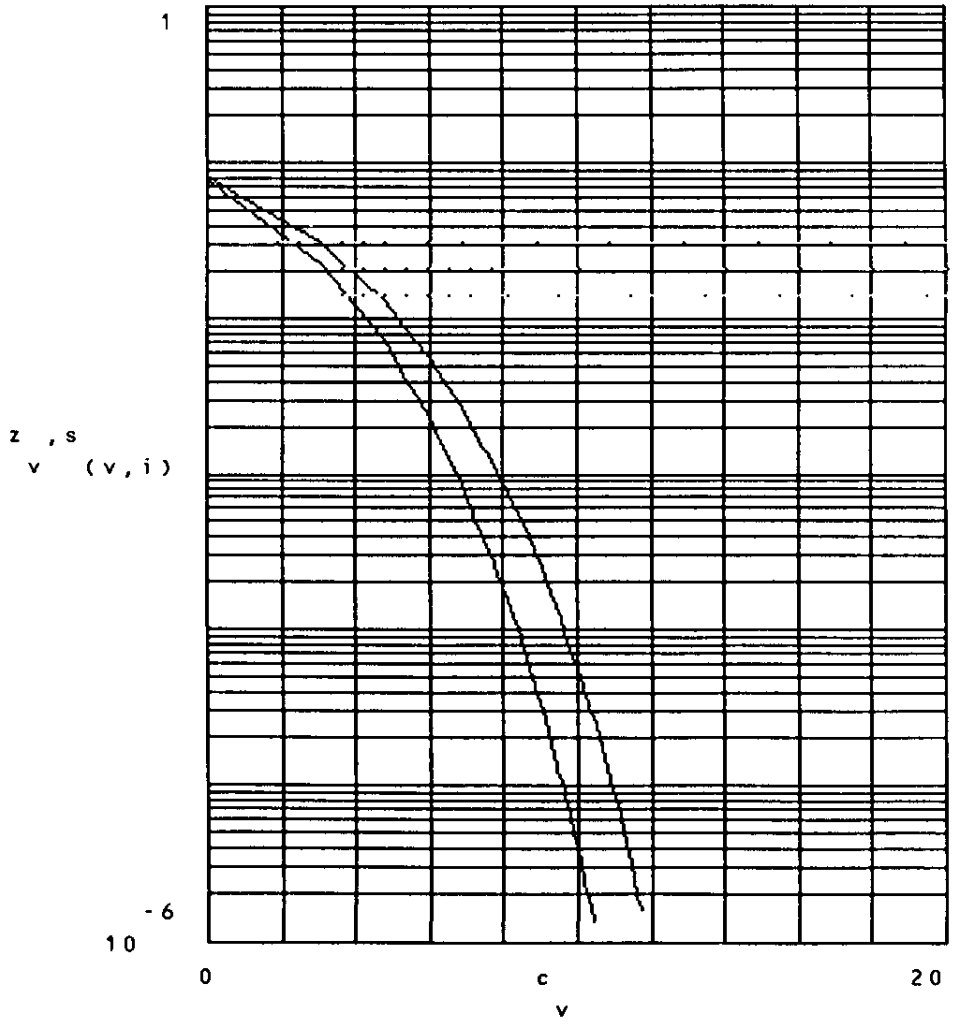

FIGURE 4 PE vs SNR (db) for Optimum and Suboptimum

CONCLUSION

The bit synchronizer modeled above was actually implemented in a programmable logic cell array made by Xilinx. In this design we chose a sample rate of 16 times our modulated subcarrier rate of 166.666 KHz. Thus, the sample period 2N, equals 16. As we mentioned earlier, the tracking bandwidth is a function of the number of bit periods M, over which the update vector is averaged. In this design, we chose M to be 4, thus permitting a tracking bandwidth on the order of 0.7 percent. The transition threshold j was selected to be 4 samples, generating a nominal 8 sample, 2j wide transition pulse. A single pole low pass filter was used in this design, with a cut-off frequency set at 6 times the data rate which minimizes signal distortion in the pass band and provide an anti-aliasing feature.

Additionally, a crystal oscillator was used to generate the 16 times sample rate. This approach reduced the phase noise during non-update periods as compared to standard frequency synthesis. The bit error rate performance was measured in a laboratory environment, and was found to be in agreement the theoretical predictions, when $E_b > N_o$. When $E_b < N_o$, the performance of this synchronizer does deviate from the theoretical BER curve provided in this paper. However, we believe this discrepancy is due to the signal shape near the transition points, [1] and [2], and the assumptions used to formulate the sampled signal-to-noise probability.

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