PROGRAMMING CODE-MODULATOR AND DEMODULATION-DECODER SUITED TO PCM SYSTEMS

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ABSTRACT

In order to suit the development of computer telemetry systems, we have developed the intelligent code-modulator and demodulation-decoder. In hardware, they consist of a monolithic processor and some high-integrated devices. Different code or decode ways and several subcarrier modulation or demodulation systems can be varied by carrying out corresponding software programs. In this paper, the equipments' hardware constructions and software cnarts and their main principles are presented.

KEY WORDS: code, modulation, monolithic processor

INTRODUCTION

In order to suit the development of computer telemetry systems, which have modularized structure and buses organization, we have developed the intelligent code-modulator and demodulation-decoder.

In hardware, they consist of a monolithic processor and some high-integrated devices, therefore their volume and weight are smaller (lighter) than others, so that it is better to use them in airborne equipments. Different code or decode ways (corresponding to different frame and subframe structure), several subcarrier modulation or demodulation systems (DPSK, FSK, ASK, etc), the code rate and the subcarrier frequency are varied by carrying out corresponding software programs memorized in EPROM in the monolithic processor, so that they have better antijamming properties.

CODE-MODULATOR

The main principles:

The code is accomplished by a monolithic processor, whose input signals are telemetry data, decode answerbacks, actuality answerbacks, etc. and whose outputs are frame structure singnals. The sampling points of sinusoidal waves are memorized in EPROM, whose address bus are linked to data output interface of a double CTC. The monolitic processor controls the double CTC to read out the corresponding sampling values which take shape the corresponding subcarrier modulation signals (sinusoide waves) in output interface of EPROM (data bus). The principles are shown in figure 1.

The hardware construction & software chart:

The hardware construction is shown in figure 2.
The software chart is shown in figure 3.

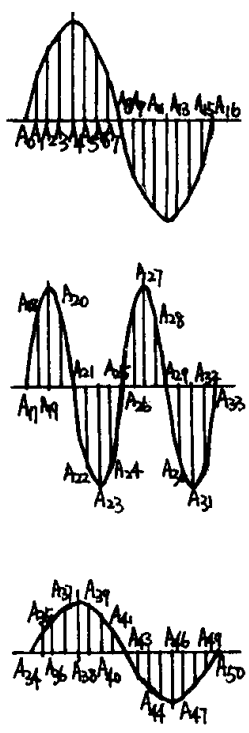
The analog switch and the A/D converter act as telemetry exchanger. 8/1 analog switch forms subframe, 32/1 analog switch and 8 bit A/D form frame. In order to keep coder rate, the monolithic processor must periodically output frame construction signals, thus open-interrupts have to be arranged between intervals of two bits signals. D/A converter converts sinusoide sampling digital values into analog signlas. The low-pass filter is a smoothing circuit.

DEMODULATION-DECODER

The main principles:

The overzero detector converts subcarrier signals into square waves to input them to the monolithic processor. The DPLL takes out bit-synchronization signals to send them to the interrupt-end of monolithic processor as interrupt-sampling signals. Each square wave is divide-equally sampled four time. (Each synchronization signal is sampling starting-point.) The four sampling values are compared and judged to demodulate “0" and “1”. By software controlling, the monolithic processor takes out frame synchronization signals from demodulated binary signals and takes frame synchronization protection, i.e. three-state protection, whose principle software chart is shown in figure 4.

The hardware construction is shown in figure 5.
The interrupt software chart is shown in figure 6.



ADDRESS	VALUES
0 0 0 0 0 0	A_0
0 0 0 0 0 1	A_1
0 0 0 0 1 0	A_2
0 0 0 0 1 1	A_3
1 0 1 1 1 1	A_{47}
1 1 0 0 0 0	A_{48}
1 1 0 0 0 1	A_{49}
1 1 0 0 1 0	A_{50}

EPROM

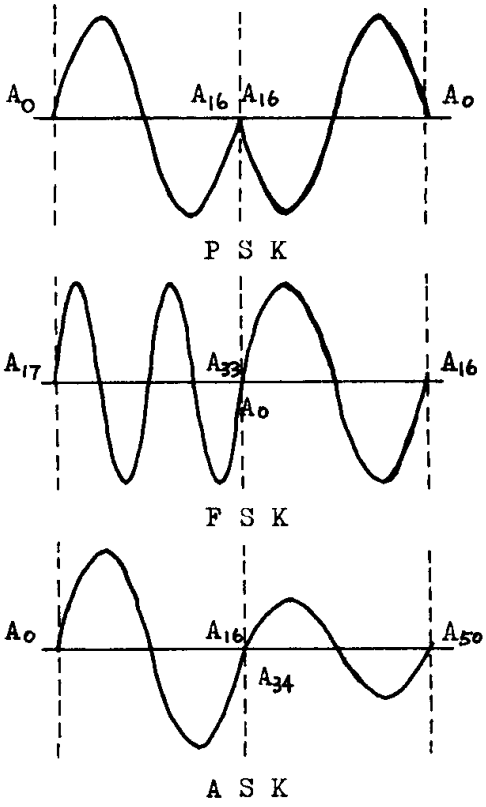


Figure 1

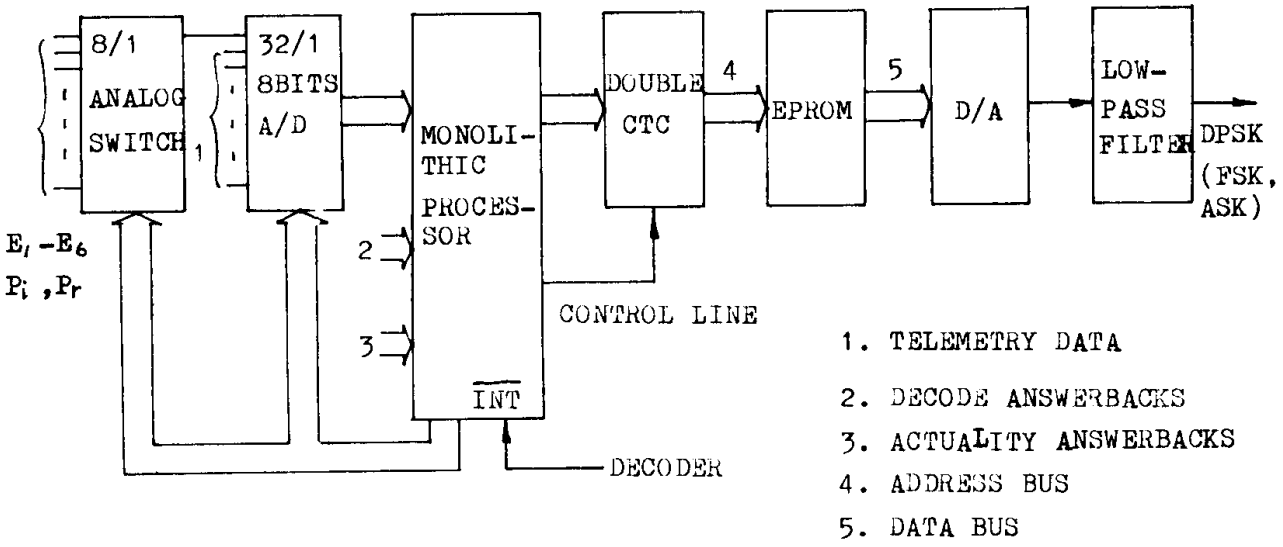


Figure 2

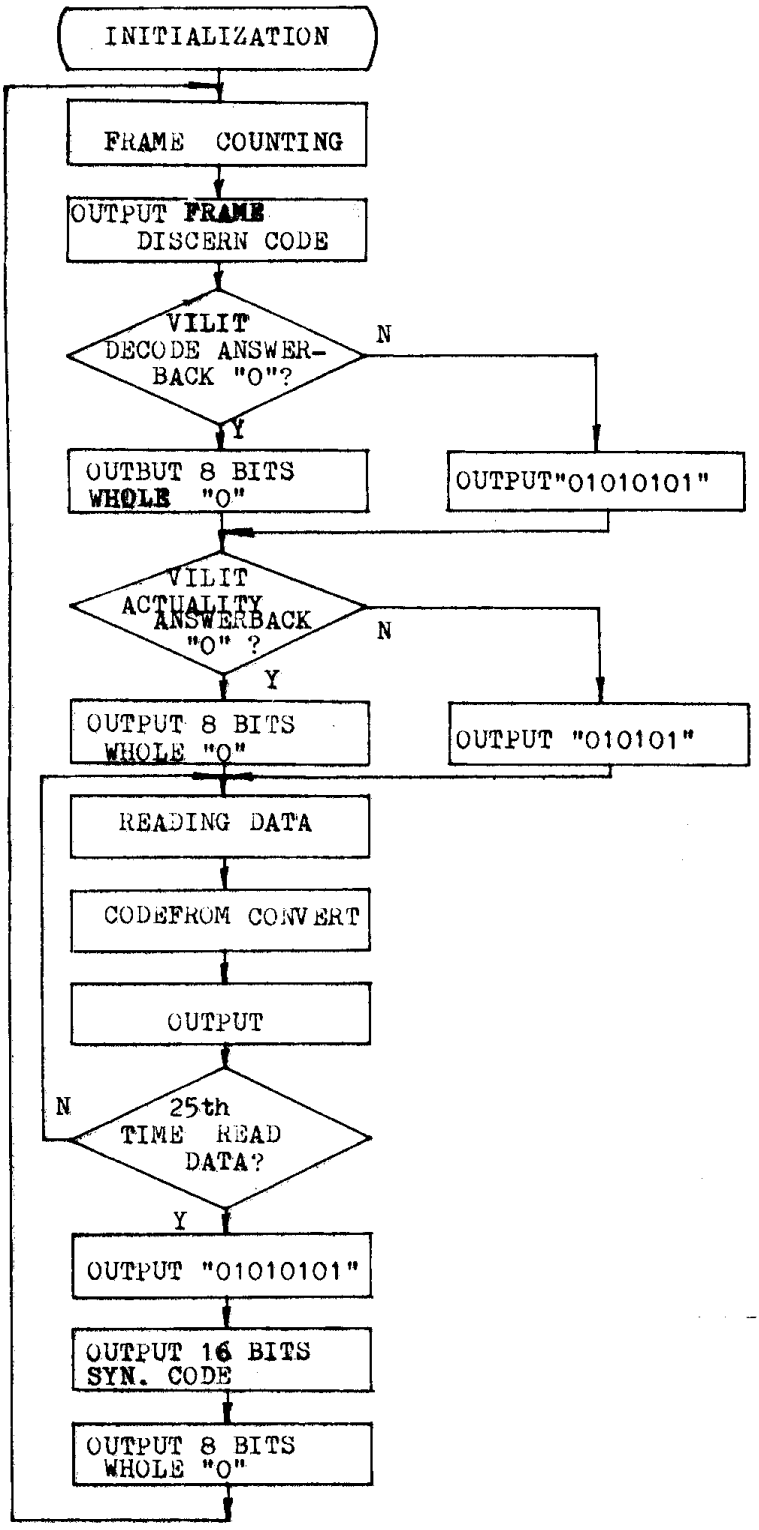

INITIALIZATION
FRAME COUNTING
OUTPUT FRAME DISCERN CODE
VILIT DECODE ANSWER-BACK "O"?
N
Y
OUTBUT 8 BITS WHOLE "O"
OUTPUT"01010101"
VILIT ACTUALITY ANSWERBACK "O" ?
N
Y
OUTPUT 8 BITS WHOLE "O"
OUTPUT "010101"
READING DATA
CODEFROM CONVERT
OUTPUT
N
25th TIME READ DATA?
Y
OUTPUT "01010101"
OUTPUT 16 BITS SYN. CODE
OUTPUT 8 BITS WHOLE "O"

Figure 3

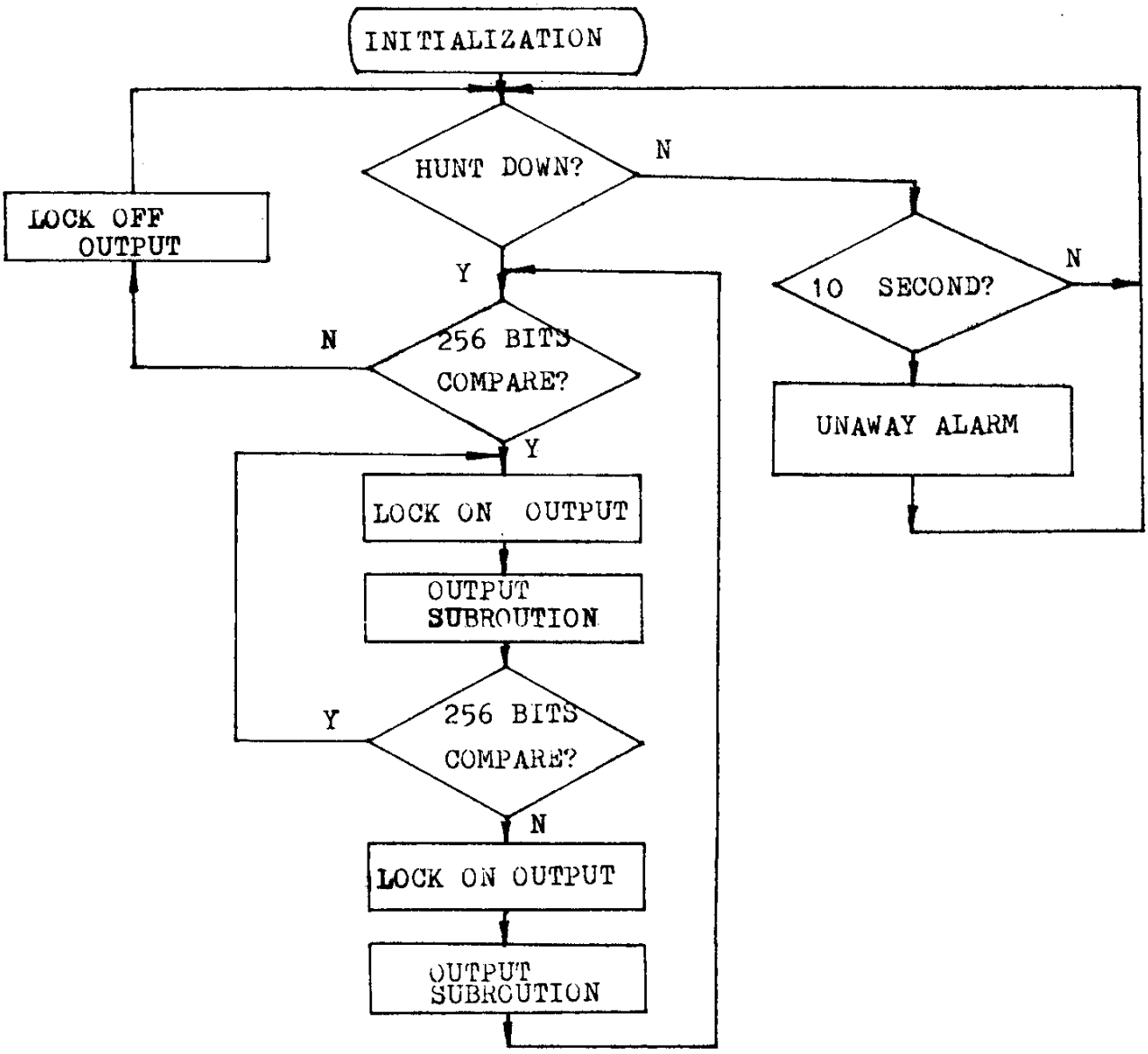

INITIALIZATION
HUNT DOWN?
N
LOCK OFF OUTPUT
Y
10 SECOND?
N
N
256 BITS COMPARE?
UNAWAY ALARM
Y
LOCK ON OUTPUT
OUTPUT SUBROUTION
Y
256 BITS COMPARE?
N
LOCK ON OUTPUT
OUTPUT SUBROUTION

Figure 4

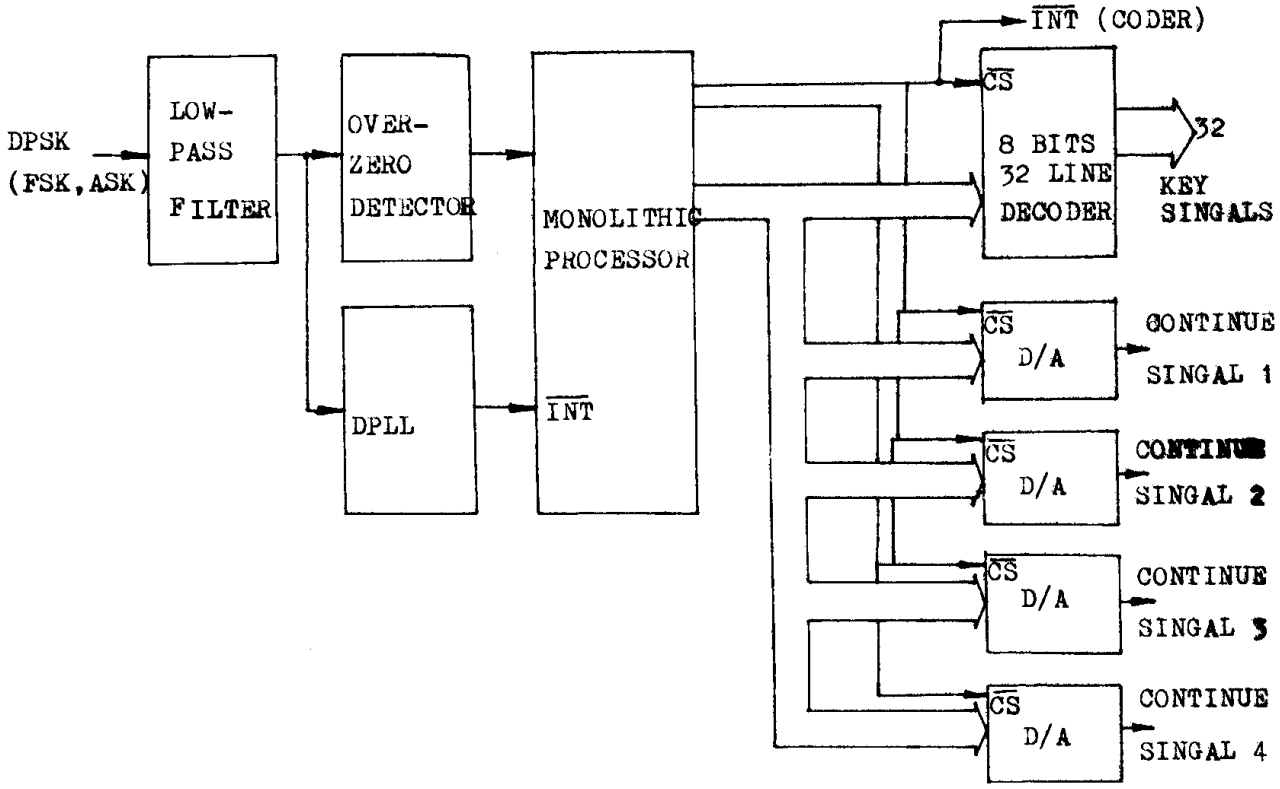


Figure 5

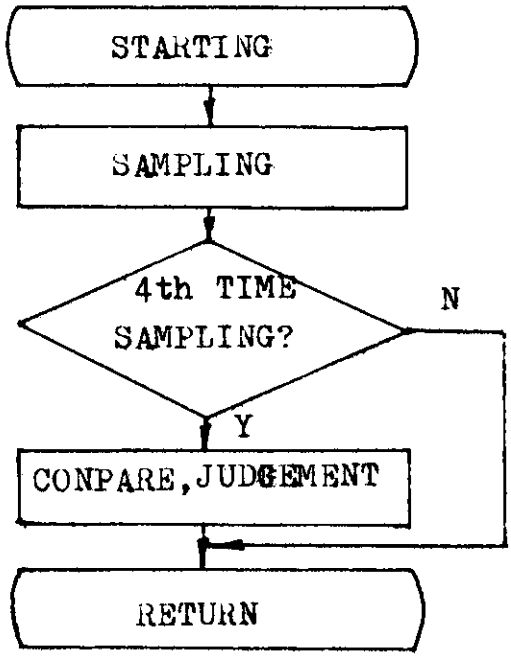


Figure 6