HIGH SPEED VLSI SYSTEMS FOR NASA S TELEMETRY RETURN LINK PROCESSOR

Sarah L. Hand, Luis G. Salichs
Data Systems Technology Division
Code 520

John K. Steedman
NASA Communications Division
Code 540

Mission Operations and Data Systems Directorate
NASA, Goddard Space Flight Center
Greenbelt, Maryland 20771

ABSTRACT

In the upcoming Space Station Freedom (SSF) era, NASA will require many new data systems capable of performing basic data handling functions such as Frame Synchronization, Frame Error Detection & Correction, and Multiplexing/Demultiplexing at rates in the hundreds of Megabits per second (Mbps) range. The Data Interface Facility (DIF) is a key element in NASA's advanced communications systems. The DIF will support communications between the space elements and multiple ground facilities.

This paper will describe the architecture of the DIF and its core element, the Return Link Processor (RLP). Current activities to prototype some of the primary functions of the RLP will be presented. Finally, the paper will show how the prototype elements could be integrated into a full performance DIF RLP.

1. INTRODUCTION

The Goddard Space Flight Center's Mission Operations and Data Systems Directorate is applying advanced technologies such as Very Large Scale Integration (VLSI) to the development of components and systems to meet NASA's data handling needs well into the future. These systems will be needed to support space elements communicating through the Tracking and Data Relay Satellite System (TDRSS) such as the Space Station Freedom (SSF), the Polar Orbiting Platform (POP), and the Co-orbiting Platform (COP).

Current efforts include the development of high speed VLSI systems for the core of the DIF, the Return Link Processor (RLP). The DIF RLP must perform the functions of Frame Synchronization, Reed-Solomon Decoding, Virtual Channel Sorting, and Frame

Multiplexing at rates up to 150Mbps. Two high speed systems, the Virtual Channel Sorting System (VCSS), and the Virtual Channel Multiplexing System (VCMS), comprise the full performance DIF RLP. This paper describes the architecture and components that have been prototyped for these systems and how they will meet the requirements of the DIF RLP.

2. DIF OVERVIEW

Return Link data generated by a low-earth orbiting spacecraft will be sent through a Tracking and Data Relay Satellite (TDRS) to one of the two geographically diverse ground terminals at the White Sands Complex (WSC) in White Sands, New Mexico (figure 1). The WSC will be made up of the White Sands Ground Terminal (WSGT), the Second TDRS Ground Terminal (STGT), and the Data Interface Facility (DIF). The DIF will serve as a gateway between the space network and the ground distribution network. The ground terminals will have multiple interfaces to the DIF. The rate of these interfaces will depend on the type of service the spacecraft is using.

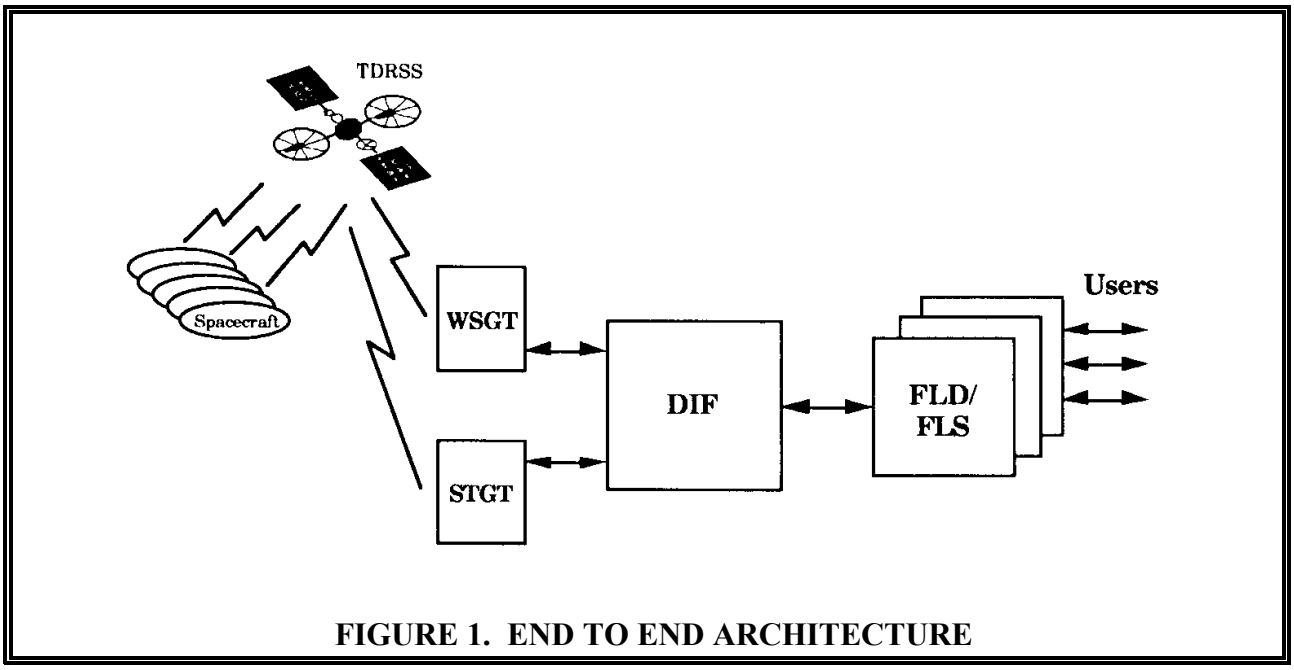

FIGURE 1. END TO END ARCHITECTURE

On the return link, the DIF will support twelve K-band single access (KSA) channels at 150Mbps and twelve S-band single access (SSA) channels at 3Mbps. The DIF will accept streams of data from the ground terminals that comply with the framing format recommended by the Consultative Committee for Space Data Systems (CCSDS). This format is referred to as the Virtual Channel Data Unit (VCDU) (figure 2) and will be the unit of data on which the DIF will operate. The DIF will route VCDU's to First Level Destinations (FLD). The FLD provides some data processing functions and serves as an interface to the user.

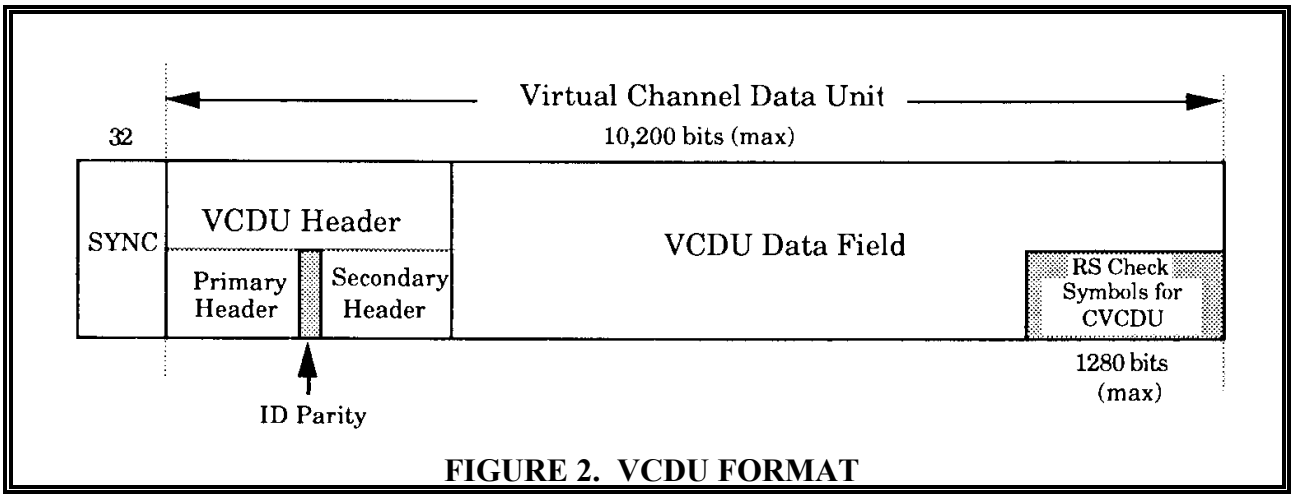

FIGURE 2. VCDU FORMAT

Similarly, on the forward-link, data generated by a First Level Source (FLS) will also comply with the VCDU format. Forward link VCDU's will be routed to ground terminal interfaces, each of which represents a spacecraft. On the forward link, the DIF will support twelve KSA channels at 25Mbps each and twelve SSA channels at 300kbps each.

VCDU's are of two types: those protected by a Reed-Solomon (RS) code called Coded Virtual Channel Data Units (CVCDU) and those that are not protected called VCDU's. This paper will use the term VCDU to generically refer to both types. Within the Primary Header of the VCDU are Spacecraft and Virtual Channel Identifier fields (SC/VCID). The SCID uniquely specifies a source of return link data or a destination for forward link data. The VCID allows for up to 64 virtual channels to be active for each assigned SCID. The DIF will base its routing on these fields. At the end of a CVCDU is a space for the parity checks of a RS forward error correcting code. It will be the responsibility of the DIF to correct the correctable errors within CVCDU's and detect those that are uncorrectable. The SC/VCID fields are covered by a shorter RS code to ensure that the routing information is correct when VCDU's are used. However, the RS code that covers the whole data unit is more powerful than the one that covers the header. Finally, a 32 bit synchronization field is added to the VCDU to form the data unit that is sent over the physical channel.

2.1 DEF FUNCTIONAL ARCHITECTURE

The DIF will be composed of several functional elements (figure 3). The DIF contains circuit switches on both the side that interfaces to the WSGT/STGT and the side that interfaces to the ground communications system. The switch on the WSGT/STGT side serves two functions. On the return link it selects the element of the Return Link Processor to be used for a particular spacecraft. If one of the elements of the RLP were to fail, this switch could select an alternate. On the forward link, this switch selects the forward link interface to the WSGT/STGT. The switch on the ground communications

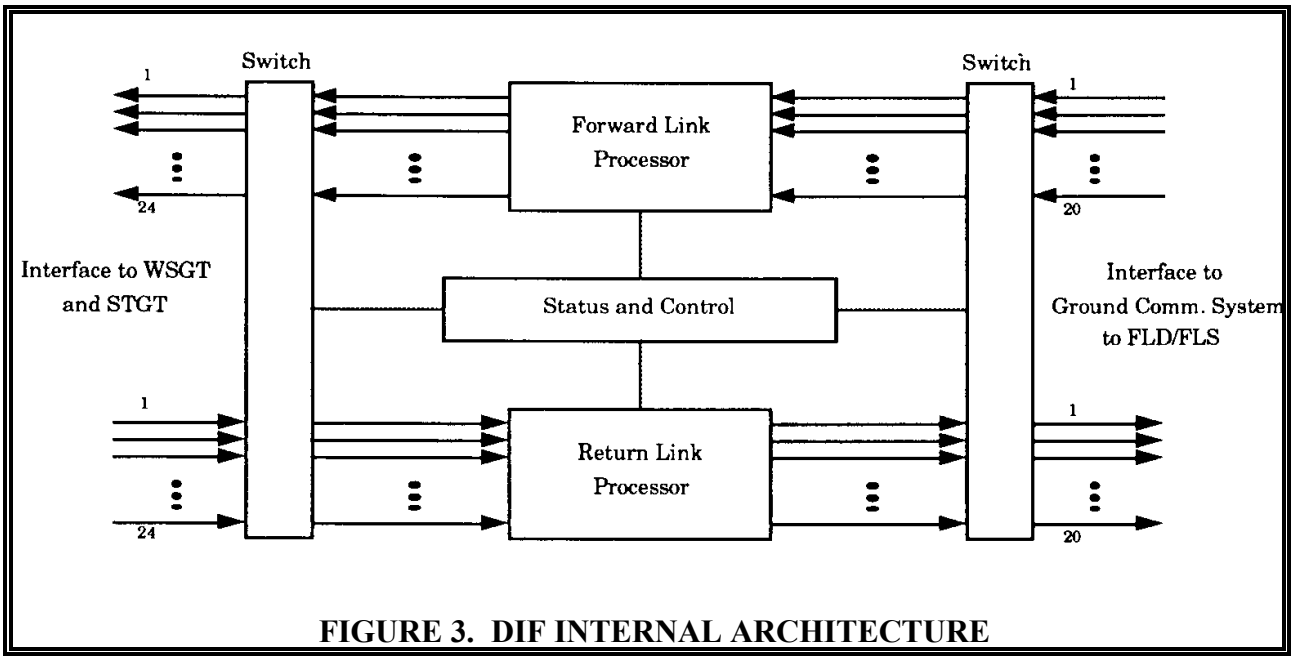

FIGURE 3. DIF INTERNAL ARCHITECTURE

system side also performs two functions. On the return link, it selects the ground communication interface to the FLD and can select another in the case of a failure. On the forward link, the switch selects the element of the Forward Link Processor (FLP) that will serve a particular First Level Source (FLS).

Both the RLP and the FLP operate on VCDU's. This paper primarily discusses the functions of the RLP. The RLP accepts a stream composed of VCDU's from the ground terminal interface. The RLP synchronizes on the data stream, corrects errors in CVCDU's that may have been incurred on the space-ground link, and routes VCDU's based on the SCNCID field. The RLP removes fill frames inserted by the spacecraft which are identified by the all ones VCID. The RLP also inserts fill frames at the output to maintain a continuous stream to the FLD. The FLP performs similar functions on the forward link.

The DIF will also maintain a Status and Control System to allow the DIF to change configurations and recover from failures in an automated fashion. Finally, the DIF may also provide storage for line-outage protection or rate-buffering.

3. RLP FUNCTIONAL ARCHITECTURE

A model for the Return Link Processor (RLP) is shown in figure 4. The RLP must accept 24 input data streams consisting of VCDU's from the ground terminal interface and route the VCDU's to as many as 20 First Level Destinations. The input streams are processed by the 24 independent input channels of the RLP each consisting of the following elements:

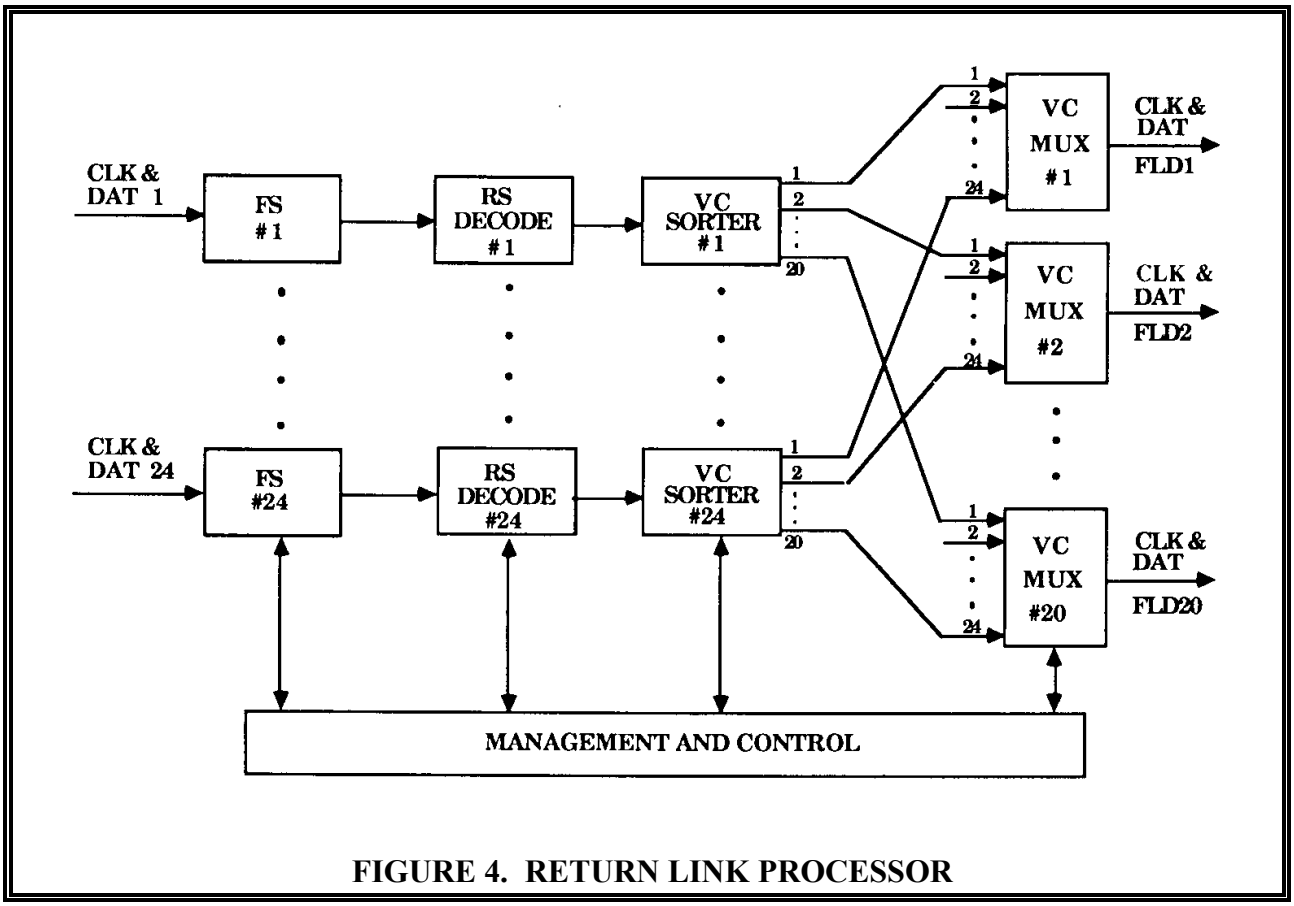

FIGURE 4. RETURN LINK PROCESSOR

- Frame Synchronizer (FS)
- Reed-Solomon Decoder (RS DECODE)
- Virtual Channel Sorter WC SORTER)

All VCDU's destined for the same FLD would then be multiplexed together by a Virtual Channel Multiplexer (VC MUX). By using 20 VC MUX's, the RLP could support 20 FLD's.

The above functions are currently being prototyped by the Mission Operations and Data Systems Directorate at the NASA/Goddard Space Flight Center. Four cards are currently under development: the Frame Synchronizer Card (FS Card), the Reed Solomon Card (RS Card), the Virtual Channel Sorter Card (VC Sorter Card), and the Virtual Channel Multiplexer Card (VC Mux Card). Each of these cards represents a generic stand-alone function that takes advantage of previous design activities and could also be used in other data processing systems.

Each card is physically a 9U VME printed circuit board. One third of the card is a commercially available single board computer with 512kbytes of RAM, VME bus

arbitration logic, and interrupt capability. This CPU board acts as the Card Controller (CC) on which all operational programs are run. Through a side connector the custom logic card is attached which provides the special purpose hardware needed to perform the card specific functions. Each custom card utilizes semi-custom VLSI gate arrays designed in the Microelectronics Systems Branch, Code 521.

Using these cards, a 2-input, 2-output prototype of the RLP is being developed as a proof-of-concept. Early testing indicates that this system will operate at 20Mbps. The full-performance DIF RLP described in this paper is based on this prototype and is expected to operate at 150Mbps.

3.1 FRAME SYNCHRONIZER CARD

The Frame Synchronizer Card (FS Card, figure 5) utilizes Emitter Coupled Logic (ECL) for performing the frame synchronization function on a single data channel. This design is modeled after the existing low rate CMOS FS Card currently used in other data handling systems. To provide a low cost, compact and standard implementation of this function, this design incorporates semi-custom ECL VLSI gate arrays, taking advantage of the high switching rates and high density characteristics of current ECL gate array technology.

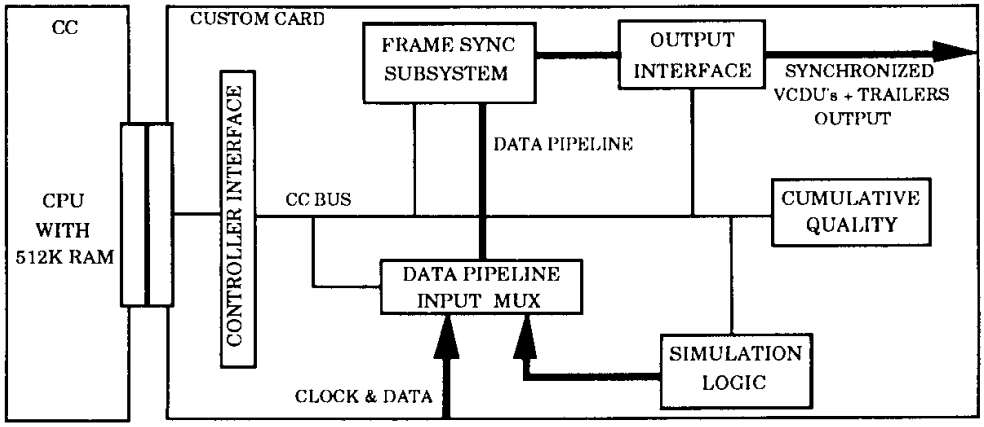

FIGURE 5. FS CARD BLOCK DIAGRAM

The Frame Synchronizer Card receives VCDU's formatted according to the CCSDS data format. The FS card provides a programmable synchronization strategy in which it searches for the Sync Mark (32 bits max), locks to it and then continues looking for the Sync Mark in subsequent VCDU's at the expected position. This card provides quality information on the data received, VCDU buffering, quality trailer generation and self test capability.

The Frame Synchronizer design is divided into six subsystems: Data Pipeline Input Mux, Frame Sync, Output Interface, Cumulative Quality, Simulation Logic, and Controller Interface.

3.1.1 DATA FLOW

The CC transfers setup data through the Controller Interface to every subsystem on the card. This setup data includes the synchronization pattern (up to 32 bits), the VCDU length, and a specific synchronization strategy to insure proper buffering of telemetry VCDU's. The Data Pipeline Input Mux allows the FS card to receive data from different external sources or from the on-board Simulation Logic for self test purposes.

After finding the frame synchronization pattern, the Frame Sync subsystem begins the implementation of a search, check, and lock strategy to insure correct buffering of VCDU's. The Frame Sync subsystem can be programmed to accept either Forward True (FT), Forward Inverted (FI), Reverse True (RT), or Reverse Inverted (RI) data. It provides for data buffering of up to 4K bytes and for automatic VCDU transfer through a parallel Output Interface. A status word is generated for each VCDU processed which indicates if there was a sync error, CRC error or slip error and the mode of the Frame Sync subsystem (search, check, lock, flywheel). It also indicates if the data stream is in RT, RI, FT, or FI format. The status word is used by the Cumulative Quality subsystem to provide the CC with the status of the Frame Synchronizer card for each VCDU processed.

3.2 REED-SOLOMON CARD

The CCSDS has recommended the use of the Reed-Solomon forward error correcting code on the space-to-ground link. The RS code was selected because of its ability to correct the multiple burst errors that may occur in space links. Specifically, they have recommended a (N=255,K=223) symbol code where the symbol size is eight, N represents the code word length (data+parity), and K is the length of the data space. The length of the parity field is 32 symbols which is capable of correcting 16 symbols in error. This particular code can correct one maximum burst length of 121 bits per code word. The rate of the code is 0.875.

The CCSDS has also recommended an interleaving method to be used over the CVCDU. As mentioned before, the space-to-ground link is susceptible to burst errors. An interleaver rearranges the order of a block of data in a deterministic fashion prior to transmission. At the receiving end, the decoder must deinterleave the data before it can be decoded. This has the effect of distributing the errors more uniformly at the decoder.

3.2.1 DATA FLOW

The primary functions of the RS Card are to correct errors within CVCDU's and within the header of all VCDU's (figure 6). The RS Card accepts frames through a parallel interface from the FS Card and outputs through a parallel interface to the VC Sorter Card. There is no hardware currently available to perform the header decoding so this version of the card will only use the RS header check bits to determine if errors have occurred. The RS Card deinterleaves those CVCDU's that are more than one RS codeword in length, corrects the CVCDU's codeword by codeword, interleaves the corrected codewords back into a CVCDU, and then re-encodes the CVCDU. The chip-set that does the RS decoding over the CVCDU provides a byte of status for each codeword to indicate if it was correct, correctable, or uncorrectable. Taken together with the results of the parity check on the header, the RS Card determines whether a frame is routable or not. An alternate path is provided through the card to recover VCDU's if the RS decoding status and header parity check indicates that a VCDU with a good header has been received.

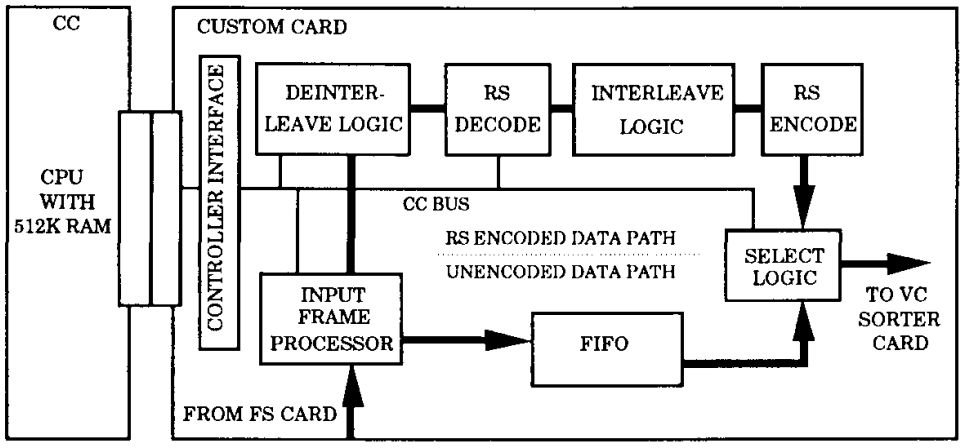

FIGURE 6. RS CARD BLOCK DIAGRAM

3.3 VIRTUAL CHANNEL SORTER CARD

The Virtual Channel Sorter Card (VC Sorter Card) accepts routable VCDU's through a parallel interface from the RS Card. Based on information in the VCDU header and a programmable look-up table, each data unit is routed to one or more of eight output ports. Fill VCDU's are filtered (i.e. not routed).

3.3.1 DATA FLOW

A block diagram of the VC Sorter Card is shown in figure 7. The Decode and Control Subsystem provides the interface to the CC and allows for the memory mapping of all of the other logic subsystems. The incoming parallel data is automatically buffered by the Input Control Subsystem which maintains a triple buffering cycle. This allows the CC to read the SC/VCID field in the header of each VCDIJ. Based on this information and a programmable look-up table, the operational program writes a byte of data to the Virtual Channel ID (VID) latch in the Status/Control Subsystem. The VID latch controls hardware in the Output Subsystem which allows the VCDIJ to be routed to the appropriate output ports (from zero to eight). The Cumulative Quality Subsystem automatically maintains various card statistics. The Data Simulation Subsystem provides for complete self-testing of all card functions.

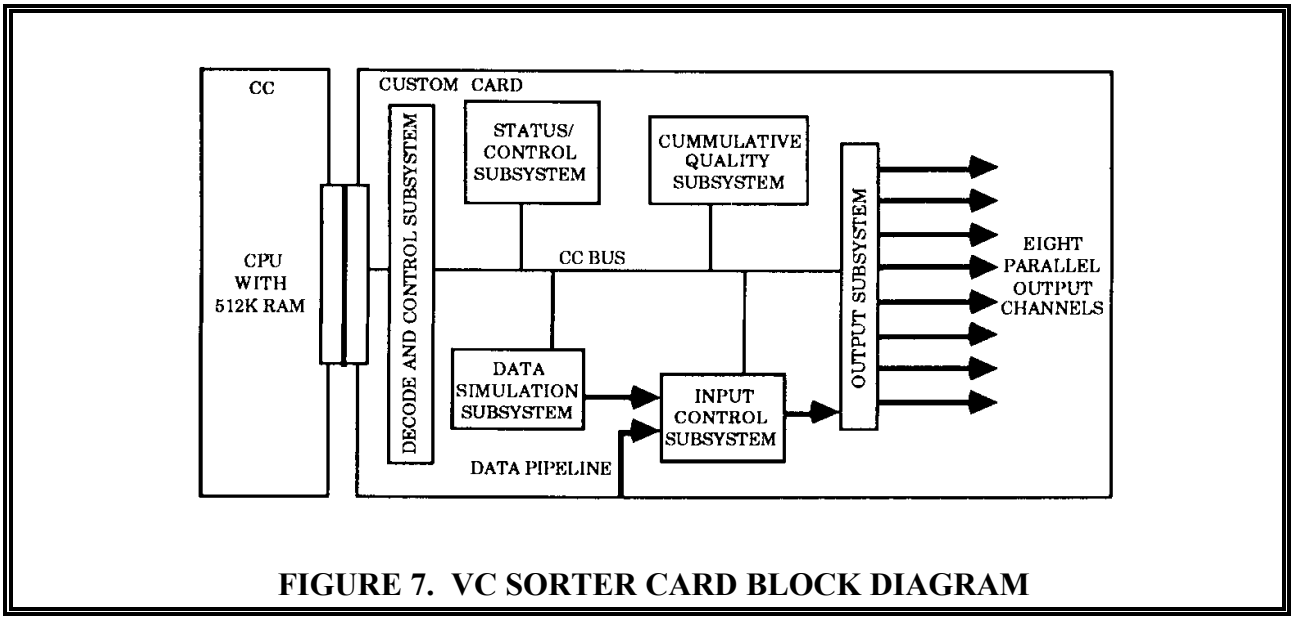

FIGURE 7. VC SORTER CARD BLOCK DIAGRAM

3.4 VIRTUAL CHANNEL MULTIPLEXER CARD

The Virtual Channel Multiplexer Card (VC Mux Card) accepts parallel VCDU's from up to five independent sources. It multiplexes the VCDU's into a composite serial or parallel output stream. The parallel interface could be used for multilevel multiplexing or for backup protection to a line outage system.

3.4.1 DATA FLOW

A block diagram of the VC Mux Card is shown in figure 8. The Decode and Control Subsystem provides the interface to the CC and allows for the memory mapping of all of the other logic subsystems. Incoming parallel data is automatically buffered by each Input

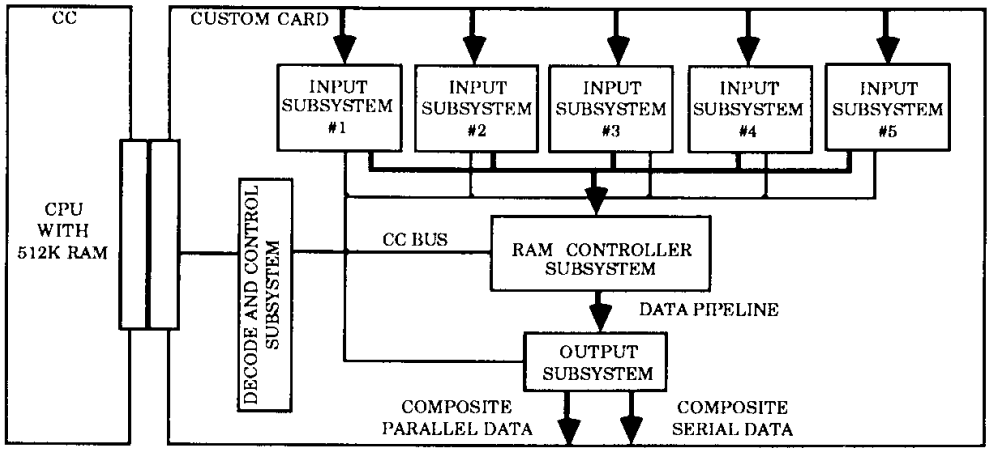

FIGURE 8. VC MUX CARD BLOCK DIAGRAM

Subsystem (1-5) which provides 8K bytes of data storage. When the operational program determines that an Input Subsystem has received an integral number of VCDU's, the RAM Controller Subsystem is activated. After receiving instructions from the operational program, the RAM Controller acts autonomously to transfer VCDU's from an Input Sybsystem to the Output Subsystem. The Output Subsystem automatically outputs the VCDU's from the serial and/or parallel interfaces. The operational program maintains flow control by monitoring readiness of the Input and Output Subsystems to accommodate data transfers. If a break in the data occurs, the RAM Controller may, as an option, insert fill VCDU's to maintain a continuous output stream.

4. SYSTEM HARDWARE ARCHITECTURE

It will now be shown how the components described above could provide the core functions needed for a full performance DIF Return Link Processor. The architecture would use two high speed systems, the Virtual Channel Sorting System (VCSS) and the Virtual Channel Multiplexing System (VCMS). Each system would be built on a standard hardware platform consisting of a VME rack with standard commercial cards. Custom logic cards would be used to perform the system's specific data processing functions. Multiples of the VCSS and VCMS could be configured to perform the main functions of the DIF RLP.

4.1 VIRTUAL CHANNEL SORTING SYSTEM

The architecture of the Virtual Channel Sorting System (VCSS) is shown in figure 9. Serial clock and data is received by the Frame Synchronizer Card, which outputs synchronized VCDU's to the Reed Solomon Card. Routable VCDU's are then passed to

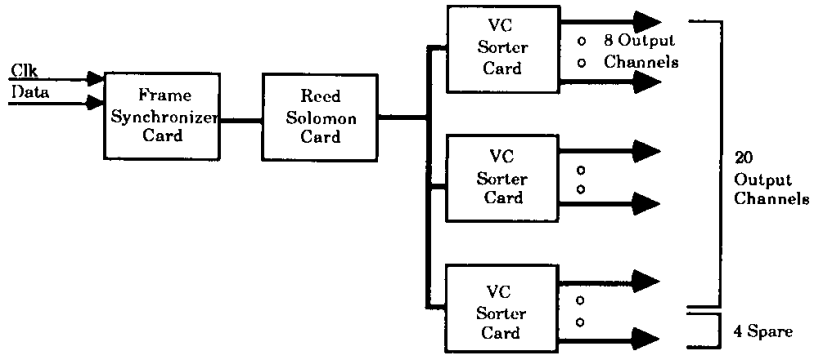

FIGURE 9. VIRTUAL CHANNEL SORTING SYSTEM

multiple VC Sorter Cards. Each VC Sorter Card can sort VCDU's to up to 8 output channels. Up to 8 Sorter Cards could be used in the VCSS for a maximum of 64 output channels. Each VC Sorter Card output represents the set of VCDU's from a space-ground link that are bound for a particular FLD. Three VC Sorter Cards could satisfy the requirement of the DIF RLP for 20 channels, with 4 channels left as spares.

4.2 VIRTUAL CHANNEL MULTIPLEXING SYSTEM

The architecture of the Virtual Channel Multiplexing System (VCMS) is shown in figure 10. The VCMS uses a two level implementation of VC Mux Cards to multiplex data from 24 separate input channels into a composite output stream. Each VC Mux Card can accept data on five independent input channels. Five of these cards are used on the first level for a total of 24 input channels with 1 spare. The outputs of these five cards feed one VC Mux Card on the second level which produces a composite output stream to a FLD.

4.3 DEF RLP CONFIGURATION

Multiple VCSS's and VCMS's can be configured to perform the functions of the DIF Return Link Processor (figure 11). One VCSS is needed for each input channel from a space-ground link. Each output of a particular VCSS is destined for a different FLD, and therefore is connected to a different VCMS. Each VCMS accepts one input channel from each VCSS. These input channels are all multiplexed together into a composite output stream for a single FLD. One VCMS is needed for each FLD supported. As presently defined, the DIF Return Link Processor would accept 24 input channels and output to 20 FLD's.

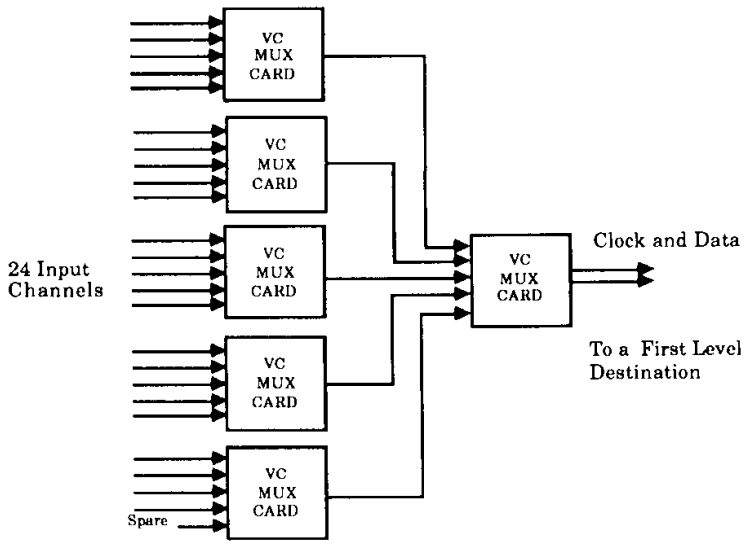

FIGURE 10. VIRTUAL CHANNEL MULTIPLEXING SYSTEM

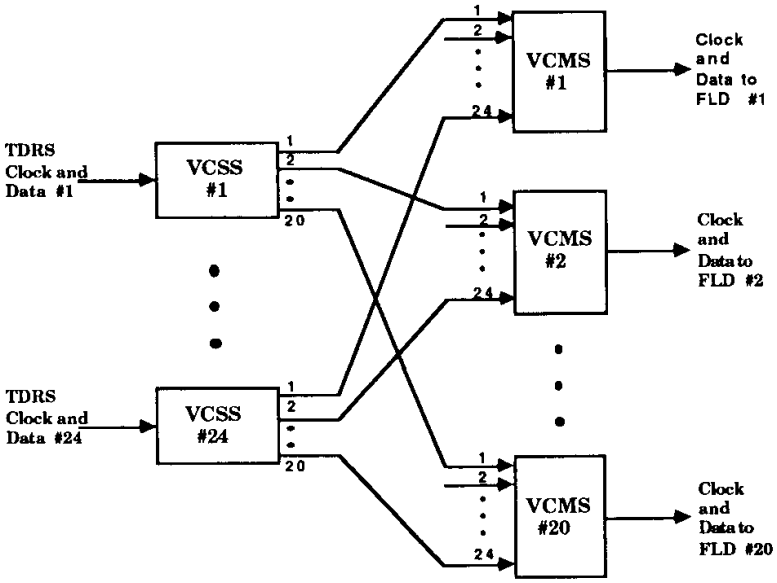

FIGURE 11. SYSTEM ARCHITECTURE

Therefore, the core functions of the DIF Return Link Processor could be implemented using 24 VCSS's and 20 VCMS's. Each of these systems is contained in one 19 inch VME card cage. Four of these card cages fit into one six foot rack. Therefore, an implementation would include six Sorting Racks, each containing four VCSS's, and five Multiplexing Racks, each containing four VCMS's. The fully integrated system would be housed in a total of eleven six foot racks (figure 12).

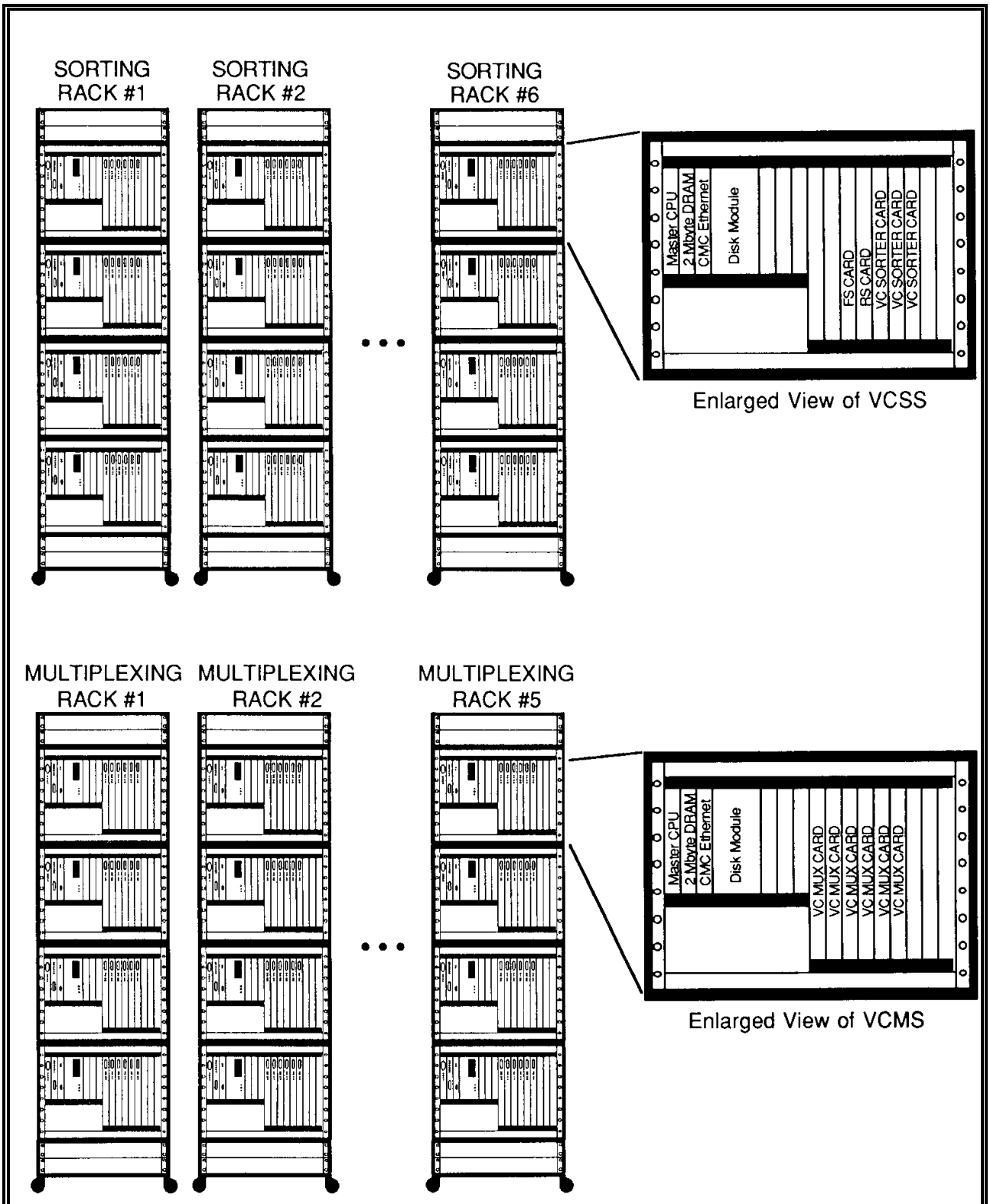

FIGURE 12. RLP HARDWARE IMPLEMENTATION

5. CONCLUSION

This paper has described the architecture and key functions of the DIF RLP. These functions are currently being prototyped at NASA's Goddard Space Flight Center. It has been shown that these prototype elements could be integrated to perform the core functions of a fully operational DIF RLP. Since synchronization, routing, and multiplexing are generic functions, the prototype elements could also be used in other data handling systems.

It is important for NASA to continue to prototype systems such as the VCSS and the VCMS. This ensures that the technology and expertise required to implement such systems will be available in the SSF era.

REFERENCES

1. CCSDS 701.0-R-2A: Recommendation For Space Data System Standards, Issue 2, Red Book, Consultative Committee for Space Data Systems. January 1989.

2. "DIF Cost and Technology Evaluation Study", NASCOM Task S224. Ford Aerospace and Communications Corporation, College Park, MD. December 1987.

NOMENCLATURE

CC	Card Controller
CCSDS	Consultative Committee for Space Data Systems
CMOS	Complimentary Metal Oxide Semiconductor
CPU	Central Processing Unit
CVCDU	Coded Virtual Channel Data Unit
DIF	Data Interface Facility
FLD	First Level Destination
FLS	First Level Source
FS	Frame Synchronizer
GSFC	Goddard Space Flight Center
Kbps	Kilobits per second
Mbps	Megabits per second
NASA	National Aeronautics and Space Administration
NASCOM	NASA Communications
RAM	Random Access Memory
RLP	Return Link Processor
RS	Reed-Solomon
SCID	Space Craft ID

STGT	Second TDRS Ground Terminal
TDRSS	Tracking and Data Relay Satellite System
VCDU	Virtual Channel Data Unit
VCID	Virtual Channel ID
VCMS	Virtual Channel Multiplexing System
VCSS	Virtual Channel Sorting System
VLSI	Very Large Scale Integration
VME	Versabus Module Eurocard Format