20 GHz MULTISTAGE FET POWER AMPLIFIERS*

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ABSTRACT

A GaAs FET power amplifier module operating in K-band is described. The module has integral input and output WR-51 waveguide ports and incorporates a pair of low-loss waveguide to microstrip transitions. Single-stage and multi-stage microstrip FET amplifiers are fabricated on individual copper carrier blocks incorporating in-package impedance matching. Six packaged amplifiers are cascaded to achieve a 0.5 W, 30 dB gain amplifier module operating over the 17.7-20.2 GHz band.

INTRODUCTION

Recent improvements in GaAs power FET device performance have made possible the realization of solid state amplifiers operating at high microwave frequencies including K-band (18-26 GHz).[1] The potential higher reliability and simpler power supply requirements of such amplifiers when compared to their vacuum tube counterparts make them attractive for medium power (~ several watts) airborne and space applications including satellite communications. In this paper we discuss the device and circuit design considerations and the results obtained for experimental high gain, 0.5 W FET module amplifiers operating in the frequency range of 17.7 to 20.2 GHz. The module amplifiers consist of cascaded single-ended microstrip FET stages with up to six stages producing a gain of 30 dB. In-line WR-51 waveguide flanges are utilized at the input and output ports of the module housing as well as low loss waveguide to microstrip transitions which provide efficient coupling of the waveguide TE_{10} mode to the microstrip mode used in the FET stages. The modules can therefore be easily interfaced with other waveguide circuit components.

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* This work is supported by NASA (LERC) under Contract No. NAS3-22504.

The largest single chip FET device used in our work has a gate width of 1.35 mm and is capable of achieving at least 450 mW of saturated output power with 4 to 5 dB gain across the 17.7 to 20.2 GHz frequency range. To obtain more linear operation at the same output power level, or to achieve still higher saturated power, chip level and circuit level power combining must be used. We discuss microstrip circuit power combining of two 1.35 mm gate width FETs on a single copper-block or "package" which is used as the output stage of the six-stage module. In-package impedance matching using lumped and distributed circuit elements is incorporated in the individual packaged amplifier stages. These stages can be individually tested and easily removed and replaced in the module amplifier housing. The feasibility of circuit power combining such modules for achieving still greater output power is also discussed.

20 GHz GaAs FETs

GaAs MESFET's have demonstrated the capability of producing several watts of output power with useful gain through Ku-Band frequencies (up to 18 GHz).[2] A necessary requirement for obtaining these performance levels has been the optimization of device structures and material parameters such as epitaxial doping level and thickness, channel structure, etc. In order to obtain high gain and output power at even higher frequencies, it is necessary to re-evaluate these parameters. In this section we describe the devices responsible for the performance of the amplifiers reported below, and we discuss the optimized values of the different channel parameters for 20 GHz operation. The material growth, device structure, fabrication and characterization are described first, followed by the performance results.

Material Growth Device Structure and Fabrication

All of the GaAs MESFET'S epitaxial layers were grown by vapor-phase epitaxy using the $GaAsC1_3$ H_2 system. Two layers are grown sequentially on a Cr-doped substrate: an undoped buffer layer 1 or 2 μm thick is followed by the sulfur doped n-type active layer. The active layer is grown thicker than necessary (1 or 2 μm) and then thinned anodically. This self-limiting process reduces the epitaxial layer thickness to a value close to the optimum for device fabrication and eliminates any non-uniformity in sheet resistance. Typically, following anodic thinning and before gate definition, 300 μm devices fabricated on the slice have saturated currents of 220 to 240 mA with a standard deviation of 5% across a 12 cm^2 slice.

Figure 1 shows the devices during fabrication. Each field has six devices of the π-gate structure, one 300 μm, two 600 μm and three 1350 μm gate width devices. A detailed view of the 1350 μm device is shown in Figure 2. Source and drain contacts are alloyed AuGe/Ni with a 5 μm separation. The gate is a single 1.35 mm stripe with nine gate pads.

In effect each gate pad feeds two individual 75 μm wide gate fingers. This unit gate width seems to be optimum for high frequency operation. If the individual gate fingers of a GaAs FET are made too wide, the microwave signal will suffer excessive attenuation and phase-shift while propagating down the gate stripes and the performance will be degraded. The gates are defined exclusively by electron beam machine and electron beam evaporated Ti/Pt/Au is employed as gate metal. The slice is etched immediately prior to placing it into the evaporator in order to recess the gates below the epitaxial surface and reduce the device current to the correct value. For K-band operation it is important to have a gate as short as possible without increasing the resistance of the stripe. The best compromise is a 0.5 μm long and 6000 Å thick gate.

A large source grounding bar extends the length of the chip on one side and the sources are connected to it by plated gold air bridges. Four drain pads are used.

Device Characterization

RF S-parameter measurements demonstrate the reduced parasitics of the multiple feed gate design (π-gate). The reverse isolation $|s_{12}|$ is 3 dB higher than with a similar gate width device having the parallel gate structure. The better isolation is due to lower source lead inductance and lower gate-drain feedback capacitance (C_{gd}). The source grounding bar is connected to ground by a low inductance mesh or a sheet of solder and its large area ensures a very low source lead inductance per unit gate-width. Equivalent circuit calculation from the S-parameters demonstrate that the very small pads of the present design coupled with their wide spacing, reduces the gate-to-drain capacitance C_{gd} over the parallel gate design. It is thought that performance is also improved by more symmetric feeding of the gates. Another advantage of this structure for high frequency operation is that with the large number of widely spaced gate and drain pads, the effective bond wire inductance can be very low and the device input and output capacitances can be resonated at very high frequencies.

Extensive study and previous experience at Ku-band helped determine the optimum doping level for K-band operation. In general, the small signal gain increases with higher epitaxial layer doping levels. However, for the highest doping levels, the limiting factor for the output power is the gate breakdown voltage which decreases with increasing doping level, n. For 20 GHz; operation best results have been obtained with values of n between 2 and 2.3×10^{17} cm^{-3}.

Device Evaluation and Performance

Complete evaluation and testing of a slice is done first at 15 GHz on 300 µm devices for simplicity. It has been observed that performances scale almost exactly from 300 µm to 600 µm gate width devices.

The best results obtained on 300 µm gate width devices of several slices are as follows:

- small signal gain with 5 dBm input power and 5 V on the drain: 9.5-10.5 dB
- output power with 6 dB gain and 8 V on the drain: 23.2 dBm
- output power with 4 dB gain and 8 V on the drain: 23.7 dBm

Devices from the best slice had 24.2 dBm output power with 4 dB gain, 9.5 volts being applied on the drain. These results are summarized in Figure 3 where the output power is plotted as a function of the input power.

These results at 15 GHz translate into performances reported in the circuit section from 17.7 to 20.2 GHz. For reference we mention below narrow band results, previously reported in (1), obtained with devices of the same type. A 1350 µm device had an output power of 675 mW with 5.8 dB gain and 18% efficiency at 20.5 GRz as an amplifier. Another device bonded as an oscillator had the performance recorded in Table I. Up to 200 mW was obtained at 25 GHz. With two devices bonded in parallel, 1 W output power was obtained at 19.7 GHz with 4 dB gain and 17% efficiency. At higher frequencies, breadboard single-stage amplifiers using 1350 µm devices have achieved 355 mW with 4.5 dB gain at 22 GRZ and 200 mW with 4.0 dB gain at 23 GHz.

AMPLIFIER DEVELOPMENT

A Low loss Waveguide to Microstrip Transition

A waveguide-to-microstrip transition was designed for adapting WR-51 waveguide to the microstrip transmission lines of the FET amplifiers. The transition circuit makes use of gradually tapered “fin-line” ridges on opposite sides of RT duroid dielectric substrate.[3,4] The duroid substrate provides a reliable, low-loss interface. Figure 4 illustrates the transition test circuit, with back-to-back transitions, and the test fixture used for microwave testing. Good electrical contact of the waveguide to the circuit is made with mechanical pressure without the risk of substrate breakage as with the case of fused quartz.

Low insertion loss and good return loss are achieved using 0.25 mm thick RT duroid ($\epsilon_r = 2.2$) with 0.5 oz rolled copper cladding. Shown in Figure 5, the insertion loss of two

transitions back-to-back is less than 0.5 dB across the 17.0 to 22.0 GHz frequency band. Return loss is greater than 18 dB across the entire band. The shape of the fins was experimentally optimized and required a small amount of tuning in the vicinity of the fin overlap. The final design, with the additional tuning incorporated, provides very reproducible performance. To be certain that the microwave energy was actually propagating in the microstrip mode in the center portion of the test circuit, a metal block was positioned in the waveguide test fixture at the location of the ground plane under the microstrip. No change was observed in insertion loss or return loss, indicating that the waveguide was indeed cutoff by the back ground plane of the transition circuit.

Multi-Stage Amplifier Design

Amplifier stages, for use in the 17.7 to 20.2 GHz band of frequencies, have been constructed utilizing several different sizes of FET devices. To increase the cascaded six-stage efficiency, the FET chips have gate widths graduated in size from 150 micron gate width devices for the first stages to a pair of 1350 micron gate width devices for the sixth stage. Figure 6 shows a block diagram for the nominal gain and bias schedule of the six-stage amplifier. Amplifier circuit design was done with scattering matrix parameters that have been generated from device equivalent circuit models. These lumped element models have been derived from RF characterization data measured on an automatic network analyzer (ANA) over the 2 to 18 GHz band of frequencies. In addition, slotted line measurements were made at selected frequencies to confirm the accuracy of the ANA data. Figure 7 shows a typical example of the equivalent circuit model for a 600 micron gate width FET. This method of device characterization produces acceptable results when the amplifiers are to be operated in a linear mode. However, when the amplifiers are to be operated in a power saturated mode, this characterization is used only as a starting point for the circuit design. Observations have borne out the fact, especially at lower frequencies, that there is very little change in the input equivalent network of the device when going from a linear mode of operation to a power saturated mode, while there is a significant variation in the output network. There are several methods currently being used in the industry for determining the variation in large signal output impedance as a function of drive level for the FETs. These include the "load pull method".[5], computer aided output power vs load impedance mapping methods[6] and empirical analysis. For our applications the latter technique was considered to be the most practical method to use at K-band frequencies. Nevertheless, all of these methods require extreme diligence in order to obtain reliable results. The amplifiers are first designed on a single stage basis, assuming an ideal 50 ohm generator and load, using a computer optimization routine that is commercially available. Once acceptable results are obtained the modeled stages are then cascaded and further selected optimization is performed to obtain the desired characteristics for the multistage amplifier. Once an acceptable design is obtained a first pass evaluation prototype circuit is fabricated for the various stages. These circuits are

then evaluated on the bench under actual operating conditions and compared to the circuit model predictions. Seldom do the evaluation circuits give the exact computer predicted performance, especially, at the higher frequencies. This is due primarily to circuit parasitics and variations in device characteristics that have not been included in the model. As a result several iterations are usually performed to converge upon a reproducible circuit.

Figures 8 through 11 and Figure 13 show the performance of the various single and multistage amplifiers used in the six-stage amplifier module. Figures 8 and 9 show the performance of 150 μm and 300 μm single stage amplifiers operating in an ideal 50 ohm environment. Figure 10 illustrates both the transmission gain and the input return loss of the first four amplifier stages. The centerline reference for this photograph represents 20 dB of linear gain (1 dB per division) for the top trace, and 0 dB reference (10 dB per division) for return loss indicated by the lower trace. Band edge markers appear as notches in the traces. Figure 11 corresponds to a single 1350 micron gate width device used in the 5th stage. A gain of 6 ± 0.5 dB is obtained across the band.

A pair of 1.35 mm gate width FETs are used for the sixth stage circuit block. Figure 12a shows the circuit layout for the sixth stage amplifier, while Figure 12b shows the corresponding circuit schematic. The quartz substrates on which are etched the microstrip distributed circuits, the discrete impedance matching capacitors, and the pair of 1.35 mm FETs are mounted on a copper carrier block or package whose dimensions are 1.3 x 0.64 x 0.62 cm. Precise lengths of bond wires (25 μm diam.) interconnect these three elements and are used as the lumped inductors in the impedance matching circuits. The "in-package" lumped and distributed impedance matching networks transform the 50 Ω input impedance to a level of about 2 or 3 Ω to each 1.35 mm FET. A simple Wilkenson-type combiner, less the isolation resistor, is used to power combine the two FET chips.[7] Each half of the circuit between the 71 Ω lines of the Wilkenson power splitter/combiner combination is simply the circuit used for the fifth stage amplifier where a single 1.35 mm gatewidth FET is utilized. Figure 13 shows the measured gain versus frequency result for the sixth stage amplifier with the nominal input power level of 23.4 dBm. A linear gain of 4 dB and over 0.5 W output power is obtained over most of the band. In the power saturated mode the 1 dB gain compression point occurs at about 800 mW (29 dBm). The somewhat lower gain of these single stage amplifiers utilizing the pairs of 1350 μm devices is due in part to the additional losses associated with the Wilkenson combiner and impedance matching networks and in part due to the difficulty of physically realizing an exactly identical circuit configuration for each 1350 μm FET. The latter problem results in amplitude and phase imbalances between the two FET chips which lowers the power combining efficiency and gain.

Finally Figure 14 shows the six stages assembled in the module housing and interfaced with the waveguide to microstrip transitions. The housing cover is removed for the photograph but must be in place to test the amplifier, since it forms an integral part of the transition. Figure 15 shows the gain versus frequency characteristic for the six stage amplifier. At the nominal input level of -3.8 dBm the gain at mid-band is 31 dB with an output power of 562 mW (27.5 dBm). The overall peak DC to RF efficiency is 9.7%. As seen in the Figure the first 250 MHz of the band has a substantial gain roll-off. This problem has been traced to some rf ground continuity problems between the copper carrier blocks, and some interstage interaction not taken into account in the computer modeling. These problems are being corrected and it is expected that subsequent six stage module amplifiers will have a gain of 30 dB ± 2 dB across the entire 2.5 GHz band.

Module Power Combining Considerations

Because of increased microstrip circuit losses and inadequate gain of the FET devices, it becomes difficult and impractical to parallel more chips on a given circuit block (e.g. the sixth stage) to achieve higher output power. Devices with larger gate widths per chip are also disadvantageous since the impedance levels become even lower and the chip dimensions become a substantial fraction of the operating wavelength. The former consequence results in greater losses, while the latter problem causes lower gain due to uneven gate drive and phase mismatch in the FET device.

A possible alternative to achieving greater power at 20 GHz is to power combine amplifier modules of the type described above using a rectangular waveguide (e.g. WR-51) divider/ combiner network. Rectangular metal waveguide offers minimum loss and at 20 GHz even a complex divider network utilizing several levels of binary power splitting can be made quite compact.[8] It is expected, for example, that a sixteen-way waveguide divider network using four levels of 3 dB power splitting employing magic tees will have a maximum excess insertion loss of 0.8 dB at the band edges and 0.3 dB at band center for the 17.7-20.2 GHz frequency range. The size of a single divider (or combiner) manifold is about 19 x 19 x 3.2 cm. Because of the "in-line" mechanical design of the multi-stage 0.5 W amplifier modules it is relatively straightforward to interface the modules with a pair of waveguide manifolds which split the input power evenly to each module, and after amplification combine the power into a single output. If magic tees are used as the 3 dB power splatters then the fourth port of the tee can be terminated and thus provide isolation between modules. The key to the success of such a scheme is the degree to which the phase and amplitude characteristic of each module can be matched from unit to unit. Schemes to adjust the phase of each module to within ± 20° and the amplitude to ± 1 dB are currently being developed. The power goal for the sixteen module power combined amplifier is 7.5 W.

CONCLUSIONS

GaAs power FETs designed for 20 GHz operation have been incorporated in a single-ended six-stage amplifier module which yields up to 30 dB gain at an output power of 0.5 W and 9.7% efficiency in the frequency range of 17.7-20.2 GHz. The GaAs power FETs used in the module employ gate widths per chip ranging from 150 μm for the first stages, to a pair of 1.35 mm gate width FETs for the output stage.

The FETs use 0.5 μm long electron-beam-defined gates and employ a multiple π-gate feed structure. For the largest gate width FET, the single gate stripe is 1.35 mm wide. For 20 GHz operation this design is superior to other designs used at lower microwave frequencies due to the realization of higher reverse isolation and better gate feed uniformity. Typical performance of these devices, when used in single-stage packaged amplifiers designed to cover the 17.7-20.2 GHz frequency range, include output powers of 450 mW with 4 to 5 dB gain and 15% efficiency.

The design and development of the six-stage module included S-parameter device characterization at lower microwave frequencies, generation of a simplified equivalent circuit model, and extrapolation of the model for use in the 17.7-20.2 GHz band. Using the device equivalent circuits each of the six-stages was first designed and fabricated to operate with 50 Ω source and load resistances across the band of interest with 4 to 6 dB gain. In-package impedance matching facilitates testing of each stage separately. The design and realization of the single-ended six-stage cascade was based on the single stage circuits as a starting point and modifying these to account for interstage interaction. Computer circuit optimization and final empirical optimization of the actual microstrip circuits was used for the design and fabrication of the six-stage network. For comparability with WR-51 waveguide, a low-loss waveguide to microstrip transition using RT duroid substrate material to support an antipodal fin line transition design is incorporated into the module amplifier at input and output. For one transition the insertion loss from 17.0 to 22 GHz is less than 0.25 dB. This in-line design allows modules of this type to be easily and efficiently interfaced with waveguide circuit power combining networks. Work is currently in progress to power combine sixteen modules to achieve a 7.5 W FET amplifier at 20 GHz. An amplifier of this type would be appropriate for future communications satellite transmitter applications.

ACKNOWLEDGEMENTS

The authors wish to thank Glen Westphal for supplying the GaAs material, Pete Lindsley and Charles Moore for helpful discussions, and Wanda Johnson, Alice Miramontes, Larry Duke, and Tom Kaiser for technical assistance.

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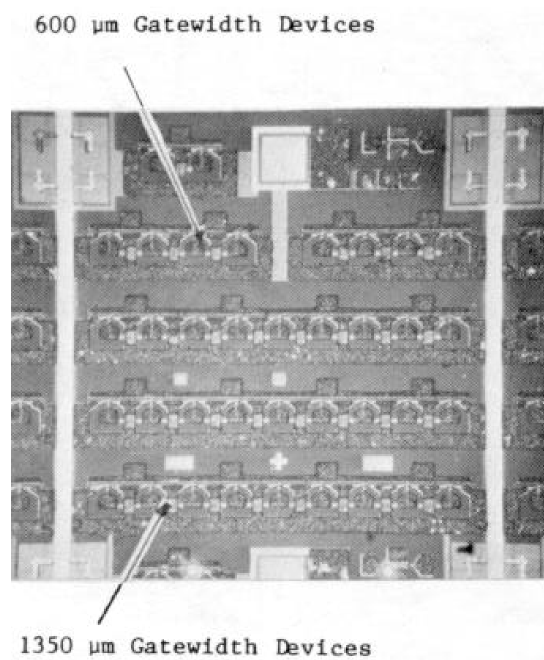

Figure 1. π-Gate Devices During Fabrication

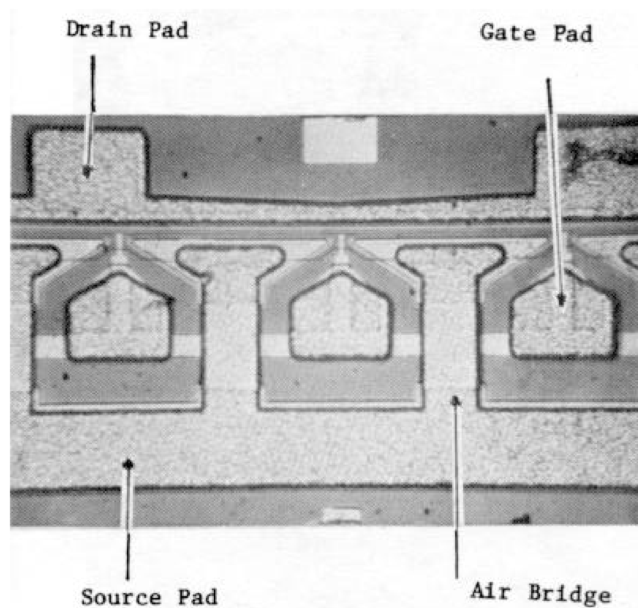

Figure 2. Detailed View of a 1350 µm Device

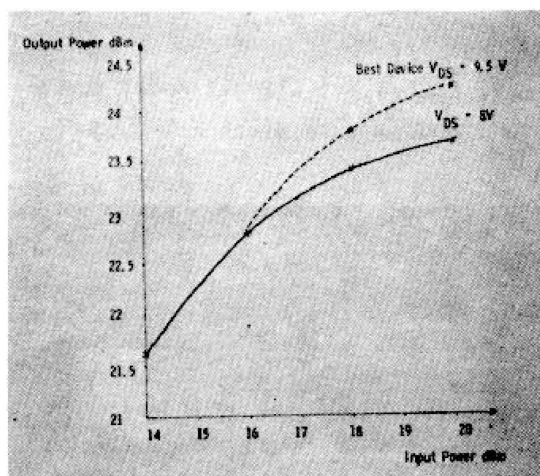

Figure 3. Output Power Versus Input Power for a 300 Gatewidth Device at 15 Ghz

FREQUENCY (GHz)	OUTPUT POWER (mW)	EFFICIENCY (%)
20.2	250	7.6
23.5	220	6.8
25.1	200	6.3
26.1	150	4.6
26.6	105	3.4

Table I. Oscillator Performance of 1.35 mm Gatewidth Device

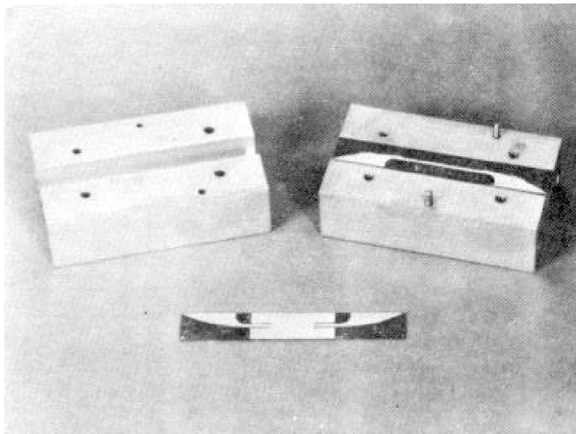

Figure 4. Back to Back Waveguide to Microstrip Transition Test Circuit

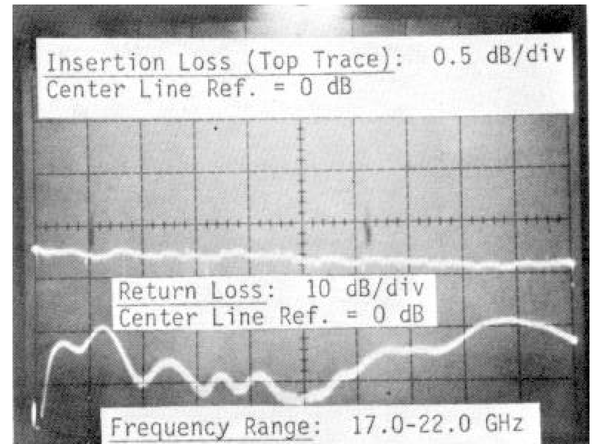

Figure 5. Frequency Response of Transition Test Circuit

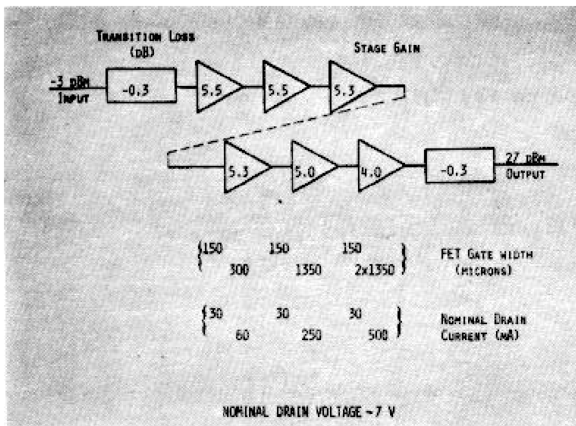

Figure 6. Block Diagram of Six-Stage Module Amplifier

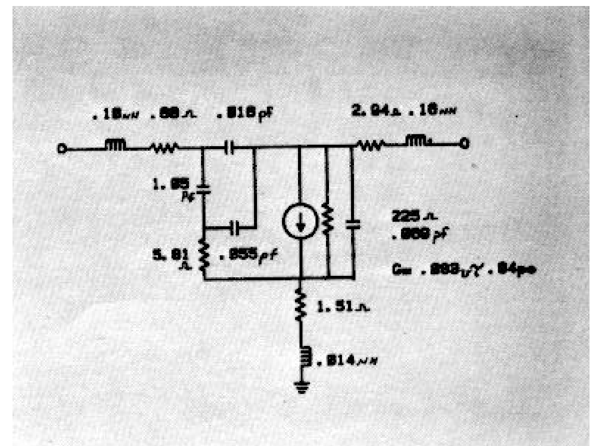

Figure 7. Equivalent Circuit Model for a 600 μm Gate Width FET

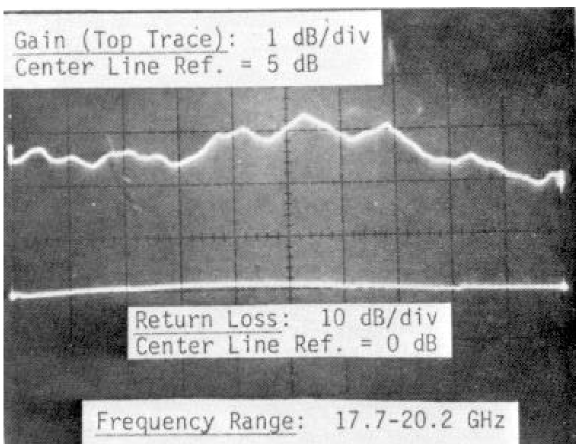

Figure 8. Small Signal Gain Characteristic for 150 μm Amplifier

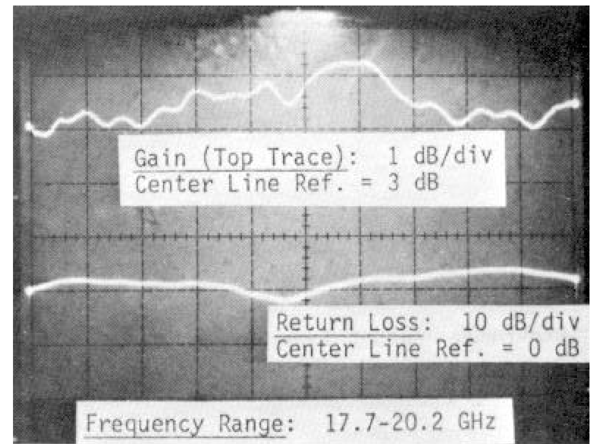

Figure 9. Small Signal Gain Characteristic for 300 μm Amplifier

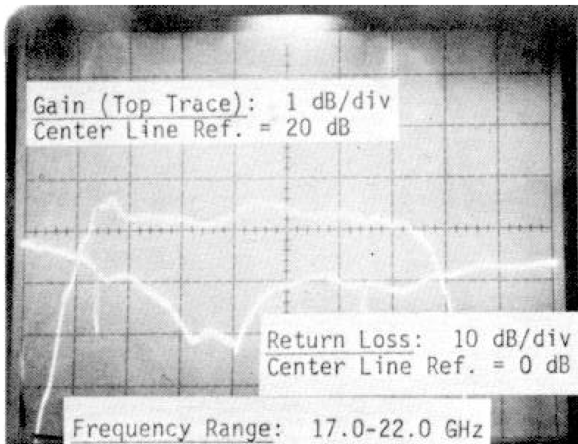

Figure 10. Small Signal Gain Characteristic for First Four Stages

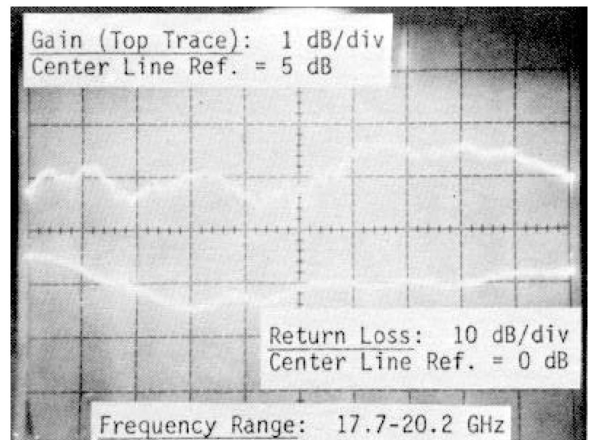

Figure 11. Gain Characteristic for 1.35 mm Amplifier (P_{in} = 18 dBm)

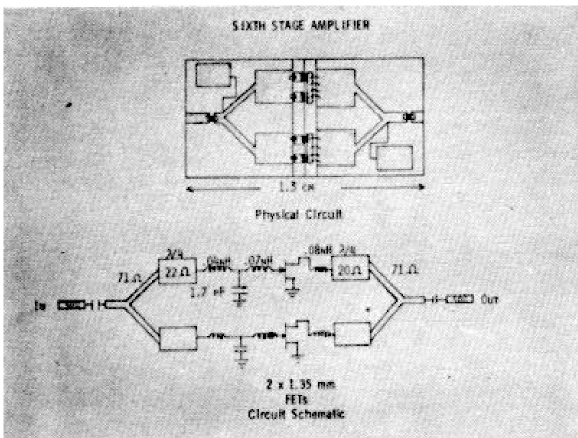

Figure 12. Circuit Layout and Schematic for Sixth Stage

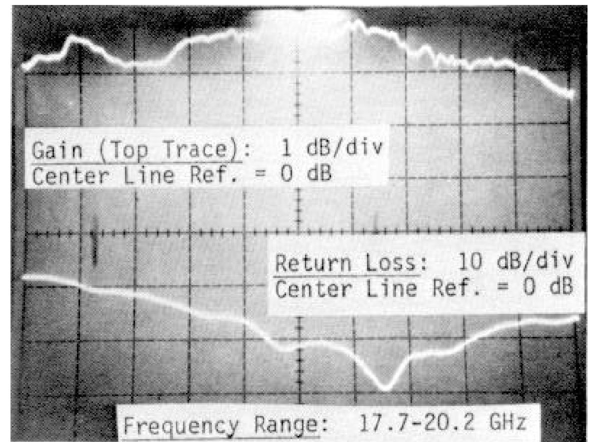

Figure 13. Gain Characteristic for Sixth Stage (P_{in} = 23 dBm)

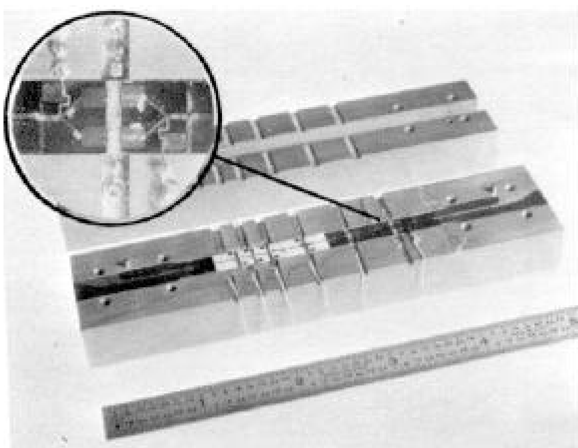

Figure 14. Six-Stage Module Amplifier

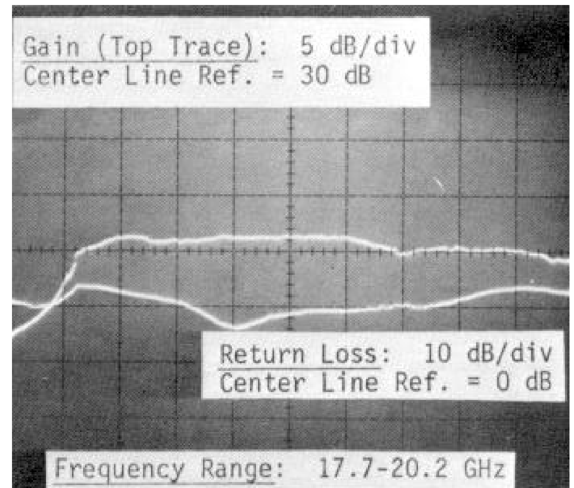

Figure 15. Gain Characteristic for Module Amplifier (P_{in} = -3/9 dBm)