A CHARGE-BALANCING INCREMENTAL ANALOG TO DIGITAL CONVERTER FOR INSTRUMENTAL APPLICATIONS

D. Zrilić*, D. Skendzić, S. Pajavić, R. Ghorishi, F. Wu, G. Kandus**

BOSTON UNIVERSITY

Department of Electrical Engineering
44 Cummington St.
Boston, MA 02215

ABSTRACT

A switched-capacitor technique for realization of one bit serial A/D converter is presented. A conversion accuracy that is higher than 15 bits can be expected from its integrated realization. Results of simulation are presented. It is shown that arithmetic operations on bit serial signals are possible. Using arithmetic operations on delta-modulated signals, it is possible to build inexpensive options necessary in instrumentation.

Key words: switched-capacitor, delta-sigma modulation, delta-full adder.

INTRODUCTION

The basic circuit diagram of the delta-sigma modulator (DΣM) and waveforms at relevant terminal points are shown in Fig. la, b, c, d, respectively. The control loop acts in such a way that the average voltage on the comparator input is kept at zero. When no input is applied, the number of positive and negative pulses must be equal. When an input signal is applied, the difference in the symmetrical positive and negative pulses is proportional to the anlog signal. This circuit configuration has made a great impact on low-speed precision instrumentation because of its stability, linearity and accuracy. Due to the fact that the time constant of integration of the DΣM is large, its direct implementation as a continuous time integrator in monolithic form is very difficult. To avoid this problem, Kondoh at al. proposed to use switched-capacitor techniques in dual-slope analog-to-digital converters [1], [2]. We will use similar charge-capacitor strategy to implement a DΣM.

---

*D. Zrilić is a visiting professor from J. Stefan Institute, Yugoslavia.

**G. Kandus is from J. Stefan Institute, Yugoslavia.

CHARGE BALANCING INCREMENTAL MODULATOR CIRCUIT DESCRIPTION

Fig. 2a shows the circuit diagram of the switched capacitor A/D converter. The operation controlled by the nonoverlapping two phase clocks CL and $\overline{CL}$. Switch CLr is used to discharge C_2 in the beginning of conversion period when the modulator is used as an A/D converter. MOS switches are used. V_x is an analog input signal to be converted into positive-negative pulse train with reference voltage V_r. Capacitors C_2 and C_1 act as noninverting integrators controlled with the switches. Capacitor C_r is charged depending on the present value of the output of the integrator which is:

$$V_i(nT) = V_i(nT - T) + C_1/C_2) \ast V_x + (C_r/C_2) \ast V_r$$

The offset free and parasitic-insensitive configuration for the integrator is adopted. The simplified block diagram of this A/D converter is shown in Fig. 3. Positive and negative pulses are processed in a 2^n up/down counter. For DC or quasi DC signals, the modulator generates a repetitive pulse pattern. The counter is allowed to count during N periods of the clock. If there are n1 up pulses and n2 down pulses, it is shown in [3] that

$$(n1 - n2) / (n1 + n2) \leq (V_x/V_r) \leq (n1 + 1 - n2) / (n1 + 1 + n2)$$

Above formula is valid if $C_1 = C_r$. Total number of the pulses during conversion period is

$$N = n1 + n2$$

Thus conversion speed is f_c/N, where f_c is clock frequency and resolution is N. For positive values of V_x, the conversion counter contains n=n1-n2 pulses. Thus

$$V_x = (n/N)\ V_r\ (*)$$

The transfer characteristic of DΣM in Fig. 2b is presented. It is evident that conversion accuracy is dependent on the sampling frequency and length of averager (such as the length of the counter in Fig. 3).

Circuit level implementation of DΣM was carried out using CMOS technology and is shown in Fig. 4. The transient behavior of the circuit was simulated using SPICE simulation program. To achieve the level of simulation accuracy desired, the circuit was simulated in different functional pieces. Fig. 5 shows the transient behavior of the switched-capacitor integrator, which performs the initial processing. As can be seen, the

circuit performs a clocked integration (i.e. integrates and dumps). The ratio of C_1/C_2 determines the time constant. The output of this integrator was fed to a counter using a comparator with hysteresis.

CONVERSION ACCURACY

The switched capacitor integrator is configured such that the offset voltage of the Op.Amp. and parasitic capacitance have no effect upon its operations. Also the finite open loop gain does not disturb the charge balance. This is the effect of the holding capacitor C_3 in the integrator. The main error source which limits the resolution is the feed through of clock signals through the parasitic capacitors of MOS switches. In an IC realization using advanced MOS technology, the signal to noise charge ratio (C_1V_x/Q_f) as high as $5x10^4$ can be obtained.

APPLICATIONS

Besides the application of A/D converter as a digital voltmeter, it can be applied to a wide range of applications which require measuring voltages. When some degree of processing is required to derive the measurement parameter, for example, in a resistance measuring circuit, an analog circuit can be made to produce a proportional voltage. We show a simple example in Fig. 6, that

$$V_{in} = (R_1/R_2) \ast (R_X/R_r)V_{ref}$$

Therefore, using (*), we have

$$n = N(R_1/R_2) (R_x/R_r).$$

R_r is a ranging resistor and knowing N_1, R_1, R_2, C_1 and C_n, the desired scaling can be obtained. This pre-processing of the analog signals is common in low cost instrumentation systems. The accuracy is limited by the component accuracy and the analog network can be unstable. Higher performance systems may choose to digitize the primary analog quantitates directly and use digital signal processing to derive the required results. In the resistance measurement example of Fig. 4, such an approach would measure the quantitates V_A, V_B, and V_C and perform the operations $(V_B - V_C)/(V_A - V_B)$ digitally.

We propose an intermediate solution: Linear operations on the primary analog quantities after conversion to the pulse density format, but before the data are assembled into a binary weighted digital word.

Using arithmetic operations on ordinary LDM signals, it is possible to show that arithmetic operations on DΣM signals are also possible. Fig. 7a shows the case of addition

of analog signals x(t) and y(t) using delta full adder [4]. It is possible to conclude that after demodulation, sum of the two analog signals is obtained. It is also possible to conclude from Fig. 7b that this signal is attenuated by factor 1/2 [4]. This problem of attenuation is possible to overcome using techniques of averaging [5]. Using delta full adder, it is possible to show the influence of V_{ref} instability on the accuracy of conversion. Referring to Fig. 8a, it can be seen that when $V_{ref1} = V_{ref2}$, Xn = Yn, then Sn = 1/2 (Xn – Yn) = 0. If Y_{ref2} has some additional fluctuation, it is possible to show that it has some DC offset. Fig. 8b shows this offset for a short period of averaging. Larger periods will smooth the oscillation. Using arithmetic operations on DΣM pulse stream it is possible to construct many useful options which can be implemented in various instruments.

CONCLUSION

A method of one bit analog-to-digital conversion utilizing a switch-capacitor technique is described. This technique allows us to use monolithic IC realization. High tolerance of component is not required. On the basis of our simulation results and preliminary laboratory testing, we expect a conversion accuracy higher than 15 bits.

REFERENCES

[1] K. Kondoh, K. Watanabe, “An autoranging switched-capacitor analog-to-digital converter,” IEEE Tr. on Instrumentation and Measurement, vol. IM-36, No.4, December 1987, pp. 882-897.

[2] H. Matsumoto, H. Shimizu, K. Watanabe, “A switched-capacitor charge-balancing analog-to-digital converter and its application to capacitance measurement,” IEEE Tr. on Instrumentation and Measurement, vol. IM-36, No.4, December 1987, pp. 873-878.

[3] R. J. Van dePlasshe, “A sigma-delta modulator as an A/D converter,” IEEE Tr. on Circuits and Systems, vol. CAS-25, No.7, July 1987, pp. 510-514.

[4] N. Kouvaras, “Operations on delta modulated signals and their application in the realization of digital filters,” The Radio and Electronic Engineer, vol. 48, No.9, pp. 432-438, September 1978.

[5] D. Zrilić et al. “Realization of digital filters for delta-modulated signals.” 30th Midwest Symposium on Circuits and Systems, Syracuse, August 1987, pp. 1343-1345.

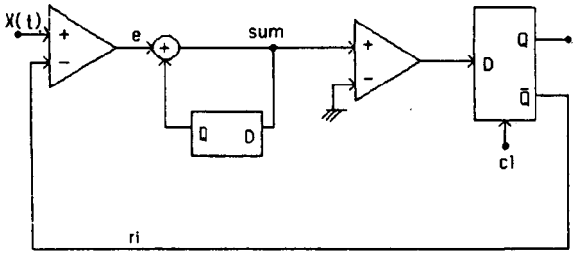

FIG. 1a

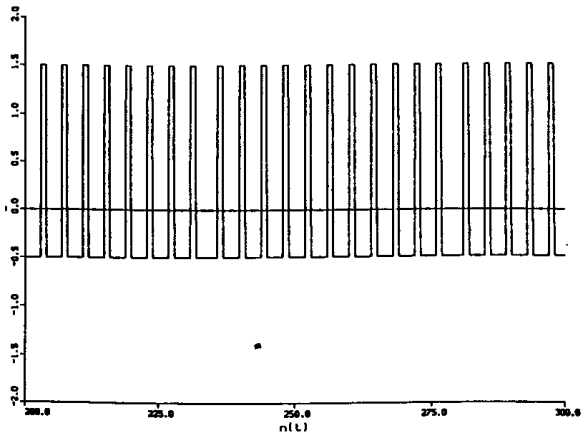

FIG. 1b

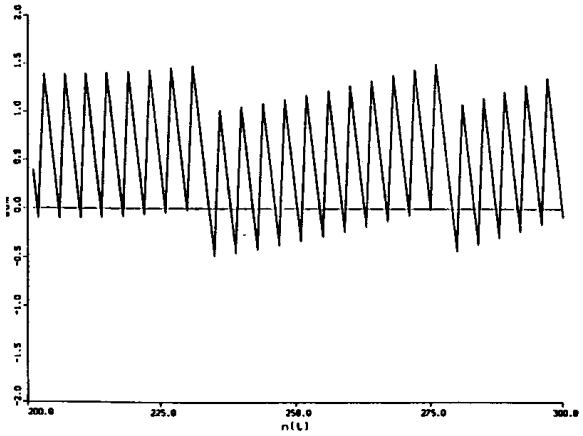

FIG. 1c

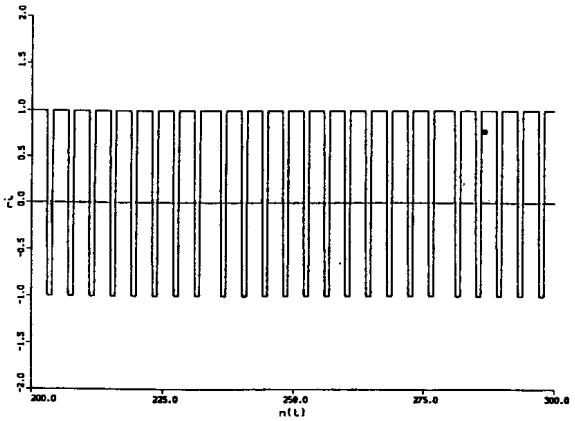

FIG. 1d

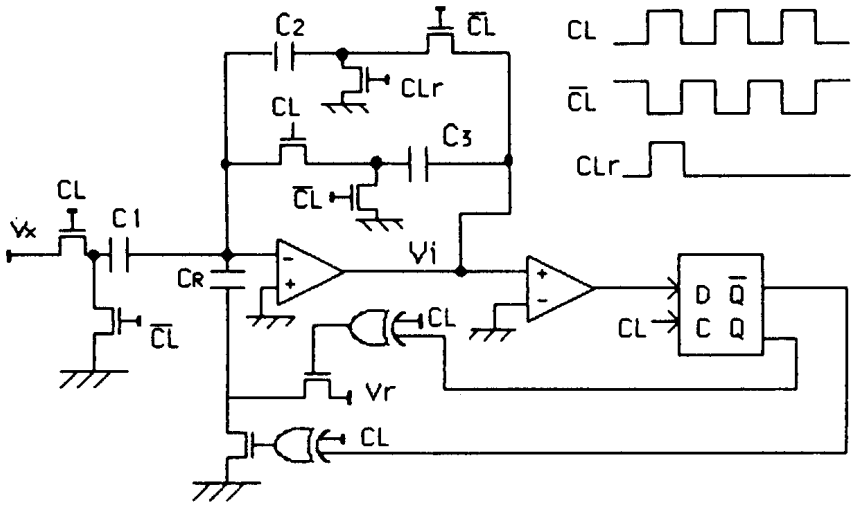

FIG. 2a

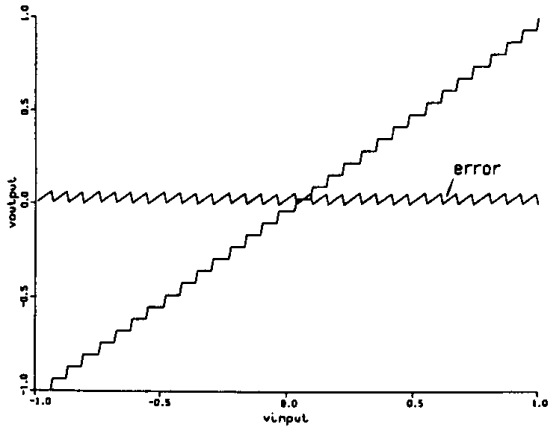

FIG. 2b

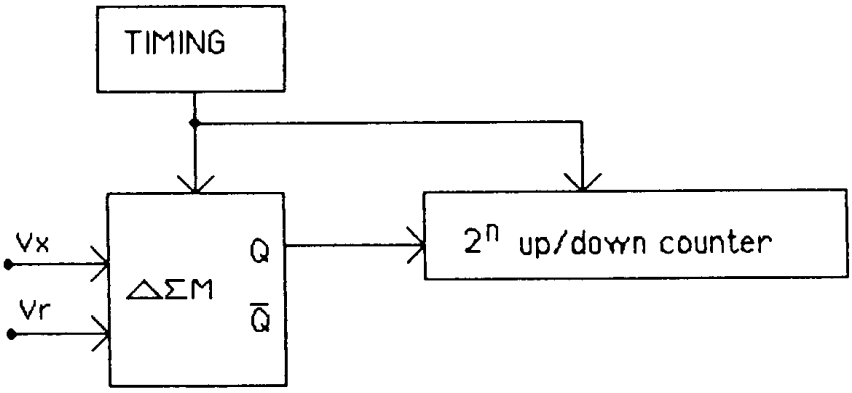

FIG. 3

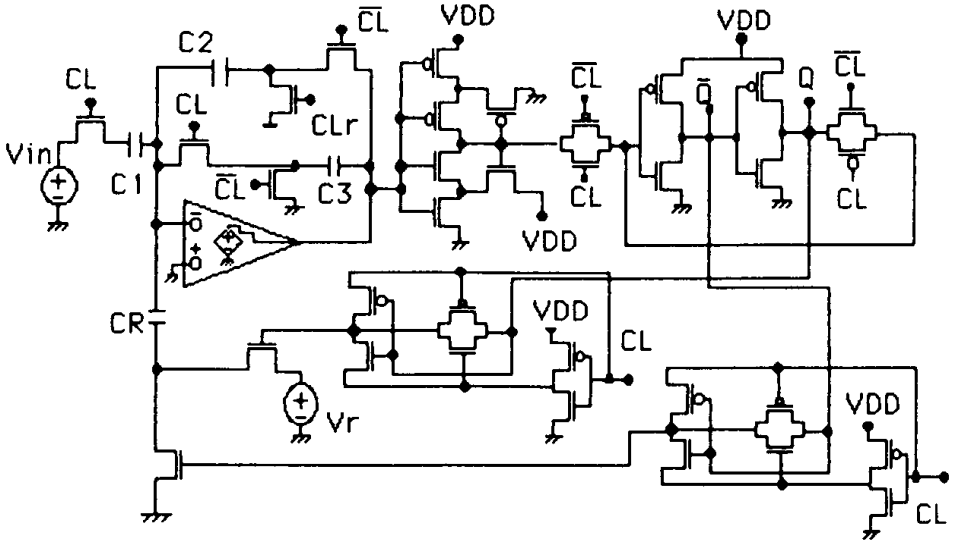

FIG. 4

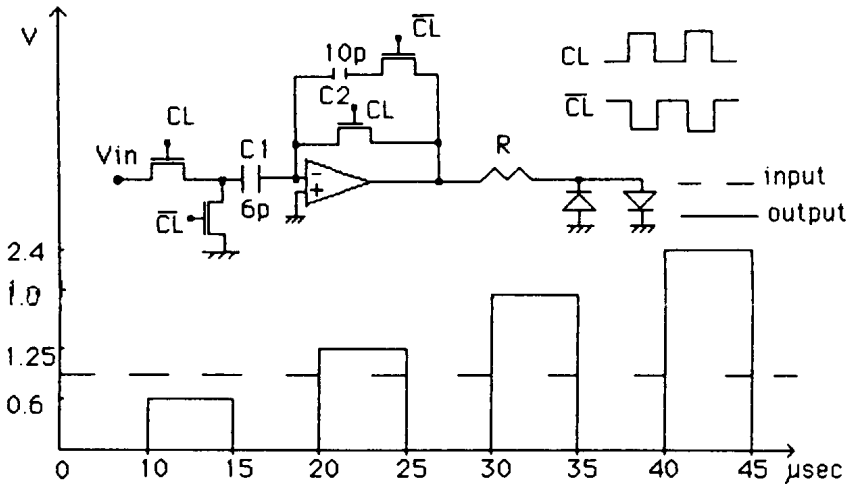

FIG 5

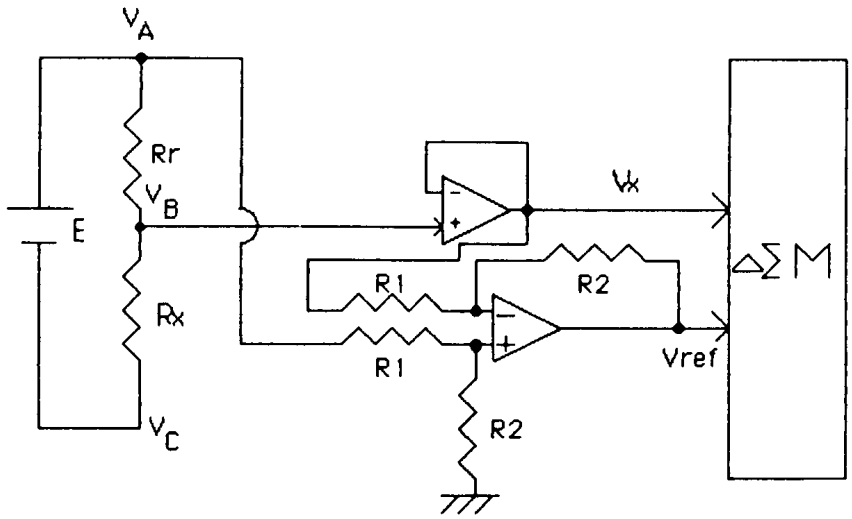

FIG. 6

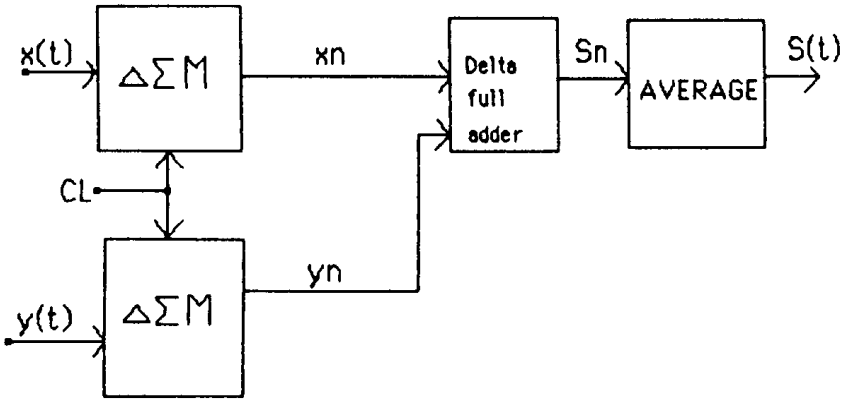

FIG. 7a

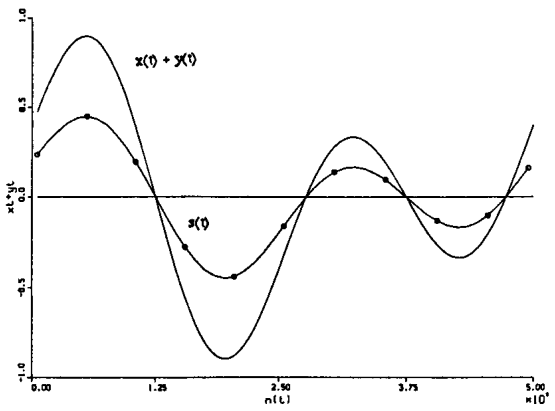

FIG 7b

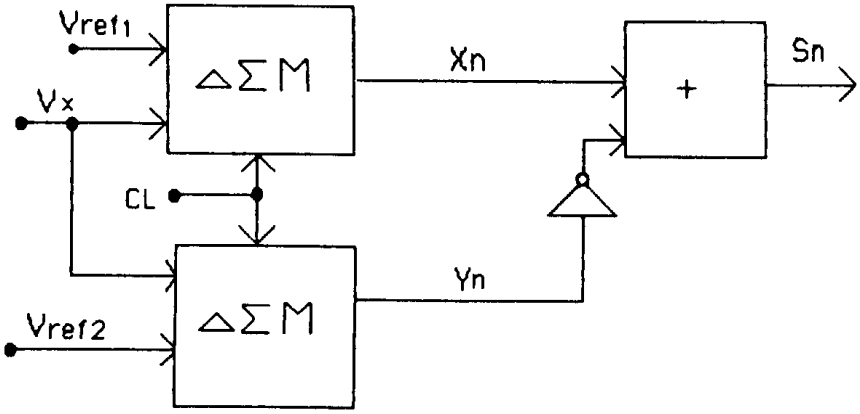

FIG 8a

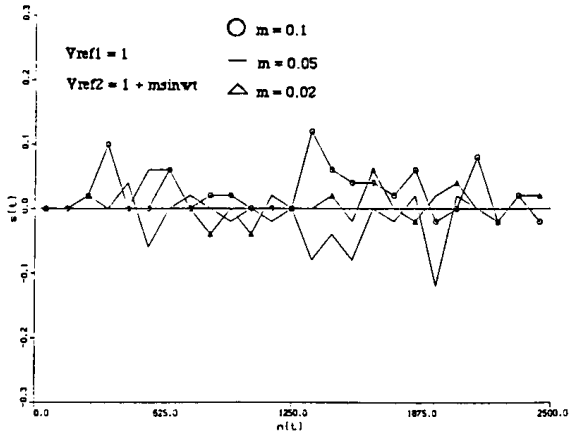

FIG. 8b