uDACS
MICROPACKAGED DATA ACQUISITION
AND
CONTROL SYSTEM

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ABSTRACT

The miniaturization of Aerospace Systems, has created a demand for effective, compact, lightweight, and power efficient General Purpose Stand-Alone Flight Computers, as well as Command, Data Handling and Control Systems, that maintain High Reliability, Full Redundancy, Radiation Hardness, Explosive Processing Speed, Rapid Throughput, and High Accuracy. The innovative design techniques used in the uDACS (Micropackaged Data Acquisition and Control System) offer a unique and comprehensive solution to this quandary.

INTRODUCTION

The uDACS unit is a Modular General Purpose, I/O Intensive, Information Management and Command Processing Control System, designed primarily for use on both Manned and Unmanned Space Vehicles, Missiles, and Aircraft. The uDACS hardware uses an internal computer bus that can accommodate many different CPU, Memory, and I/O Cards. Through the selection of appropriate card types the uDACS can be structured to provide a multitude of configurations ranging from a simple data gathering system (with or without CPU) to a full up distributed fully intelligent network capable of data handling, command processing, and high speed number crunching, that is in closed loop control of a vehicle or an experiment.

The standard uDACS enclosure including power supply is less than 176 cubic inches (6" x 4.88" x 6"), weighs less than 9 lbs, and accommodates up to 1056 I/O channels. An expanded version is available, with up to 2112 I/O channel allocations. The system supports High Voltage Outputs, Low Level-High Level Analog Inputs/Outputs, Discrete Inputs/Outputs, and Serial Inputs and Outputs. In addition the bus arbitration scheme employed supports up to 6 bus masters allowing for computational throughput to be above

200 Mips, when using the Real Time Control Processor Card (RTCPC). Using advanced power management techniques power dissipation is typically 13 to 14 watts when uDACS is completely operational. Power strobing is incorporated to allow standby powers in the 1-2 watt range. Conventional Spacecraft and Aircraft interfaces are supported such as Space Ground Link Support (SGLS), MIL-STD-1553, IRIG, Flexible Multiplexer Demultiplexer (FMDM) etc. as well as MIL-STD-1750A CPU. Using a unique no-fault SCI-Bus up to 28 uDACS units can network forming a distributed system. All I/O cards support built-in-test, allowing for verification of their operation. The uDACS is assiduously redundant, to tolerating all single and most multiple failures while maintaining absolute functionality.

SYSTEM ARCHITECTURE

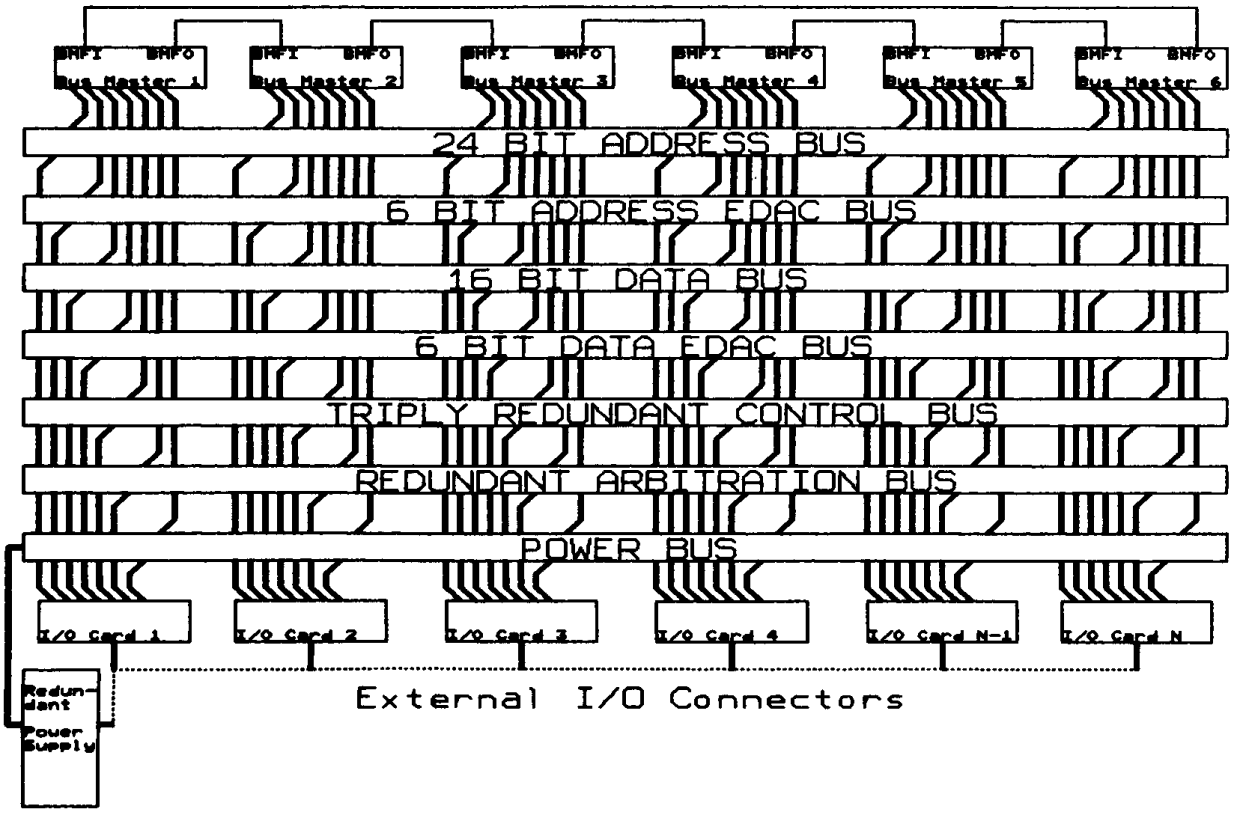
The diverse architecture provides for high computing throughput, along with both fault tolerance and fault recovery. The system is very modular and easily restructurable, allowing for unlimited I/O Configurations. All I/O Cards are cross-strappable. The system supports both internally and externally redundant configurations.

The established methodology consists of an internal parallel bus and an external serial bus. The internal bus allows for communication between different cards inside the housing, while the external bus provides for communication of multiple boxes. This internal bus of the uDACS consists of two separate parallel buses, the Global Bus and the Local Bus.

GLOBAL BUS

The Global Bus (Figure 1) shared by all uDACS Cards, progresses down the motherboard allowing I/O and memory cards to be accessed by a Bus Master. Both the address and data lines are error detected and corrected using a modified Hamming Code. All control lines on the motherboard are triply redundant. Control line validity is resolved by both voting and activity detection circuitry. Two isolated 10 Mhz Clock lines, along with two autonomous clock sources provide sequencing clocks for all I/O cards. Clock validation circuitry provides for automatic switchover in event of clock failure. These features maintain system integrity during multiple failures. The architecture permits the uDACS to be 100% functional, with simultaneous failures on an address bus, a data bus, one of each of the control lines, and a clock line. Auxiliary failure prevention circuitry (Activity Detection) is provided on all control lines allowing the control line receivers to follow on y the lines that have activity on them. This unparalleled feature allows the uDACS to be fully functional (at a 99.99% probability) with two simultaneous failures on all control lines, and coexisting failures on address, data, and clock lines!

Figure 1
MICRODACS BUS ARCHITECTURE



If an error does occur the uDACS Bus Master that is on the global bus is immediately flagged that either a correctable or an uncorrectable error has occurred. The error, the type of error and the location of the error are stored in error status registers that are read by the Bus Master. The last place of data written to or read from the CPU is contained in a Data Verify Register. The last address written to that card is loaded in an Address Verify Register. Should an error occur, the CPU can thus determine if the problem was in the address or data lines or in the syndrome bits. Control Line Status is contained in the CLS Register. This register which is located on the system manager bus master allows the uDACS to monitor the health and status of the control and clock lines. There are also provisions on all uDACS cards that receives/transmits data or commands to accept optional reception/transmission of modified Hamming Syndrome bits, allowing the uDACS to correct for errors in the system it is being interfaced with, or correct for transmission/reception errors.

In addition to the standard Cyclic Polynomial Codes for error coding, the uDACS architecture supports Concantenated, Self-Orthogonal, Convolutional Coding etc. error handling codes.

LOCAL BUS

While any bus master is operating on its own local bus it is isolated from the rest of the uDACS System. The use of the local bus allows a bus master to operate on its local bus while another bus master has requested and is using the Global Bus.

BUS ARBITRATION

The uDACS can support up to six different master cards in the box at any one time. A Master card is designated as any intelligent card (CPU, interleaver, etc.) that can take jurisdiction of the global bus for data transfers. Since more than one master card can be contained in the uDACS housing, a bus arbitration scheme is essential to evaluate which master card can gain authority of the global bus at any given time. There are two bus arbitration schemes deployed:

1. Normal Priority: Time Tagged Prioritized with Four Programmable Levels of Priority
2. Emergency Priority: Highest Priority (Not User Programmable)

NORMAL PRIORITY

The normal bus arbitration is essentially a first-come first-served algorithm in which bus requests are queued with the first bus request processed first and so on. This first-come first-served algorithm is true only if all of the Master cards have the equivalent priority level. In some cases, various Master card will need to have a higher priority over other cards to obtain the bus. The bus arbiter initializes all priorities upon power up and will contain a bus priority mask register which can alter bus priorities on the fly. There are 4 different priority levels. In a unit with Master priority levels, the first-come first-served algorithm is modified to give the highest priority card first chance to take control of the global bus.

The priorities associated with the various master cards are sorted and placed in the bus request queue (time 0). Each item in the bus request queue is time tagged to evaluate how long a bus request has been present in the queue. New bus requests are continually entering the bus request queue times 1, 2. & 3). If the new requests have a higher priority than a lower priority already in the queue, then the lower priority is demerited and waits a longer period of time for service. If the wait for service is determined to be too long by the time tag, then this lower priority bus request is masked to a higher priority (time 5) and resorted in the queue (time 6).

In order to furnish arbitration, the motherboard contains six redundant bus request signals (one signal for each master), six redundant bus grant signals and a redundant bus active or busy signal. A masters need for the global bus is initiated by that master pulling its bus request line low. If the bus arbiter has determined that the request will be serviced, then the arbiter pulls the bus grant line low to that master. The master then responds by activating the busy line low and keeping this line low until its bus cycle time is finished. All of these bus arbitration signals are interfaced to the bus arbitration section of the bus interface gate array (BIGA), contained on all cards. All bus interface gate arrays contain an arbiter but only one arbiter is deemed the bus arbitration unit (BAU). The BAU has full control over all global bus arbitration. Each BIGA bus arbitration sections are daisy chained so that in the event of a BAU failure, full control over arbitration is passed to the next BIGA and then this arbitration section of the next BIGA becomes the BAU.

On master cards, the BIGA also regulates the local bus (on card) in conjunction with the global bus. The BIGA is responsible for tristating the CPU from its local on card bus whenever an off card access of local memory is necessary.

EMERGENCY PRIORITY

CPU failure flags are also located in the BIGA. One failure flag is for local use and another is accessible globally. Upon power up, the flags are both reset. In the unlikely occurrence of a CPU failure, the local flag is set causing a reset of the CPU, if the anomaly then is cleared, this local flag is also reset. If the failure condition cannot be cleared then the global CPU failure flag is set. There are two global flags that initiate task reassignment necessary to obtain system recovery /BMFI-/BMFO and /CMFO.

/BMFI: Bus Master Failure Input - Active low; this redundant signal is a link in a daisy chained bus master arbiter scheme that lets the next CPU Card in the chain Know that a bus master has failed. If the next CPU Card is a redundant CPU with power turned off, it also turns power on.

/BMFO: Bus Master Failure Output - Active low; this signal is the other link in the daisy chain described above. This signal is triggered by either a failure on a Bus Masters BIGA or a time out on the watchdog timer on a bus master. The watchdog timer will be enabled on power up but be allowed to “Long Cycle” for its first cycle.

/CMFO: Common Master Failure Out: This active low signal has two functions: Enable the Redundancy Manager, and Distinguish if the failed bus master is the system manager (contains the Bus Master Arbiter), or not. If the failed Bus Master is the system manager it pulls the /CMFO along with the /BMFO signal low, telling the bus master receiving /BMFO that the system manager has failed. System manager responsibility is relinquished

to this bus master, at least temporarily. Since /CMFO is routed to all bus masters all bus masters are cognizant that a failure of some bus master has occurred, however only the bus master receiving the /BMFI signal knows exactly which master has failed. If the failed bus master is not the system manager it only pulls /BMFO. The bus master receiving this signal (/BMFI) then immediately pulls the /CMFO signal, enabling the redundancy manager and telling all other bus masters that a failure has occurred. In all cases the bus master receiving the /BMFI signal is immediately granted **EMERGENCY PRIORITY** status.

Since there has been a critical failure, once a bus master has been granted Emergency Priority (E.P.) It no longer must arbitrate for use of the global bus. If the bus master with E.P. requests the global bus it immediately gets the bus. The bus master with Emergency Priority's paramount function during this critical period it to determine if there is adequate processing capability left in the box to fulfill the mission, or to allow the already activated redundancy manager to power up the back-up side of the box, and power down the failed side of the box. If the bus master with Emergency Priority Status determines that there is enough processing capacity left to complete the mission (the bus master only has the amount of time programmed in the redundancy manager's watchdog timer to determine this), three specific data pointers are written to, suspending the time-out process.

REDUNDANCY MANAGER

The Redundancy Manager Card provides totally redundant electronics, including its own redundant power supply to prevent any number of multiple failures causing a uDACS System failure. Engagement of the Redundancy Manager initiates a PO28 pulse for 16 msec activating a latching relay in the power supply powering down the unit. A power down time of 2 seconds is provided for the unit to power down and deactivate all cross-strapped outputs. A second 16 msec PO28 pulse is then fired actuating a latching relay in redundant power supply, powering up the backup side of the unit.

There are 8K x 22 bits of Write Keyed Error Detected and Corrected RAM on the Redundancy Manager. This RAM can be read by the redundant half of the box upon wakeup to determine vehicle/experiment status. The Write Keyed tactic is used to prevent a bus master that has failed from thrashing this RAM before its on-board watchdog timer has timed out. In order to access the Write Keyed RAM, a Bus Master must first write the three appropriate key words in succession to specific addresses on the redundancy manager. The bus master is then and only then given access to write to the RAM. Once that bus masters bus arbitration cycle is complete, the key is reset so the next Bus Master requesting to write data to the Redundancy Manager RAM must repeat the sequence.

A triple voting technique is used on the card to determine if there has been a failure. Any two of the three on-card watchdog timers must time out before the redundant half of the

Box is placed in control. Curtailment of the watchdog timer from switchover to the back-half of the box is instituted by the bus master that has been granted Emergency Priority writing Key Data to three specific addresses on the redundancy manager.

PROCESSING CAPABILITY

The uDACS SYSTEM supports many different type of CPUs: 80C86RH, 80C286, 80386, RTX2000, MIL-STD-1750A. Each of these CPU Cards contain memory, programmable timers, Error Detection and Correction, Vectored/Maskable Interrupt Systems, Bus Arbitration for Multimastered System, Watchdog Timer, clock validation circuitry and their own local bus. Each CPU card can contain up to 128K x 22 bits of RAM and 64K x 22 bits of PROM. OP-Code residing in PROM can optionally be loaded into RAM, allowing for the PROM to be power strobed off. Clock rate control circuitry is contained on static Processor cards allowing for power management during low processing periods.

The 80C86RH CPU/Memory Card is for for use in systems that require modest CPU usage (less than 450 KIPS at 8 Mhz), and where power requirements are low, while the 80C286 and the 80386 are for systems that require greater than 1 MIP of throughput. The 1750A CPU is used whenever MIL-STD-1750A requirements are imposed on a program. The RTCPC, which uses dual RTX-2000 CPUs, is employed whenever an ultra-high performance real time control system is mandatory. Processing speed with the RTX-2000 can approach 40 MIPS using a single card.

SEQUENCER MODE OF OPERATION

The uDACS architecture allows for simple error-free high speed data transfers both internal and external to any module without a CPU in any box. All uDACS Data and Address lines have syndrome bits generated based on a modified Hamming Code. These syndrome bits are passed down the bus internally to any uDACS unit, and can be funneled externally to remote assemblies via SCI bus. The following Command and Data Management functions are implemented in the Sequencer mode.

1. Telemetry Interleaving
2. Uplinked Commands
3. On-Board-Computer(OBC) Commands
4. Acquisition of Data
5. Downlinking of Data

The telemetry interleaver contains an on-card sequencer that can access data according to firmware. Whenever the interleaver requests data it arbitrates for the global bus by: Issuing a Bus Request, Receiving the Bus Grant Signal, and then pulling the Bus Busy Line Low. During this arbitration cycle the CCI/F (Central Computer Interface) sequencer

performs health and status checks by operating on its local bus. The interleaver then issues a command for data to either:

1. Internal I/O Cards Contained Internally
2. External I/O Cards Contained in RU-uDACS

In the first of these two cases the I/O Cards Address is merely presented on the global bus, data read, and then downlinked. In the second instance, the interleaver access the SCI Bus Card and provides a Remote Unit Address and Card Address in the the form of Data to the SCI Bus. This Data is placed in the first of three control I.D. Code registers on the SCI Bus, Data Request Pending. The three I.D. Code Registers on the SCI Bus are:

1. Data Request Pending
2. Data Request Issued
3. Data Received

The interleaver also contains a data request pending register, where it keeps an on-card status of Pending Requests I.D. Codes that have been issued to the SCI Bus.

The SCI Bus then issues a data request from the remote units by sending out the following data: 3 Sync Bits, Parity Bit, 16 Address Bits, and 16 Data Bits. The information contained in the Data Request Pending Registers is passed to the Data Request Issued Registers, and the Data Pending Register on SCI Bus only is then cleared. Data from the appropriate Remote and I/O Card is broadcast back to the SCI Bus Card, and the I.D. Code in the Data Request Issued Register is transferred to the Data Received Registers. The Data Request Register is then cleared.

On an arbitration cycle the interleaver accesses the SCI Bus and reads the data from a remote if there is any I.D. Codes in the Data received register on the SCI Bus. The Data received Registers are then cleared. The I.D. Code read from the SCI Bus is correlated with I.D. Codes contained in the Pending Request register on the interleaver, if it matches any of these, the data is downlinked, if it dose not match data is not downlinked. During this arbitration cycle all data received from SCI Bus, both I.D. Codes and Raw Data from remotes is written to global memory on the master sequencer card. This operation will be explained shortly.

Commands that are Uplinked to the system enter the uDACS Master through either the Decryption Unit - For Receiving Encrypted Commands or through a Transponder Interface - For Receiving Unencrypted Commands. Should commands enter the system through the Decryption Unit, they are transferred to registers on the Transponder Interface after decryption. When a command is uplinked, the transponder interface card issued an

interrupt to the CCI/F sequencer. The sequencer then comes and deciphers the command from the transponder I/F Card. Commands issued to the system from the Central Computer enter the uDACS Master through the CC I/F card. When a command is sent to the uDACS the CC I/F card issued an interrupt to the master sequencer. The sequencer then comes and reads the command from the CC I/F Card.

Formerly, it was stated that the interleaver writes data to the CCI/F card each time it receives data form an RU. This methodology is employed so should either the Central Computer or the Transponder need information from a remote its request as stated above is transferred to its appropriate I/F Card and then read by the sequencer. If this request is for information from a remote the sequencer access the SCI Bus card. As with the interleaver this Data is placed in the first of three control I.D. Code registers on the SCI Bus, Data Request Pending. At this time a comparison is made between this I.D. Codes and all other I.D. Codes in all three registers. If it matches any of the other I.D. Codes this I.D. Code is cleared and thus not issued. This simply means that another device has requested data from the same I/O Card in a remote and the command need not be issued twice.

The CCI/F sequencer also contains a data request pending register, where it keeps an on-card status of Pending Requests I.D. Codes that have been issued to the SCI Bus. The SCI Bus then issues a data request from the remote units, and the information contained in the Data Request Pending Registers is passed to the Data Request Issued Registers, and the data pending register on SCI Bus only is then cleared. Data from the appropriate Remote and I/O Card is passed back to the SCI Bus Card, and the I.D. Code in the Data Request Issued Register is transferred to the Data Received Registers. The data request register is then voided.

On a normal arbitration cycle the interleaver and not the CCI/F Sequencer accesses the SCI Bus and reads the data from a remote. If there is any I.D. Codes in the Data received register on the SCI Bus the Data received Registers are then cleared. The I.D. Code read from the SCI Bus is compared with I.D. Codes contained in the Pending Request register on the interleaver, if it matches any of these the data is downlinked, if it dose not match it doesn't. The comparison is made at this time to see if both the interleaver and either the Sequencer or the Transponder has requested data from the same place, if so both modules receive the data.

As always during this arbitration cycle all data received form SCI Bus, both I.D. Codes and Raw Data from remotes is written to the CCI/F sequencer card. The I.D. Code read from the SCI Bus is compared with I.D. Codes contained in the Pending Request register on the CCI/F sequencer, if it matches any of these the data is written to the appropriate I/O Card, if it dose not match it doesn't. Once transferred the I.D. Code on the CCI/F sequencer is cleared.

MASS MEMORY STORAGE

In addition to the local CPU memory the uDACS supports a 320K x 22 MASS Memory Board with EDAC used to provide mass storage internal to each uDACS housing. Memory types supported on this card are RAM, EEPROM, EPROM, or PROM. The error detection and correction uses 6 check bits (Hamming Code) so that a total of 22 bits are required for the memory width. The error checking and correction may optionally be turned off so that diagnostics may be run to verify correctness of the memory. Two signals are provided from the error correction circuitry. One signal indicates that the word being read contains a single bit error. The other signal indicates that the word being read contains a double bit error. Up to 16 Mbytes of Mass Memory can be contained in a single enclosure.

DISTRIBUTED SYSTEM

The uDACS system is readily configured for use in a assiduously distributed system. The master unit contains the Bus Master Controller Card, while the remote units the Bus Remote Card. The Bus Remote units can be operated with or without a CPU Card, allowing for distributed processing and preprocessing of data before transfer to the master unit.

The Bus Master Controller (BMC) card transmits commands on the Serial Communications Interface Bus (SCIbus) to Remote Units (RU) and receives their responses. Either a Sequencer or a CPU of the uDACS unit containing the BMC directs the operation of the BMC, loading commands for transmission and reprieving replies. Alternatively, the central computer, if present, could run the BMC via CCI/F.

The SCIbus actually consists of two sets of shielded twisted wire pairs, one for commands and one for replies. Both commands and replies are Manchester bi-phase encoded and are transmitted at a 4.096M bps rate. Each command is composed of a sync pattern, mode and function control bits, an RU address, data and parity. The command bus is active continuously. Dummy commands are sent whenever real commands are not required to maintain clock synchronization between units. The reply bits are only active when an addressed RU responds. An addressed RU must always respond to a valid command with either an acknowledgment or data. The RU must never reply to a command having the wrong address, improper sync, invalid Manchester encoding, or incorrect parity. The reply is three bit times times shorter than the command to allow for SCIbus and RU delays. The interface to the host uDACS consists of 16 data lines, 20 address lines, and 4 control lines. The uDACS CPU writes to a specific address to write data, reset interrupt, or reset the BMC. The CPU reads from other addresses to read reply data or read status.

To send a command or information request over the SCIbus, the CPU writes two 16-bit words containing the unit address and data, most significant bits first. The command is automatically sent as soon as the second word is transferred. When the BMC receives a reply, it generates an interrupt. The CPU then reads the data. If an error occurs, the BMC sets the appropriate bits in a status register and generates an interrupt. Errors detected by the BMC include no reply, reply parity error, and invalid reply.

The SCI Bus Distributed Concept, supports both ARQ (Automatic Repeat Transmission) and FEC (Foward Acting Error Correction), error detection and correction.

Redundant SCIbus capability is provided. There is a second pair of command and reply buses that can be used should a failure occur in the primary pair. Redundant bus use is command selectable by the CPU, and can be controlled from the command input from the transponder.

The Bus Remote Interface Card provides each unit that is remote to the Central Control unit access to the serial data bus. It contains redundant receiver and transmitter stages, control and timing circuitry, buffers, and direct memory - I/O interfacing circuitry to each units internal bus. The control and timing circuits perform synchronization, bit-shifting, unit address decoding word verification, parallel buffering/transfers and monitors process transactions. Once an incoming word has been decoded as addressed for, that unit, parity is tested/stripped, function is determined, and the word is passed to the unit via the DMA-I/O circuits. A response will occur from the unit within the specified time interval, being transferred into the Bus interface card for transmittal to the central unit. If a response is not received in time, the response on the bus will be a “dummy” word.

Buffers are used to store data/address information as it is built and routed to the appropriate control circuits and interfaces. They allow the current word to be processed while a new input is being received. In addition, buffers are utilized for all serial-to-parallel and parallel-to-serial transactions and other data shifting functions.

POWER MANAGEMENT

Three modes of power management are supported: Full Operating, Standby, and Power Strobed. The full operating mode of operation is in effect whenever the card is performing the function it was designed for. The Power budget for any uDACS card in this mode of operation is 1 Watt maximum. The stanby mode of operation is in effect whenever the card is not being accessed by a bus master, receiving or transmitting data, or performing work such as an A/D conversion on an analog card. Maximum power in this application is 100 milliwatts. All I/O cards contain the following provisions for accomplishing this: Strobing the Clock OFF whenever the card is in Standby, where possible shorting inputs to analog

parts, such as operational amplifiers and powering off unused drivers and receivers. Power strobing consists of turning power off to all components on the card with the exception of the address decode.

DATA ACQUISITION CAPABILITY

The uDACS provides for the acquisition of analog, discrete, and serial digital interface signals. The analog subsystem consists of an analog multiplexer, signal conditioner, analog to digital converter, and digital signal Processor card. Discrete signals are handled by the Discrete I/O Card, while serial data is handled by the Serial Digital I/O Card. Additionally, the uDACS can be configured receive data from any of the standard shuttle, satellite, or spacecraft interfaces. All digital input cards have the capability of full verification of the receivers functionality.

The uDACS has the capability of formatting and outputting either non-encrypted data or encrypted data in a redundant telemetry stream. Telemetry formats are resident in on-card PROM, RAM, or EEPROM. Since the TLM Card contains its own sequencer, it can operate without a CPU in the uDACS unit. This configuration is ideal for simple data handling scenarios. Formats can be loaded from an external source or loaded from the CPU if used. The bit Rates are software programmable and command selectable.

Command Functions are uplinked from either ground stations or from satellites (such as TDRSS) through either single or redundant inputs. Several protocols are supported. The uDACS provides for software programmable command word size, bit rate, and field positions within the word. Command verification/validation processes are performed under software control. The uDACS supports a multitude of command outputs: Discrete Output, PO-28 Output, Analog Output, and Serial Digital Outputs. All Command outputs have independent feedback circuits for command verification.

ANALOG SIGNAL PROCESSING

With the understanding that some Sensors need special signal conditioning, the Analog Signal Processing Card provides the basic interface to Temperature Sensors, Force Sensors, Pressure Sensors, Flow Sensors, and Level Sensors. The design consists of the following sections; Anti-Alias Filter, Input Multiplexer, First Gain Stage - software selectable of 1 or 10, Auto-Error Voltage Nulling, Programmable Offset Voltages, Common Mode Voltage Sense/Guard Ring Drive, Second Stage Gain - Programmable under software software control (any one of 4 values between 1 and 50), Track and Hold Circuit, and Programmable Settling Time. A Digital Signal Processor is located on this module for Finite Impulse Response Filtering, Infinite Impulse Response Filtering, Fast Fourier Transforms etc.

FMDM INTERFACE

The MDM Interface provides the slave side of the Flexible Multiplexer Demultiplexer as defined In JSC Vol. 14. Information transmission takes place in 20-bit words, one microsecond per bit, Manchester 11 Bi-Phase format. Each 20-bit, word consists of a 3-bit sync time, 16 data bits, and one parity bit. Data and sync information is transmitted using pulse code modulation (PCM) in Manchester 11 bi-phase level coding. A logic “1” is a bipolar coded digital consisting of a logical one followed by logical zero. The clock is generated by the transmitting device and used in the fabrication of the Manchester 11 code format. When receiving data, the clock is derived from the Manchester 11 code as acquired.

PO-28

Shaped 28 Volt pulsed outputs for up to 96 inductive loads is provided by the PO-28 Card. The card additionally provides voltage threshold sensing circuits for verification of proper operation. If the driver circuitry is not populated, the card can be used for a high voltage discrete input card. Pulse width is adjustable under software control, while rise and fall times are presetable and load independent.

DISCRETE I/O

The Discrete Input/Output card provides 80 discrete input/output signals that can be used to control and/or monitor external apparatus. Numerous combinations of inputs and outputs can be configured, in groups of sixteen including input-only operation. It also provides the capability to verify the status lines configured as outputs, utilizing the unused input section of each output. Separate return lines are provided for each group of sixteen inputs/outputs. Selectable voltage thresholding is provided.

SDIO I/F

The Serial Digital I/O card provides a medium by which a serial message or command which is in parallel form, i.e. in CPU memory, is stored in one contiguous block of storage, converted to serial form, and output through one of eight addressable channels. Further, it provides for loopback confirmation of the transmitted serial stream for bit by bit comparison with the desired format used for error detection and correction.

TELEMETRY INTERLEAVER

The Telemetry Interleaver Card (TLM) has the ability to attain and interleave data from either I/O sources or memory according to a PROM format. The TLM Card can operate

with or without a uDACS CPU/Memory card in the box. Upon power-up the TLM initializes itself prior to inaugurating an operating format and bit rate. The formats are labeled A, B, C, D and test. The bit rates are software programmable up to 1 Mbit. Once initialized, the TLM then proceeds to perform the appropriate addressing, collecting, and interleaving PCM data. The interleaved PCM data is output as Manchester 11 B-Phase, NRZL and BIO-L. Other outputs of the interleaver are PCM clock, super-comsync, main frame and data cycle sync.

SGLS/IRIG

The interface to the Space Ground Link Support (SGLS) and the Inter-Range Instrumentation Group (IRIG) timing signal is provided. The circuitry contained on this card is used to receive and decode an IRIG timing signal, and receive uplink commands through the SGLS.

COMPLEX POLE FILTER CARD

The Analog Signal Conditioning Module Contains only a single pole filter. In some applications it may be necessary to filter with multiple pole anti-alias filter or a complex filter. A separate Complex Filter Card will be needed. This card is configurable as a six pole low-pass filter. In addition the filter can be configured as a Butterworth, Bessel, or Chebyshev. High Pass filters of the pole type and of the elliptical type are supported, as well as a multiple feedback bandpass, or as an elliptical bandpass filter, and as a band reject filter.

PRECISION CURRENT CARD

The current excitation card provides multiplexed, strobe, transducer excitation sources for use with the 4-wire RTD temperature sensors. Between 1 and 10 milliamps of current is multiplexed to 1 of 64 outputs. The actual current is set by writing to a 12 Bit DAC on the card, allowing the card to be set to its correct output current under software control. The card is memory mapped to the same location as the corresponding Analog Signal Processing Card. The duration of the output pulse is the same as the settling time programmed on the Analog Signal Processor.

SPACECRAFT RECORDER INTERFACE.

The Spacecraft Recorder Interface Card (SRIC) controls, and transmits data to/from the following recorders: Lockheed 4200, Lockheed 4250, Datatape M-14F, and the Oedetics.

I/V CONVERTER CARD

An interface is be provided that transforms low level currents to a precision voltage. This transresistance amplifier card contains 64 “zero” impedance inputs. After conversion to a precision voltage, the selected channel is multiplexed to an output pin that intern feeds one of the inputs on the Analog Signal Conditioning Module.

SYNCHRO AND RESOLVER I/F CARD

The uDACS is designed to allow for various interfaces to synchros and resolvers allowing for shaft angle measurements and positions. Some of the possible Synchros that can be supported are: Electromagnetic, Hairspring, Magslips, Transolvers, Slap, Linear Inductosyn, Rotary Inductosyn, and Multipole.

MiL-STD-1553 CARD

This circuitry provides an interface between the uDACS CPU and a MIL-STD-1553 data bus. The system performs the complete dual redundant Remote Terminal (RT) and the Bus Control (BC) functions of the MIL-STD-1653 Data Bus. The card contains a dual bus redundant, error detection circuitry, on-board RAM of at 1024 words. The RAM allows for the uDACS CPU to read or write data asynchronously with 1553B bus operations. An interrupt is used to signal the CPU upon reception of data or of errors.

STAR TRACKER I/F

The uDACS is capable of interfacing to the NASA Standard Star Tracker. This device is an electro-optical apparatus which uses an image polarizer to search for and track either stars or sunlit targets. This data is used primarily for spacecraft attitude control or spacecraft celestial pointing.

INTERNAL REFERENCE ASSEMBLY I/F

This card decodes pulse width modulated signals from an IRA, an produce a 16-Bit word, that represents a rate change of +/- 3.0 Degrees/Second with a resolution of 0.005 arcseconds/bit. The card receives the following inputs: Four Channels of 1200 Hz Pulse Width Modulated Data, Two Clocks for PWM decoding (From The Gyros), Two System Clocks. This circuitry outputs: Four 16-Bit data words representing the accumulated count and One 16-Bit Status Word representing the sign of each accumulated count and the number of PWM pulses decoded in each frame.

CLOCK DISTRIBUTION

The reception and distribution of precision clock sources from either “off card” or “on card” oscillators is made with this assembly. If the redundant clock sources are generated off card they are received with differential line receivers, which are in turn routed to the frequency checking circuits and the selecting multiplexer inputs. The differential output drivers are series terminated differential transmitters. The Master and Distribution Clock Card both provide pass/fall frequency check for the clocks. This information provides the CPU with error detection on the master crystal oscillator and the divider counter chain. The Distribution Clock Card uses the pass/fall checking on both clocks. The status of these test are input to the control logic to provide control of the selection of input clocks to the counter chain. The Master Clock Card control logic provides the clock status information to the CPU and produces an interrupt to the CPU upon clock failure. The Distribution Clock Card control logic takes the status on the four clock inputs along with the control signal from the CPU and uses them to control the input multiplexer. The CPU provides the control logic with a hardware swap inhibit and a software swap signal. The hardware inhibit signal prevents the hardware from swapping input clock channels automatically upon a clock failure. The software swap signal allows the CPU to swap input clock channels without having a clock error occur.

FSK INTERFACE

This card allows for Frequency Shift Keying decoding. The phase lock loop center frequency is set on the card by an R/C network. The system bandwidth, along with the loop filter time constant and damping factor is adjustable. The card contains a single pole post detection filter for the FSK data output. The card contains a lock-detect circuit for carrier detection.

HIGH SPEED HARDWARE VIDEO PREPROCESSOR

The uDACS is capable of supporting Video Data Processing. The technology provides interfaces to Video Cameras, invalid Pixel Elimination, Camera Gain Control, Offset Subtraction, Thresholding, Correlation Tracking, Data Buffering, and Data Compression etc.

RATE GYRO ASSEMBLY INTERFACE

The Rate Gyro Assembly assembly is a vehicle attitude change sensor that provides data for use in determining vehicle angular rate and attitude. Each RGA consists of a Rate Sensor Unit, an Electronics Control Unit and two Rate Integrating Gyros. Each RGA channel outputs a 1200 Hz PWM data signal and a 302.7 kHz clock signal. The 1200 Hz

PWM signal represents positive and negative incremental angle changes about the gyro axes. The PWM signal certain amount of logical “1” and logical “0’ time. The ratio of the high time to low to low time is proportional to the net rotation of the vehicle body about that gyro axes.

ENCRYPTED DATA

The uDACS has the capability of receiving and transmitting encrypted data. The encrypted data circuitry is housed in a “isolated” module of the same dimensions as the power supply. This module provides isolation allowing for Red and Black environs of the uDACS.

ADDITIONAL I/O CARD INTERFACES

The modular Architecture designed can support virtually any type of I/O function needed. Interface to the Remote Acquisition Interface to Spacelab can easily be implemented, as well as interfacing to Low G Accelerometers and Sun Sensors etc.

I/O CARD BUILT-IN-TEST

All command or data output cards either serial or discrete have verification circuitry located at the output stage of the card, while all command or data input Cards either discrete or serial have the capability of writing data to the card input stage and reading it back. The verification circuitry is able to access a preset word. If a failure is flagged this attribute allows the CPU to determine if the failure materialized on the verification circuitry or on the absolute functional circuitry.

ENVIRONMENTAL

The system is designed to function during all phases, and conditions typically encountered during Space Borne and Launch Vehicle missions. All digital control circuitry as well as the power supply will withstand the harsh radiation environments illustrated in Table 1.

Table 1
Radiation Environments

Total Dose:	1E06 Rads Si, 1E14 Neutrons/Sq Cm Functional After Exposure
SEU:	1E-10 Bit errors/Day, Latchup-Free
Transient:	1E10 Rads/Sec Functional, 1E12 Rads/Sec Survival

The system operates over a temperature range from -175 Degrees C to + 70 Degrees C in a vacuum of 1E-8 Torr. With the use of thermofoil electric heaters (below -55 Degrees C.) the system can “cold” start at -175 Degrees C. All pertinent specifications of MIL-STD-461 are met.

CONCLUSIONS

The Technology developed in the uDACS system provides high reliable, small, power efficient, light weight, radiation hardened, stand alone Flight Computers as well as Control, and Command/Data Handling Systems. The bus arbitration technique provides respectable processing throughput for most Real Time Control Systems. Since the system can withstand all single point failures and most multiple failures and provides built-in-test capability of all I/O cards (with switchover to a back-up card) Fault Tolerance and Fault Recovery are actually realizable. Combining these characteristics with the distributed processing capability of the system, a general purpose network with applications in virtually all Space Borne and Launch Vehicle assemblies is achieved.