

APPLICATION FOR SPACECRAFT OF THE 90's USING MICRODACS TECHNOLOGY

Paul Horn
Systems Engineer
SCI Technology Inc.
Box 1000
Huntsville, Al. 35802
(202) 882-4534

ABSTRACT

Recent developments in electronics have made possible the miniaturization of many of the subsystem components associated with a typical spacecraft data acquisition and control system. This paper describes a low power consumption, fault tolerant, high performance data acquisition and control system design utilizing third generation hardware. The system includes built in test autonomy, redundancy management and fault tolerant communication busses, and supports multiprocessing with up to five 35 Million instructions per second (Mips) processors.

GENERAL

A recognized need for hardware having radiation survivability, fault tolerance and autonomous reconfigurability is growing within the space community. The spacecraft data acquisition system of the 90s must encompass all of the above features, as well as being light weight, low volume and must require low operating power. It must be flexible to allow for various application specific configurations, and must have enough processor (CPU) cycles to perform reasonably computationally intensive tasks. The system described in the following paragraphs is built around the SCI microDACS (micro Data Acquisition and Control System) and embodies all of the desired attributes listed above.

SYSTEM EXAMPLE

The central unit of the system example (figure 1) provides commands to, and gathers telemetry data from, the remote units, and consists of a redundancy manager board, two processor boards, two bus control boards, two power supplies, two sets of discrete input cards, and two data interleaver cards with a split bus arrangement as shown in figure 2.

The redundancy manager uses “watch-dog” timers and majority voted control lines to provide system switch-over in the event of a failure in one half of the central unit. If some data loss can be tolerated, the system can be configured such that the stand-by half of the system is unpowered. As shown in figure 2, both system half’s are powered, with the redundant half running in the “shadow” mode until called upon by the redundancy manager. The master unit contains input ports which allow for time code inputs and uplinked command and data inputs.

Remote units are used to gather the telemetry data and to distribute commands and control to various remote sites within the spacecraft. The remote units shown in the example of figure 3 contain a power supply, analog input cards, discrete input cards, a CPU card, and bus interface cards. The analog input cards accept up to 80 single ended input channels (or 40 differential inputs), and convert each of the inputs to a 10 bit binary number, with a maximum non-accuracy of 1 least significant bit. The data input from the analog and discrete cards is passed to the CPU card for data compression and pre-processing, buffered, sent to the bus interface, and output to the serial bus.

Telemetry data can be passed to the interleaver via DNA transfers to the interleaver RAM, or can be supplied directly from I/O sources. Output data rates of up to 1 megabit per second are supported by the interleaver.

RADIATION TOLERANCE

Semiconductor devices exposed to ionizing radiation are subject to damage caused by trapped charges at bulk semiconductor interfaces and in the gate oxide. These trapped charges result from the generation of additional carriers in the oxide layer by the high energy particles, and cause shifts in the threshold voltage of MOS devices when the trapped charge occurs in the gate oxide layer. Assuming 100% oxide layer charge entrapment, the threshold voltage shift can be determined as follows (1):

$$\Delta V_T = \frac{qg_0 t_{ox}^2 \gamma}{2\epsilon}$$

Where ΔV_T is the threshold voltage shift

γ is the total absorbed dose

$g_0 = 7.6 \times 10^{12}$ h-e pairs/cm rads(Si)

q = electron charge

ϵ = dielectric constant

t_{ox} = gate oxide thickness

As can be seen from the preceding equation, radiation tolerance can be increased (ie., the threshold voltage shift can be minimized) if the oxide thickness is decreased. The

microDACs unit makes extensive use of thin oxide layer CMOS and is designed to withstand a total rad (radiation absorbed dose) of $1\text{E}06(\text{Si})$. Further, a built-in error correcting scheme employed by the microDACs on both the address and data lines ensures a low system error rate due to Single-Particle-Induced Transient Upset.

FAULT TOLERANCE

Commands and data are sent between the central unit and the remote units via a redundant serial bus. The commands may be transmitted on either the “A” or “B” command bus, and reply’s returned on either the “A” or “B” reply bus. Figure 1 shows a typical system implementation using redundant data busses for increased reliability.

System data and address lines incorporate a modified Hamming-code error detection and correction scheme. All of the system control lines are triple-redundant. The error detection and triple-redundancy ensure proper system operation in environments containing high energy particles (ie., cosmic rays). In systems requiring the highest reliability and fault tolerance, the system bus may be configured as a split, redundant bus with duplicate system resources on each isolated half. A redundancy manager using watch-dog timers monitors the system and controls system switch-over.

The serial bus uses a unique technique of driving the bus in both the voltage and the current mode. The transmitters and receivers are directional and are thus impervious to reflections and disturbances on the bus downstream of the unit. Even bus shorts and opens do not disturb the operation of units upstream of the fault. The directional nature of the bus allows redundant units to transmit transparently into the bus of the primary unit, allowing flexibility in cross-strapping for redundant operations. This feature, along with the redundant bus architecture, provides system tolerance to single, and in many cases multiple, failures.

FLEXIBILITY

The overall system shown in the example embodies flexibility due to the mother-board/daughter-board configuration used in the central and remote unit physical packaging. Many different card compliments and configurations may be used depending upon the requirements of the end product: As many as 27 remote units may be used on the serial busses for very large system configurations. Additional flexibility results from the light weight (under 9 lbs., central unit; under 7 lbs., remote unit), and low volume of the modern components, allowing full hardware redundancy in less weight and volume than was often required with previous generation hardware.

The central unit supports a number of different configurations, ranging from a sequencer based system with no processor, to high speed, multi-processor systems containing up to five 35 Mips processors with a system throughput (using the 80% rule) in excess of 117 Mips. Up to 16 MByte of memory can be supported by the central unit, providing sufficient memory for full autonomous systems, artificial intelligence, or other memory intensive applications.

Various I/O cards can be used in the remote units depending upon the number of signals and type of conditioning required by the spacecraft system. A CPU in the remote unit is optional and may be present if required for data preprocessing or remote autonomous operations

SUMMARY AND CONCLUSIONS

The new generation data acquisition and control systems are flexible and powerful, and can be configured to match any system configuration required. Full hardware redundancy is now possible with less weight and power consumption than could be obtained with previous generation hardware in a non-redundant system. The extensive use of CMOS ensures low system power consumption and provides hardening for ionizing radiation environments. Error detection and correction provides protection against Single-Particle-Induced Transient Upsets, an important feature when the system is exposed to high energy particles and data and control errors cannot be tolerated.

REFERENCES

1. Sander, H. H. and Gregory, B. L., 1975, "Unified Model of Damage Annealing In CMOS, from Freeze-in to Transient Annealing", IEEE Trans. Nucl. Sci., Vol. NS-22, No. 6, pp. 2157-2162, December 1975.

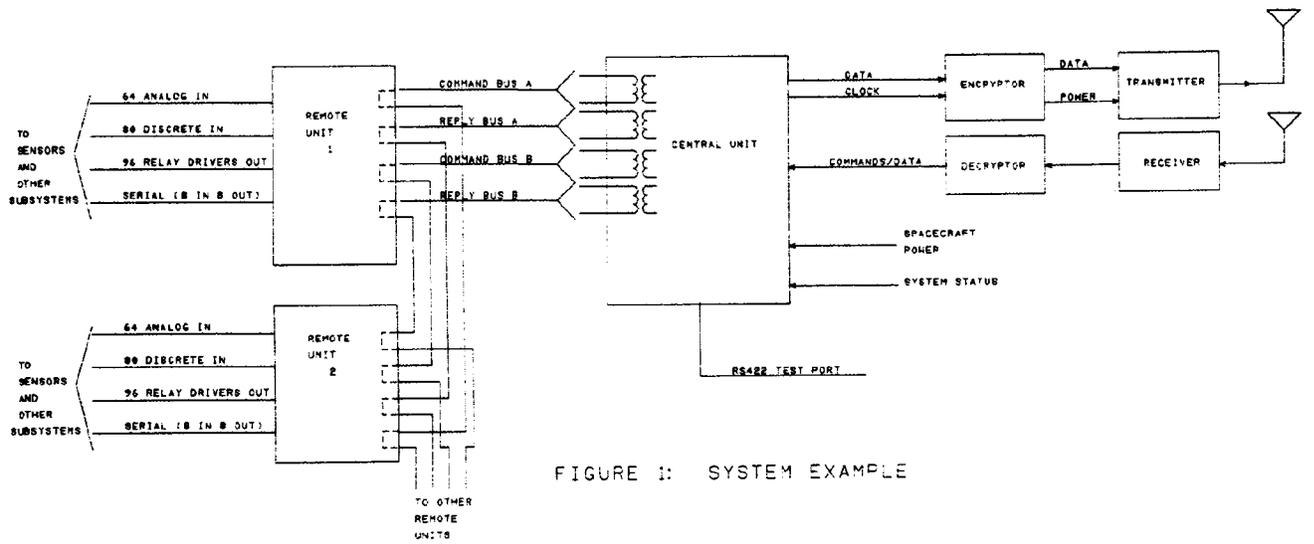


FIGURE 1: SYSTEM EXAMPLE

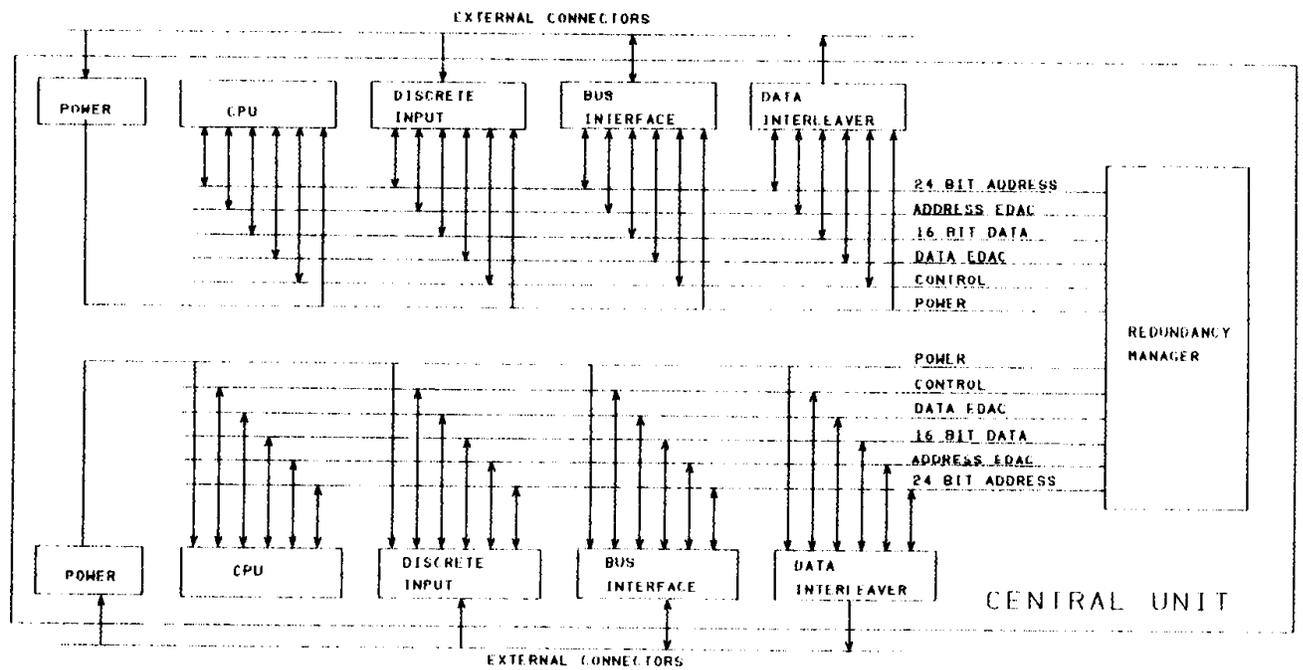


FIGURE 2: CENTRAL UNIT

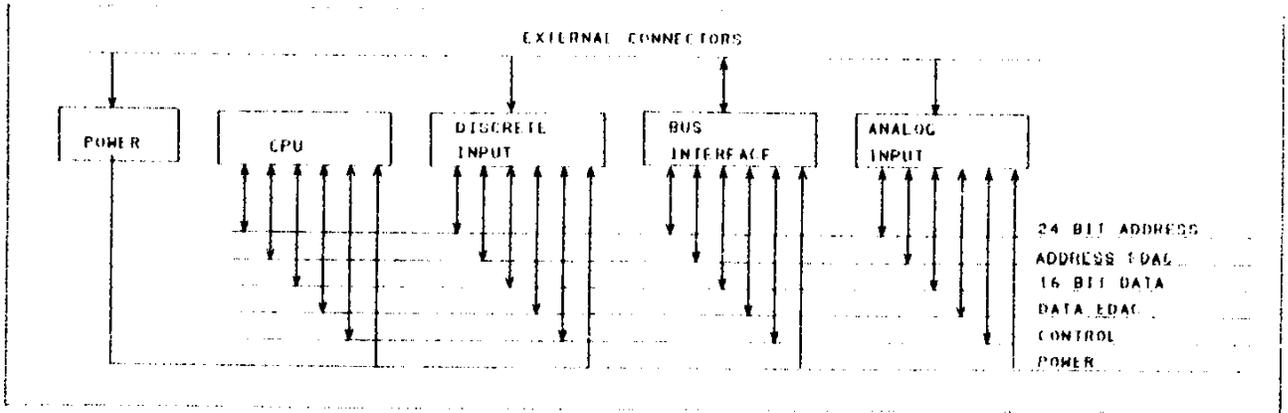


FIGURE 3: REMOTE UNIT