A DIGITAL VIDEO LINK FOR TELEMETRY APPLICATIONS*

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ABSTRACT

Using a simple, yet flexible, pixel compressor and a frame buffer, a compact digital video link has been built which allows a trade-off between bit rate, spatial resolution, and frame rate.

INTRODUCTION

Video cameras can be a useful part of a telemetry system that is required to gather motion analysis or reconnaissance data. Video can be transmitted in two forms: analog or digital. The disadvantage of analog video is that it is not easily encrypted and is susceptible to noise and distortion. Digital video allows the use of standard encryption and error correcting codes. However, digital video is not widely used in telemetry systems because it usually requires either a high bit rate or complex data compression circuitry. This paper describes a simple digital video encoder/decoder suitable for airborne telemetry. Some of the system design considerations include:

1. Low volume and power.
2. Compatibility with range receiving and recording capabilities.
3. Flexibility, so the system can be adapted to a wide variety of scenarios.
4. Budget constraints which preclude the development of custom chips.
5. A specific mission requirement to multiplex several cameras to the encoder and have a test pattern generator for an end-to-end system ground check.

DATA FORMAT

Most test ranges can only receive and record up to about 1-10 Mbit/sec and digitizing video results in bit rates exceeding 40 Mbit/sec; consequently, the video bit rate must be reduced. The system to be discussed reduces the bit rate by using a pixel compressor to reduce the number of bits per pixel and a frame buffer to allow the reduction of the spatial

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resolution and frame rate. The system can be tailored to a specific application by selecting the appropriate digitizing format from Table 1.

Table 1: Image Digitizing Formats

Image Resolution	For Bit Rate =	7.16 Mbit/sec	3.58 Mbit/sec	1.79 Mbit/sec	0.89 Mbit/sec
320 H x 490 V x 6 bits/pixel:	Frame Rate =	7.5 frames/sec	—	—	—
320 H x 490 V x 3 bits/pixel:	Frame Rate =	15 f rames/sec	7.5 frames/sec	—	—
320 H x 245 V x 6 bits/pixel:	Frame Rate =	15 framestsec	7.5 frames/sec	3.75 frames/sec	—
320 H x 245 V x 3 bits/pixel:	Frame Rate =	30 frames/sec	15 frames/sec	7.5 frames/sec	3.75 frames/sec
160 H x 245 V x 6 bits/pixel:	Frame Rate =	30 f rames/sec	15 frarnes/sec	7.5 frames/sec	3.75 frames/sec

Data is transmitted NRZ-L with the frame format shown in Figure 1. A minor frame consists of 15 sync bits and 960 data bits. A horizontal line is contained in one or two minor frames depending on the horizontal resolution and number of bits per pixel. A major frame consists of 245, 490, or 980 minor frames, depending on the vertical resolution and the number of minor frames per line.

Major Frame Sync: 15 bits	Data: 1st 960 bits (160 6-bit or 320 3-bit pixels)
Major Frame Sync: 15 bits	Data: 2nd 960 bits (160 6-bit or 320 3-bit pixels)
Major Frame Sync: 15 bits	Data: 3rd 960 bits (160 6-bit or 320 3-bit pixels)

- o N = 245: 320H x 245V x 3bit/pix or 160H x 245V x 6bit/pix
- o N = 490: 320H x 245V x 6bit/pix or 320H x 490V x 3bit/pix
- o N = 980: 320H x 490V x 6bit/pix

Minor Frame Sync: 15 bits	Data: Nth 960 bits (160 6-bit or 320 3-bit pixels)

Figure 1: Digital Video Frame Format

This data format allows a simple, synchronous system architecture. A system using a fixed number of bits per pixel is much easier to implement (at the expense of lower compression ratios) than one using a variable bit per pixel algorithm like Huffman coding. The format sends one image every 1, 2, 4 or 8 NTSC (National Television Subcommittee) frames. Also, the A/D clock, output bit rate and frame rate are all integer sub-multiples of a 14.31818 Mhz system clock, which is also the basis of the NTSC standard [1]. This allows easy synchronization to and generation of NTSC signals.

DIGITAL VIDEO ENCODER

The digital video encoder is shown in Figure 2. The encoder has inputs for three video cameras. Camera 1 is the master, and the encoder is phase locked to it. This is done by feeding the sync from the master camera and the sync generated in the encoder to the PLL. The 14.31818 Mhz voltage controlled crystal oscillator in the PLL is the encoder system clock. The other cameras then lock on to the encoder. By changing two jumpers, the

encoder can serve as the master. The sync generator also provides addressing and control signals needed to reconstruct the test image stored in EPROM.

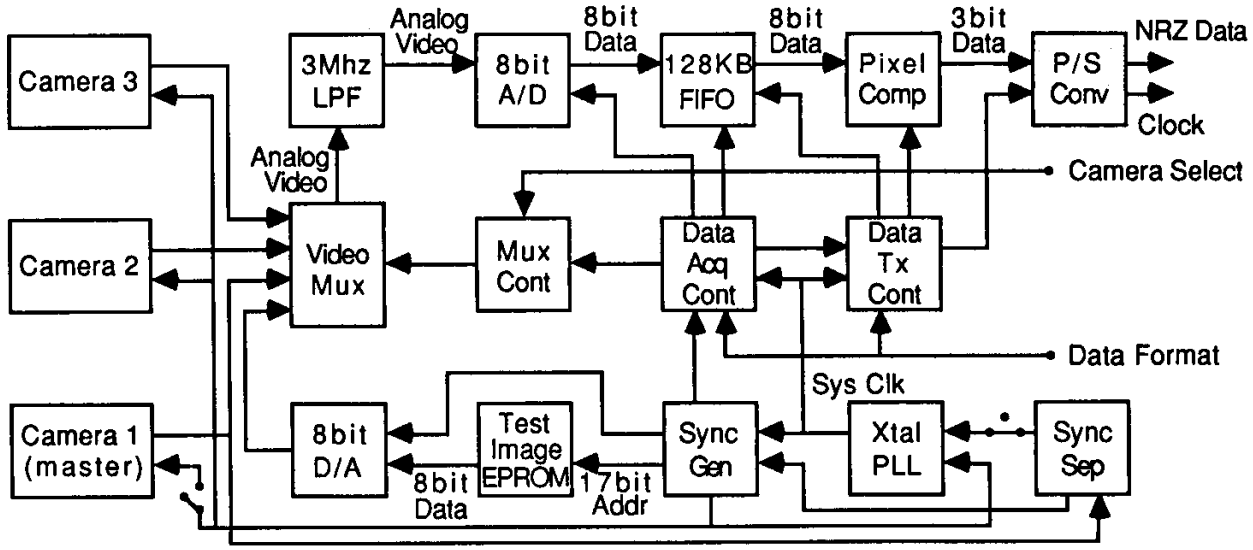

Figure 2: Simplified Digital Video Encoder Block Diagram

The test image and the three video inputs are DC-restored and fed to the video multiplexer. A state machine serves as the multiplexer controller. With no camera selected, the multiplexer is switched to the test image. When any one camera is selected, the multiplexer is switched to that camera. But when more than one camera is selected at a time, the selected cameras are time division multiplexed on a frame by frame basis. This allows near simultaneous digitization of up to three B/W cameras (or one RGB camera) by reducing the effective frame rate. The controller also superimposes the source ID on the first line of each frame so that the decoder will be able to sort the received frames.

The multiplexed video is passed through a 3 Mhz anti-aliasing filter and digitized by an 8 bit flash converter at 7.16 Mhz. The data format is determined by jumper settings and the algorithm that is programed into the pixel compressor. The data acquisition and data transmission controllers interpret the jumper settings and generate the appropriate control signals. The data acquisition controller uses information from the sync generator to determine which pixels digitized by the A/D will be saved in the FIFO. The data transmission controller and the FIFO are synchronized to the data acquisition controller. The data transmission controller recalls the data from the FIFO, passes it through the pixel compressor, and serializes it in the parallel-to-serial converter. The data transmission controller also generates and inserts sync words into the output bit stream.

The pixel compressor consists of a 64K x 16 bit EPROM and an 8 bit latch (as shown in Figure 3). Incoming data and the feedback data which has been delayed by one clock cycle

form the EPROM address. The output of the EPROM is the output data and feedback data for the next address. Many functions of the input data can be realized by programming the EPROM. For instance, the compressor can be programmed to implement an ALDPCM (adaptive log differential pulse code modulation) algorithm. It can just as easily be programmed with an algorithm to dither and truncate the input signal. In the 6 bit per pixel mode, the EPROM is programmed to compress an 8 bit pixel into a pair of 3 bit data words in two clock cycles. The compressor is initialized every minor frame by resetting the feedback data latch to minimize transmission error propagation.

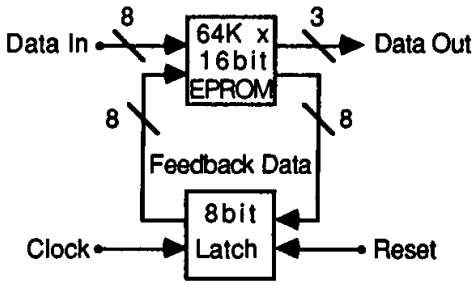

Figure 3: Pixel Compressor

The shaded blocks of the encoder in Figure 2 are implemented with two Altera EP-1800 EPLDs (erasable programmable logic device). The encoder and its power conditioning circuitry are built on four 3" x 5" PWBs (printed wiring boards) and consume less than 7 Watts.

DIGITAL VIDEO DECODER

Figure 4 shows the digital video decoder. Data enters the correlator, which looks for possible sync words. These possible sync words are passed to the synchronizing filter for interpretation. In search mode, the filter looks for sync words occurring at 975 bit intervals. When several consecutive sync words are found with the correct spacing, the filter considers itself locked to the data. When locked, the filter ignores spurious sync words yet recognizes valid sync words with single bit errors and bit slips. The filter outputs a sync pulse every time it expects a sync word. If the filter misses several sync words in a row, it drops out of lock and enters the search mode. The decoder uses the sync pulses to synchronize itself to the incoming data. The correlator also performs a serial-to-parallel conversion, and passes the resulting 15 bit data words to the multiplexer where it is parsed into 3 bit words. The data is then passed through the pixel expander, which is the same as the pixel compressor except that the EPROM is programmed with the inverse algorithm. The data receiver controller directs data flow from the correlator to the FIFO and determines the source of each frame of data. The data display controller sends each frame of data from the FIFO to the proper frame memory. Each D/A continuously reconstructs video from the contents of its frame memory. The data transfer from the FIFO

to the frame memory is done in a way that allows the same frame to be shown repeatedly until an entire new frame is ready to be displayed. The sync generator provides all the D/A control signals and frame memory addressing. The 14.31818 Mhz system clock is generated by a PLL locked to a multiple of the incoming bit rate.

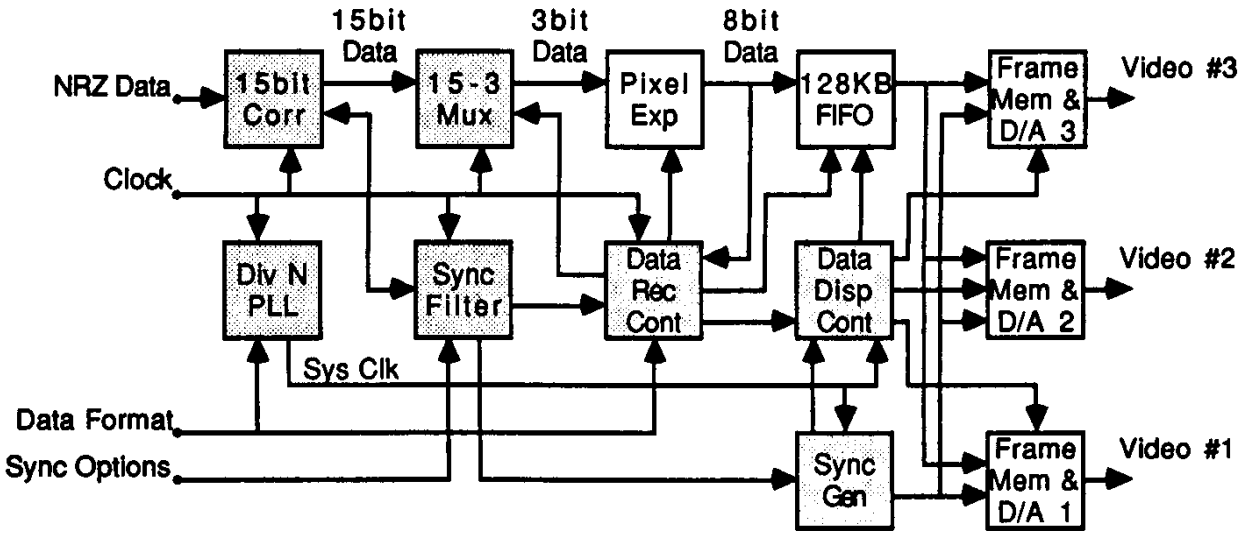

Figure 4: Simplified Digital Video Decoder Block Diagram

The shaded blocks of Figure 4 are implemented with six Altera EP-900 EPLDs. The decoder is built on six 3" x 5" PWBs and uses less than 20 Watts. If only a single video output is required, two frame memory PWBs can be removed, and the total power required drops to 12 Watts.

SYSTEM PERFORMANCE

The image quality of the system using an ALDPCM algorithm is well matched to human observers; it exhibits no slope overload and has little noticeable overshoot. The dithering algorithm is suitable for human and machine observers and is insensitive to transmission errors. Other algorithms [2][3] can be programmed into the pixel compressor. Transmission error tolerance has yet to be characterized for this system.

CONCLUSION

A digital video encoder/decoder has been built which is suitable for airborne telemetry. The system allows the use of multiple B/W or a single RGB camera. The spatial resolution, frame rate and pixel compression can be tailored to specific mission requirements. The output bit rate of the encoder can be varied from 0.89 to 7.16 Mbit/sec, depending on test range capability and RF data link considerations. The output of the encoder can be coded for increased transmission error tolerance or encrypted for data

security. The system architecture is flexible, yet very simple, leading to a compact design. Also, the entire system is implemented with off-the-shelf components, thus reducing development time and cost. The size of the encoder and decoder can easily be cut in half by using surface mount devices.

ACKNOWLEDGMENTS

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