

SIMPLE DIGITAL ENCODER FOR NTSC COMPOSITE VIDEO

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ABSTRACT

The need exists to encode NTSC composite video into a serial digital bit stream for encryption prior to transmission. Further, this need exists in places where power and volume are at a premium. This paper describes a simple solution using the Continuously Variable Slope Delta Modulation technique of encoding all lines and fields in real time and is usable with clock rates from 5 to 25 MHz. The circuits presented use only a 5-volt power supply and two active devices: a comparator and either a dual flip-flop or serial shift register.

INTRODUCTION

When designing telemetry systems for weapons carried under the wings of attack and fighter aircraft, the designer is instantly faced with several constraints:

1. Packaging - the telemetry system usually replaces the warhead and must maintain the same weight and center of gravity.
2. Power - the telemetry system has limited power available and usually operates from its own batteries during free flight.
3. Real Time - the closing velocity between the weapons and targets ranges from hundreds of feet per second to thousands of feet per second with critical data being generated as the weapon reaches the target. Since the weapon can be destroyed as it reaches the target, impact with the earth or the target itself, data cannot be stored but must be transmitted as it is generated.
4. Telemetry Receiving Stations - The maximum data rates are limited by existing telemetry receivers and there are no standards for telemetered video. The maximum data rate can be increased with new receivers, however, telemetered video requires the use of a special decoder box in the receiving station.

This paper addresses the encoding (digitizing) and decoding (restoration) of the original analog signal of an NTSC composite video signal. The designs presented satisfy the above constraints and show a simple nonstandard decoder for use at the receiving station. The driving force is to encode usable video at some minimum data rate--at the Naval Weapons Center 6 MHz. However, since receivers are available to support higher data rates, the response of these circuits at higher data rates is presented. Usable video is defined to be video that can be used for its intended purpose and not necessarily a perfect reproduction. It is assumed that the reader is somewhat familiar with Delta Modulation (Deltamod) and NTSC composite video signals.

EVOLUTION

The concepts of Deltamod are documented throughout the text books on communication theory. References 1 and 2 provide easy reading for those not familiar with Deltamod. Its use as a potential solution to the described video problem was suggested by Mr. Jim Reiger; Mr. Jack Huber designed the original flight test circuit in use at the Naval Weapons Center. It employed a single slope at a 6 MHz data rate, and has been averaging two flights per month since December 1987. The circuit of Figure 1 is representative of the original flight test circuit.

A cursory review of the literature on Deltamod gave little help on its use to encode video signals. Reported results were comparable to Huber's circuit with no mention of clock frequency. Reference 1 credits M. R. Winkler with inventing dual slope Deltamod in 1963. Reference 2 describes the use of Continuously Variable Slope Deltamod (CVSD) for digitizing voice. Combining the thoughts of References 1 and 2 led to the use of CVSD for encoding video signals.

SINGLE SLOPE DELTA MODULATION

A Deltamod Encoder is easily accomplished with a comparator, flip-flop, and an RC low pass filter and is shown in Figure 1. However, its interface with NTSC composite video requires a 75-ohm, termination, resistor R1, and that a DC component be added to the signal. Resistors R2 and R3 provide the DC component necessary to keep the input signal centered in the dynamic range of the comparator. Resistor R4 and capacitor C2 form the low pass filter.

The output of the flip-flop follows the state of the comparator at the time of the rising edge of the clock. The filter capacitor charges towards the output voltage of the flip-flop and is monitored by the inverting input of the comparator. As the voltage on the capacitor exceeds the noninverting input to the comparator, more positive if the output of the flip-flop is high--more negative if the output of the flip-flop is low, the comparator and the flip-

flop change states. The net result is an NRZ bit pattern at the output of the flip-flop, which when filtered, yields an output voltage approximately equal to the video input signal.

There is a compromise that must be considered with Deltamod. The slew rate of the RC filter must be slow enough to reproduce segments of the picture made up of near identical gray, such as pictures generated with low light levels, and fast enough to go from white on the right side of the picture to sync pulse. These tradeoffs are referred to as quantizing error (slew rate too fast) and slope overload (slew rate too slow), respectively.

The selection of the active components for use with video Deltamod is critical. The first criteria to be considered is a minim delay through the comparator and flip-flop. The second criteria is a flip-flop whose output will switch between the full range of ground and the power supply, namely 0 and 5 volts DC. The nominal delay of the components shown in Figure 1 is 15 nanoseconds with the Advanced CMOS flip-flop meeting the output switching requirements.

It is recommended that initial video Deltamod experiments be carried out using a single slope circuit, an RC time constant of 10 microseconds and a clock rate of 6 MHz. This will reproduce pictures with indeterminate (fuzzy) black to white and white to black vertical edges, good low light level performance, and reasonably good sync (except with bright white on the right side of the picture). Vary the clock rate, the filter slope, and the video intensity (camera lens opening). Finally, adjust the circuit to operate at 15 MHz. The picture will approach black and white camera quality with black/white vertical edges being slightly fuzzy.

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATION

It becomes obvious that if the flip-flop does not change states after two or three clock pulses then the filter output is not keeping up with the video input. Solution: use the bit pattern from the flip-flop to decrease the RC time constant. The result is a filter whose slew rate can be varied with each clock pulse or CVSD. The insert of Figure 1 shows a technique to modify the single-slope Deltamod circuit into a two or three slope CVSD circuit. Table 1 presents the switching logic. In the two-slope system, the RC time constant will be reduced when the flip-flop has the same state for the last two clock periods. The three-slope system reduces the RC time constant further when the flip-flop maintains the same state for three consecutive clock periods.

There is a problem using the two-slope CVSD at 6 to 8 MHz. Consider a DC voltage applied to the noninverting input to the comparator. There is only one DC level that will produce on a continuous string of alternating highs and lows, approximately 2.5 volts. Therefore, the bit pattern will have strings of consecutive highs and lows just to maintain

the DC level of the video input signal; consecutive highs and lows cause the circuits to go to the high slew rates. The result is smearing (loss of detail) when reproducing video that was originally generated during low light level conditions. In general, low light level performance is not as good as with the single slope system. This phenomena clears up at clock rates in the vicinity of 8 to 10 MHz. Some improvement was made with the three slope system, however, the right combination of slopes was not found to obtain low light level performance equal to the single slope system.

VARIABLE VOLTAGE SOURCE CVSD

There are two options for changing the charge rate of a capacitor:

1. Vary the RC time constant--technique used with previous circuit.
2. Vary the source voltage--technique used in the circuit to be presented.

Figure 2 presents two simple RC circuits with multiple voltage sources and resistors. The Thevenin equivalent circuit, as seen by the capacitor, is a single voltage source equal to the open circuit voltage and a single series resistor equal to the resistors in parallel. Tables II and III show that four or eight Thevenin equivalent voltages can be derived if the source voltages are set to all possible combinations of 0 or 5 volts, respectively.

Figure 3 presents the CVSD circuit used to evaluate both the two-source and three-source systems; the resistors shown are for the three-source system selected for optimal performance at 6 MHz. Resistor R6 is omitted for the two-source system.

The three-source system shown in Figure 3 alleviates the low light level smearing problem discussed earlier. Notice that the resistors associated with the mid and old bits are identical and three times the value of the resistor associated with the new bit. These resistor values lead to the Thevenin source voltages in Table IV. Apply a string of random highs or lows to the shift register and use the table to determine the equivalent source voltage. It is seen that small variations in the equivalent source voltage result from various combinations of one or two consecutive highs or lows. These small variations in source voltage greatly enhance picture quality at low light levels with respect to the two-source/slope systems. Three consecutive highs or lows will cause the maximum slew rate; this allows for satisfactory performance when going from white on the right side of the picture to the sync level.

Table V gives the Thevenin Source voltages for a two-source system with the resistor values set to a ratio of 3 to 1. The circuit performance is essentially equal to the two-slope system.

Below 10 MHz, the three-source circuit gives results equivalent to the single-slope circuit at low light levels and its performance nearly equals that of the two-source/slope circuits with respect to slope overload. The performance of the two-source system is equivalent to the two-slope system with poor performance at low light levels and clock frequencies below 8 MHz. Above 10 MHz, the two-source system yields noticeably better performance than the three-source system with respect to black/white edges.

The system setup is relatively easy:

1. Determine the maximum allowable clock rate. Conduct experiments to determine the system to be used: three-source system--below 9 MHz; two-source system--8 to 12 MHz; single-slope system above 10 MHz.
2. Use a camera with a manual lens. Set the iris to the minimum expected light level. Set the RC time constant of the filter to the minimum value (maximum slew rate) that will give acceptable low light level performance. In both the two-source and three-source systems, start with a 3 to 1 ratio in the resistors. Maintain these ratios as adjustments are made. Experiment. There may be better combinations for a specific application.

GROUND STATION DECODER

The ground station decoder for this system is simple. Leave out the comparator and its associated input circuitry and clock the NRZ code into the flip-flop or shift register. Filter the flip-flop/shift register output with a filter identical to the one in the encoder (note that the filter component tolerances are not critical). Monitor the filter capacitor voltage with a high input impedance buffer. The resultant voltage is a usable reproduction of the original video signal.

PERFORMANCE TO BE EXPECTED

The video reproduced with the three-slope system operating at 6 MHz will be found to be acceptable for many applications. Evaluate the reproduced video to be GOOD ENOUGH or NOT GOOD ENOUGH for its intended use and not against the original video. Black/white vertical edges will be fuzzy. This fuzziness is more noticeable in still pictures than in moving pictures. Video quality improves significantly as clock rate is increased and slew rates are set to be faster. Use of the two-source system above 8 MHz and the single-slope above 10 MHz produces very good video. Black and white camera quality video is approached at 15 MHz.

Although the new circuits described herein were developed in an attempt to reproduce video with a minimum data rate, there is a bonus when used with higher data rates. The single slope circuit can be used to encode color video using, clock rates above 15 MHz with color quality improving as the clock rate is increased. Use a color bar generator and adjust the slew rates and monitor for optimal color. The picture quality is surprisingly good.

REFERENCES

1. Fink, Donald and Christiansen, Donald, Electronics Engineers Handbook, McGraw-Hill, New York NY, Second Edition 1982, pp. 14-38 to 14-41.
2. D. Jones, Harris Analog Product Data Book, 1986, APP NOTE 607, Delta Modulation for Voice Transmission, pp. 10-226 to 10-230.

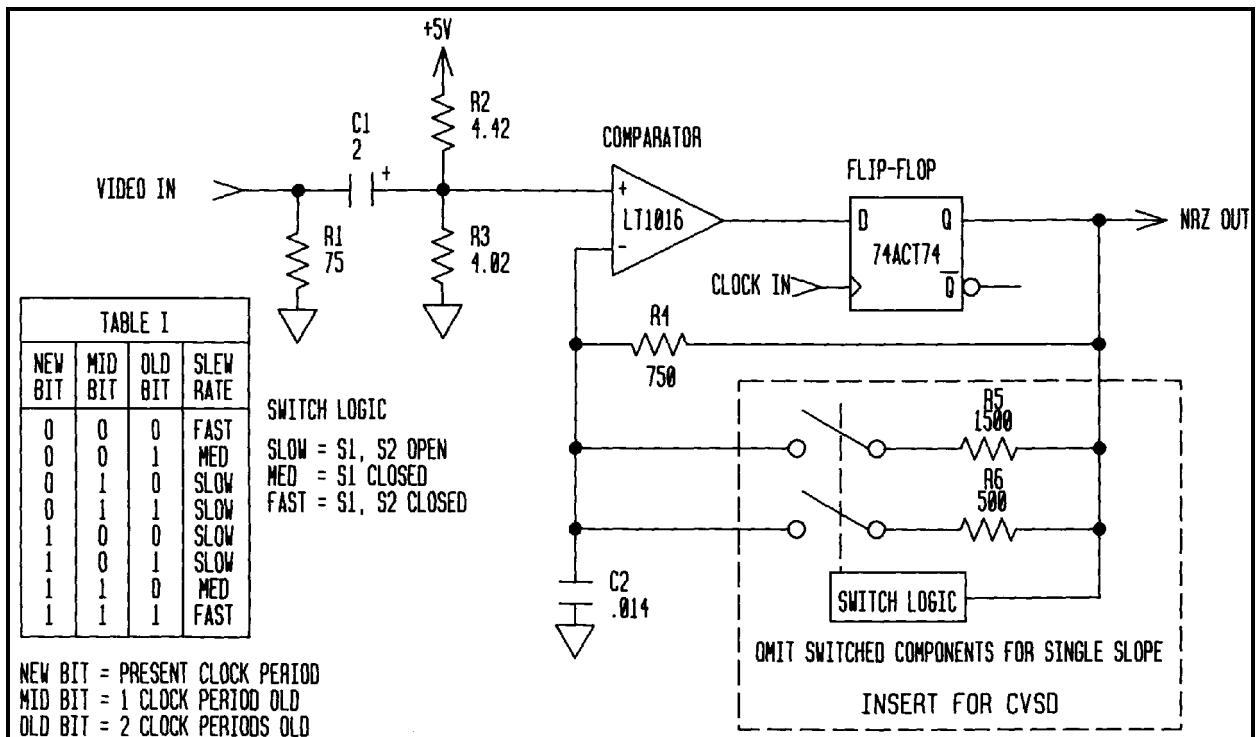


FIGURE 1: ONE, TWO OR THREE SLOPE VIDEO DELTA MODULATION

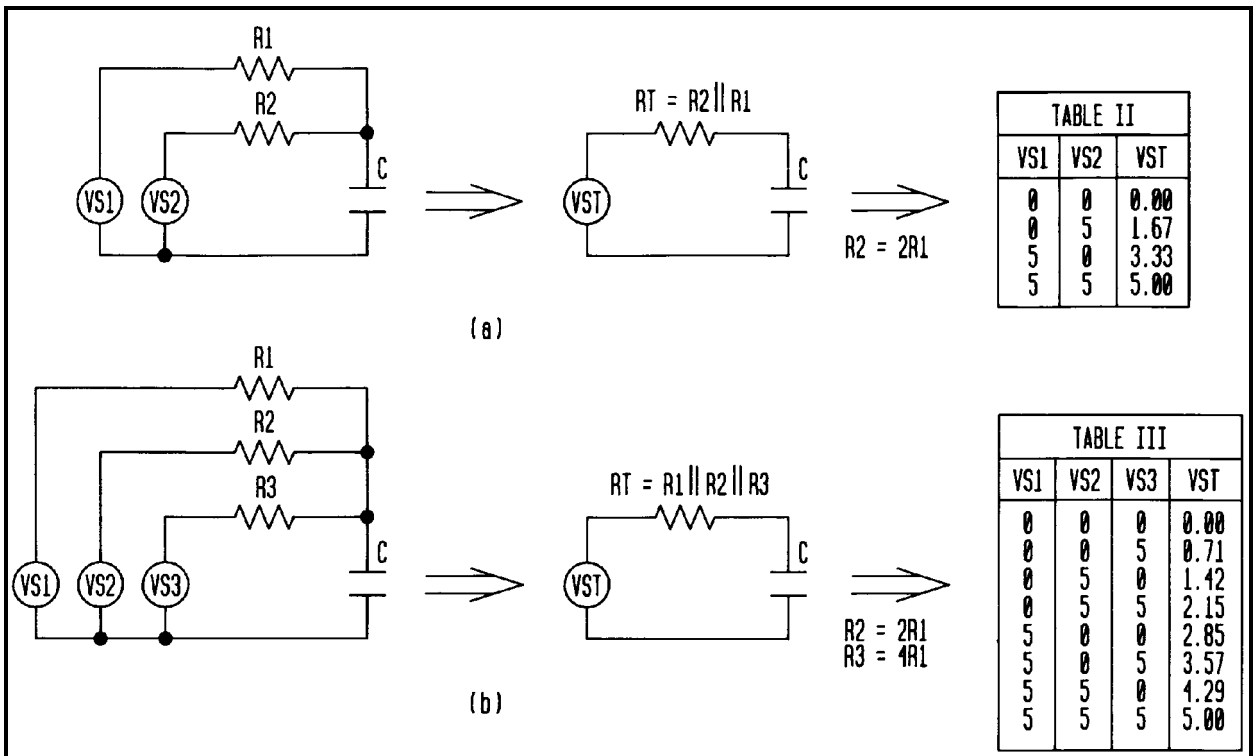


FIGURE 2: (a) TWO-SOURCE, THEVENIN EQUIVALENT CIRCUIT. (b) THREE-SOURCE THEVENIN EQUIVALENT CIRCUIT.

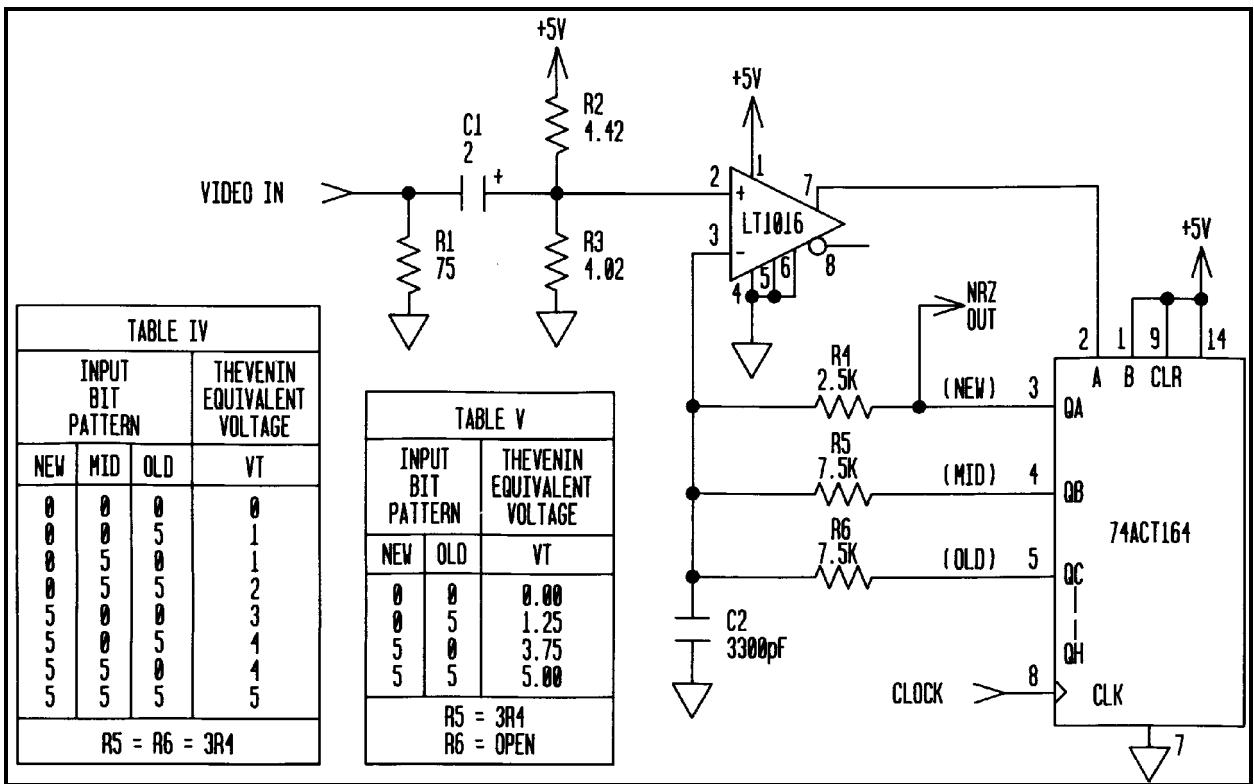


FIGURE 3: CVSD USING TWO OR THREE SOURCE VOLTAGES