MASS MEMORY RELIABILITY EVALUATION FOR ON-BOARD DATA RECORDING APPLICATIONS

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INTRODUCTION

When properly implemented, solid state memory technology can result in mass data storage products with very large mean time to failure (MTTF). Fairchild Space Company has developed a memory architecture for their Solid State Recorder (SSR), which optimizes solid state performance in terms of survival probability (> 10 years), speed (~ 140 Mbps), size, weight and power compared to market alternatives such as magnetic tape, magnetic disc, magnetic bubble and optical disc. The basis for the memory design was an in depth investigation of the survival probability of very large quantities of interconnected memory devices.

PROGRAM BACKGROUND

The objective of the SSR development program was the introduction of a new product that could be used as an on-board tape recorder replacement. Initial investigations into the size, weight and power requirements for a half-gigabit recorder, based on currently available semiconductor memory devices, indicated that these memories could be compactly packaged into a final size that would be comparable to existing mechanical recorders used in space. The goal of the recorder development was to extend the useful life of on-board recorders beyond the NASA experience of 3.5 years MTTF. A block diagram in Figure 1 illustrates the basic function blocks of the recorder design. A control section provides the circuitry for interfacing to the spacecraft telemetry and command (T&C) subsystem, establishes the data and control buses, and contains the central processing elements used

to control data flow and the basic recorder operation. The data and control buses allow expansion in memory (maximum of 32 cards or 16.4 gigabits) and input/ output (I/O) to a maximum of eight independent channels.

Before the detailed design could begin, several issues regarding the failure management technique, bit error rate control, memory architecture and hardware/ firmware partitioning needed to be resolved. As the memory was a common element in all these areas, an initial investigation was conducted to determine the failure probability of the large semiconductor memory. A relatively small, half-gigabit, capacity was considered. It very quickly became apparent that, although semiconductor device failure rates are very low, a mass memory system comprised of several hundreds of memories could not be expected to have a low failure rate. It also became obvious that this represented a problem that was generic to other applications where large scale memory is required.

As a result, the SSR development program began with an investigation of the mass memory problem in terms of defining an approach for reducing the memory system failure rates such that the SSR could have a survival probability of 0.95 for a five year mission. Based on successful results of this investigation, the development program was started.

INITIAL RELIABILITY STUDIES

Early in the mass memory development program, a series of reliability analyses were performed for a memory configuration consisting of 256K CMOS RAM devices and comprising a total memory capacity of $5x10^8$ bits. Objectives of the initial analyses were to:

a. Provide a comparison of the expected memory probability with that of other data storage devices, e.g. , tape recorders, having comparable storage capacity; and
b. Evaluate the improvement in reliability if error detection and correction (EDAC) is used to correct for random bit errors in the memory array.[1]

For the initial predictions, the memory configuration was defined as 256K x 1 RAM memory chips in an array n chips wide (with n dependent on the particular error detection and correction technique used) and sufficiently deep to provide the required memory capacity of $5x10^8$ bits. Shown in Figure 2, the processed data stream is stored starting across the top row (i.e., n bits) and continuing downward to fill a memory “page” defined

[1] It should be noted that, while EDAC techniques are intended primarily to improve system bit error rate by correction of “soft” errors in the processed data, they can also enhance the component reliability by compensating for memory device failures where such failures do not affect multiple bits in the same word.

as one row of memory chips (or 256K x n bits in this example). Data storage continues to the next page, and so on until the array is filled. When error detection and correction is used, the 256K x 1 chip is considered to be the most reliable architecture because, for almost all failure modes, loss of any single chip would affect only one bit in each n bit word.

Piece part failure rates used for the analysis were derived from Military Handbook 217, Revision E. Other significant assumptions included:

a. Part quality levels consistent with those normally used for military and spacecraft programs; i.e., Class B microcircuits, JANTXV discrete semiconductors, etc.;
b. A benign satellite environment, with operating temperature of 40°C;
c. Distribution of chip failures for large CMOS memories was based on informally obtained vendor data, reflecting burn-in and life test experience. On this basis, the failure rate was partitioned as 75% affecting single memory locations, with 25% (such as memory data or address faults) resulting in loss of multiple memory locations.

Statistics used for reliability calculations are not described in this paper. However, the methods used involve straightforward applications of the exponential failure distribution and the binomial equation for probability of success of redundant items (i.e., m of n required for success).

Results of the initial reliability analysis (which actually led to iterations of both the analysis and design trade-offs) are summarized in Table I. Not surprising, given the large number of large scale memory chips required, a calculation of memory reliability for a configuration with no capability for failure correction resulted in an extremely low value, less than 0.0001 probability of success for three years. It was surprising, however, that the addition of single bit error detection and correction, which utilizes a 64 bit word length plus eight check bits, increased the three year probability of success to only 0.132, which is still an unacceptable value for spaceflight operation. A more powerful EDAC code considered at that time could provide double error correction for words comprised of 113 information bits plus 15 check bits. While consideration of this approach resulted in a substantial improvement in reliability (to 0.692 for three years), this result was still deemed unacceptable; moreove At this point, additional approaches involving automated detection of failed memory sections and deletion of those sections from useable memory were considered. Shown in Table I, the simplest of these approaches (at least in concept) would provide for detection of two or more errors in each 72 bit word and, for subsequent write operations, would delete that line from the available memory. Using this approach, the reliability prediction for the $5x10^8$ bit memory increased to a value in excess of 0.999 for a three year mission duration.

Based on results of these initial analyses, it was concluded that the desired reliability for the solid state recorder memory could not be achieved through error detection and correction techniques alone, but that extremely high reliability can be achieved through detection and correction of single errors, with automated detection and memory deletion for more serious memory failures.

ALTERNATE MEMORY CONFIGURATION

Following the initial mass memory analyses, a second series of trade-offs was performed to ensure that the selected configuration would be the optimum one in terms of memory reliability and simplicity of circuit design. The key factors considered were:

a. Memory reliability, as reflected by the quantity of spare memory capacity which would be required to ensure high probability of success for an extended mission duration.
b. Complexity of the associated processor circuitry, e.g., memory address logic and EDAC circuitry, and the numbers of circuit interfaces between the processor and memory.

Figure 3 and Table II provide the trade-off data for eight memory configurations which could be used to comprise the 72 bit wide memory array of $5x10^8$ bit capacity. The configurations differ in terms of the memory devices used, i.e. 256K x 1 or 32K x 8, the method of substitution for failed memory sections, and the size of memory block to be substituted.

Substitution techniques which were considered include: 1) detection of 72 bit wide memory pages; 2) division of each page into smaller memory blocks and substitution of blocks within a column of the array; and 3) substitution of individual failed 256K devices, again within a column of the array.

For each of the eight configurations, Figure 3 provides a plot of expected mission lifelife, at 95% probability of success, versus the quantity of spare memory carried by the recorder; the results vary widely, with curves closest to the ordinate representing the configurations which require the lowest quantities of spare memory. Table II summarizes the results for five year mission life, and provides a qualitative assessment of the complexity of the processor logic circuits which would be required for implementation of the memory design.

SELECTED RECORDER CONFIGURATION

The memory configuration for the solid state recorder application was selected on the basis of the reliability analyses. From the results shown in Table II, configuration #8 has been selected by Fairchild as the optimum design. As illustrated in Figure 4, the recorder application uses a 72 bit wide word (64 data bits with 8 bits for error checking) which is made-up of 9 physical columns 8 bits wide. The depth is a function of the quantity of physical devices used and the scale of integration of each device. The memory is partitioned into pages which refer to a predefined depth size. For 32K x 8 bit devices, the page would be 32K x 72. This sizing was made software programmable so that pages could be compatible with the physical size of the memory devices. The error management plan is a combination of hardware implemented error detection and correction coding (EDAC) for single bit error correct and double error detect (modified Hamming code), and firmware controlled data patterns for read/write/ verify to find pages with sufficient numbers of permanent failures to compromise data storage. Pages so detected are inventoried in a bad page listing so that they will not be used for data storage. The EDAC is applied to the data real time as it is stored or retrieved. The pattern testing is done periodically in background processing. All of memory is tested in background (i.e., good pages and bad pages) so that temporary or "soft failures" do not permanently exclude pages of memory from further use. The reliability analysis has also been used to estimate the mean time between memory checking to maintain an acceptable bit error rate (BER). A typical BER for this application is of the order of 10^{-10} for the lifetime of the memory, which can be in excess of ten years with sufficient sparing.

SUMMARY AND CONCLUSION

As a result of the reliability modeling which was done in advance of any detail design, the technical risk in developing a very large scale solid state memory was greatly reduced. The apriori notion that it would be straight forward to just interconnect large numbers of memory devices was very quickly put aside with the reality of very low survival probability even when high reliability devices are used. The drivers for reliable performance are device failure rates, and to a greater extent, the error control plan, the memory architecture, operating environment and the quantity of spare devices. The analyses performed for this program are applicable to other implementations of very large scale solid state memory systems such as bulk storage for computers and large data systems, video buffers, communications networks, sensor arrays, rate converters, high speed multiplexing and secure communications components.

For specific applications of very large scale solid state memories, the design now needs to focus on the selection of support circuitry such that the overall reliability of the memory system is consistent with that of the memory itself. A further consideration is the

electronics packaging technology used. Implicit in the analysis presented was the assumption of individual die packaged in their own carriers. More exotic packaging techniques are available, however the fabrication technique for microelectronic modules may introduce increased failure rates of its own. For example, large chip and wire hybrids may be unattractive because of the number of internal wire bonds. For space applications, the trade-off between chip and wire hybrids versus mounting individually packaged memories still favors the later when the overall size and weight of the memory required is acceptable. Other microelectronic packaging technologies are emerging. Their evaluation was beyond the scope of this present analysis, however they will be the subject of future work.

The reliability analyses have resulted in a solution which is generically applicable to systems that require large scale solid state memories. As a semiconductor memory is a true random access device, it is possible to do simultaneous record and playback. The tape recorder mode of operation is only one of several possible memory applications. Other possible applications therefore are: a very large first in first out (FIFO) buffer for store and forward applications for single input single output (SISO), or as a multiplexer for multiple input single output (MISO), or as a demultiplexer for single input, multiple output (SIMO). The SSR can also be used in large memory archival systems to manage the receiving and routing of multiple high speed data sources. The ability to implement properly, large solid state memory arrays will give rise to many other applications which may reduce demands on data management systems for today’s payloads of multiple high speed data sources.

Perhaps most important, the mass memory development program can be considered a case history in the effective use of reliability prediction methodology early in the design process, and the importance of the analysis results as an input when key (and often irreversible) design decisions are made.

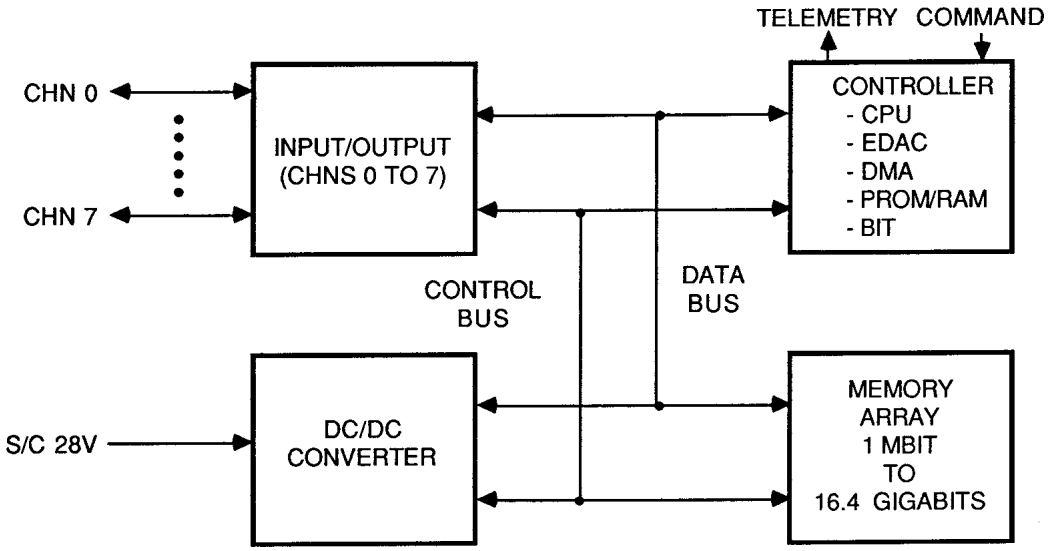

Figure 1. SSR Functional Diagram

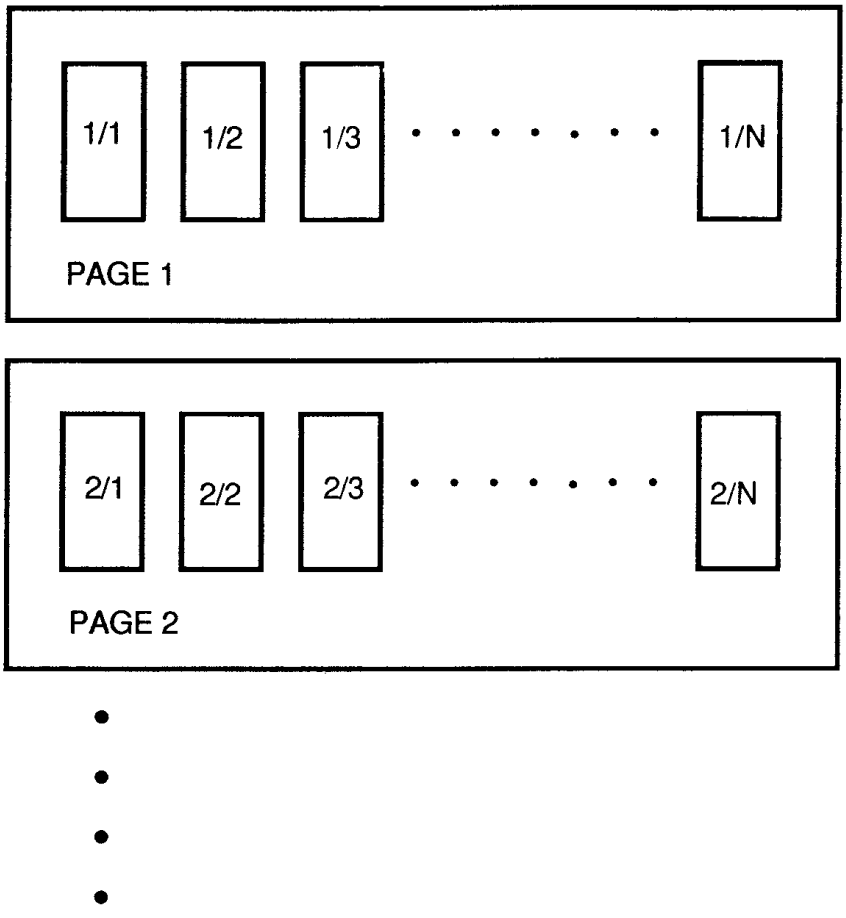

Figure 2. Memory Configuration for Initial Reliability Evaluation

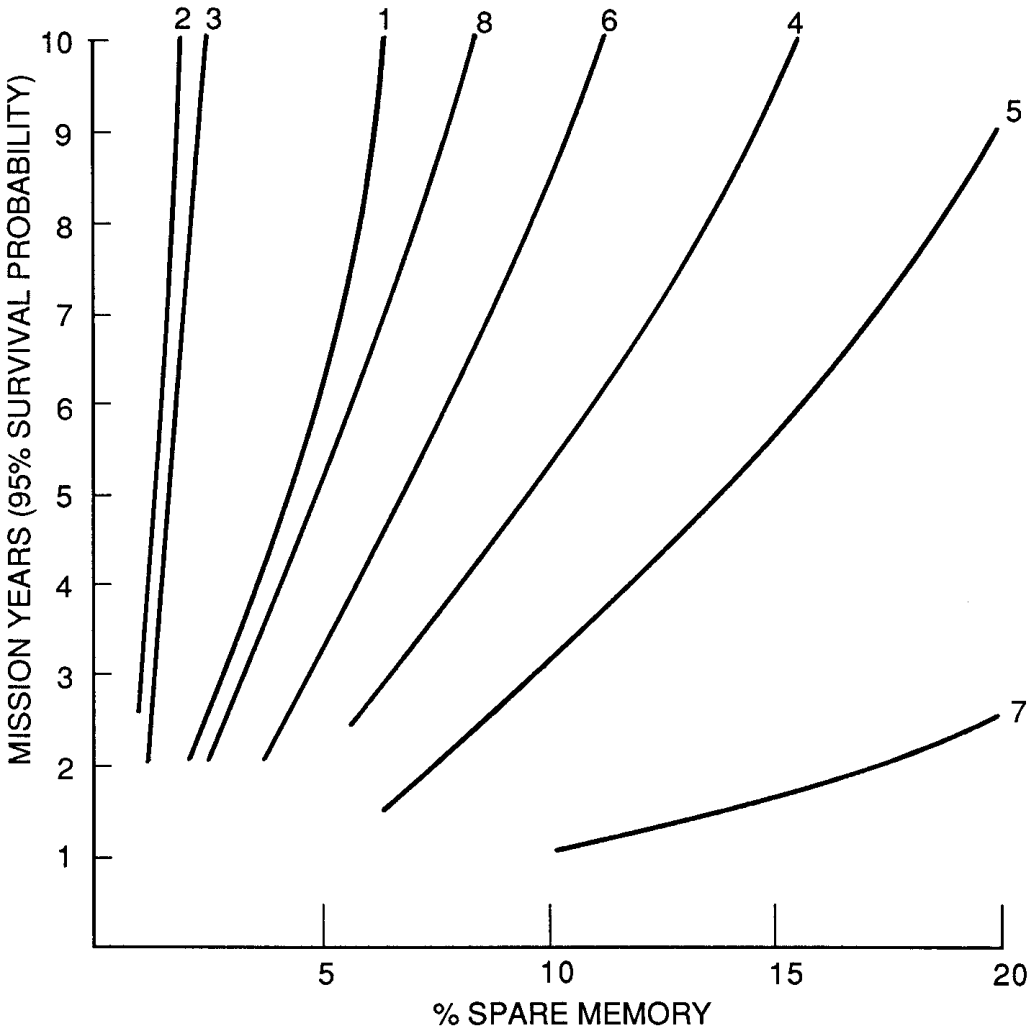

Figure 3. Expected Life vs. Spare Memory Capacity for Alternate Memory Configurations

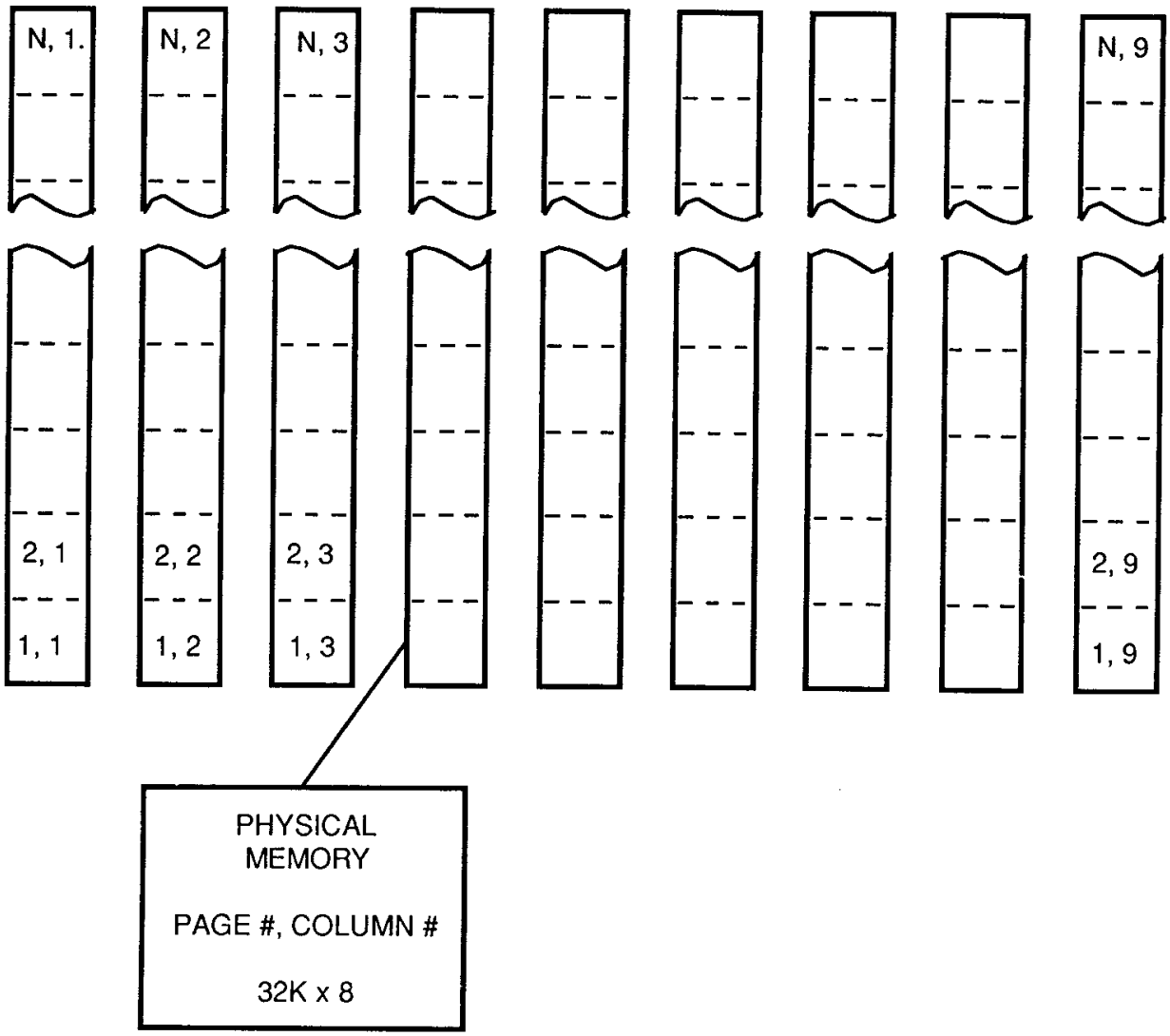

Figure 4. Memory of Architecture for Solid State Recorder Application

Table 1. SSR Reliability Assessment

Memory Configuration	EDAC Capability	Memory Deletion	3 Yr Memory Reliability
256K x 1 Devices Qty 2048	None	None	< 0.001
256K x 1 Devices Qty 2304	Single Error Correct	None	0.132
256K x 1 Devices Qty 2304	Double Error Correct	None	0.692
256K x 1 Devices Qty 2520 (10% Spare Capability)	Single Error Correct	Delete 72 Bit Line on Second Bit Failure	> 0.999

Table II. Comparison of Alternate Memory Configurations

Approach Number	Device Type	Page Size	Block Size	Level of Substitution	% Spares*	Processor Complexity
1.	256K x 1	256K x 1	-	Device	4.7	High
2.	32K x 8	32K x 72	-	Device	1.4	High
3.	32K x 8	32K x 72	32K x 16	Block	1.8	High
4.	256K x 1	256K x 72	256K x 8	Block	10.0	Medium
5.	256K x 1	256K x 72	256K x 16	Block	13.9	Medium
6.	32K x 8	128K x 72	128K x 16	Block	7.0	Medium
7.	256K x 1	256K x 72	-	Page	>20	Low
8.	32K x 8	32K x 72	-	Page	4.9	Low

* Required to achieve 0.95 memory reliability for five years