HIGH SPEED SYNCHRONIZER CARD UTILIZING VLSI TECHNOLOGY

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ABSTRACT

A high speed Synchronizer Card utilizing semi-custom and custom very large scale integration (VLSI) devices, microprocessor control, and programmable logic has been designed to provide a generic NASA Communication (NASCOM) block processing and telemetry frame synchronization function for present missions and Space Station era telemetry data streams at data rates up to 25 Mbps.

The Synchronizer Card utilizes four distinct sets of VLSI semi-custom and custom chips to shrink all of the functions required for NASCOM block processing, telemetry frame synchronization, real time quality trailer appendage and cumulative quality statistic generation into a single Synchronizer card. This paper will describe the functions performed by the Synchronizer Card and each individual set of chips.

INTRODUCTION

Previous methods for providing NASCOM block processing and telemetry frame synchronization involved the use of custom medium scale integration (MSI) systems consuming multiple cards and racks of equipment. Hundreds of these systems exist today within NASA's telemetry data systems. All of these systems are similar in function and were built by a variety of vendors. Future missions and Space Station era telemetry systems will demand hundreds more. With the advent of VLSI and Computer Aided Engineering (CAE) technology over the last few years, the ability to integrate all of the common synchronization functions into a single card has become possible. Integration into a single card will result in higher performance, lower cost, increased reliability, and simpler telemetry system design.

In developing the design specifications for the Synchronizer Card, three operational synchronization systems were studied: the Space Telescope Data Capture System (1), the Multi-Satellite Operational Control Center Telemetry and Command System (2), and the Packet Processing (PACOR) System (3). Each of these systems was built for a specific application, however, each system provides basically the same functions. Future Space Station era requirements were also studied based on the Consultative Committee for Space Data Systems (CCSDS) recommendations (4). These design specifications were then used to develop a generic Synchronizer Card capable of handling present and future synchronization requirements.

The Synchronizer Card has been implemented through the use of four distinct sets of VLSI chips with dedicated microprocessor control. These four VLSI chip sets include:

- NASCOM Block Processor chip set (NBPCS)
- Telemetry Frame Synchronizer chip set (TFSCS)
- Data Simulation chip set (DSCS)
- Cumulative Quality chip set (CQCS).

Each of the four VLSI chip sets has unique functional characteristics which can stand alone or be used together with minimal interfacing.

Design and simulation of each VLSI chip set was conducted in parallel on an in house CAE system. These designs were then integrated, again with the use of the CAE, into a comprehensive card design which was simulated and tested before fabrication. With minor revisions, a completed Synchronizer Card has been fabricated which is currently being tested for different mission scenarios: in the Enhanced Front End Data Capture System for PACOR, in the new Telemetry and Command System for the MSOCC, and in the Virtual Channel Sorter Multiplexer System prototype for Space Station Era telemetry data systems. This card will provide a ten to one improvement in cost, performance, and size of current MSI systems, and a great improvement in reliability.

SYNCHRONIZER CARD

The Synchronizer Card [Figure 1] is physically a 9U VME card. One third of the card is a commercially available single board computer (MIZAR 8115) used as the Synchronizer Card Channel Controller (SCCC). This card utilizes a 12.5 Mhz Motorola 68010 microprocessor with 512k bytes of RAM. The custom logic card is connected through a side connector provided on the controller card. It is the custom logic card which contains all the specialized hardware functions for synchronization.

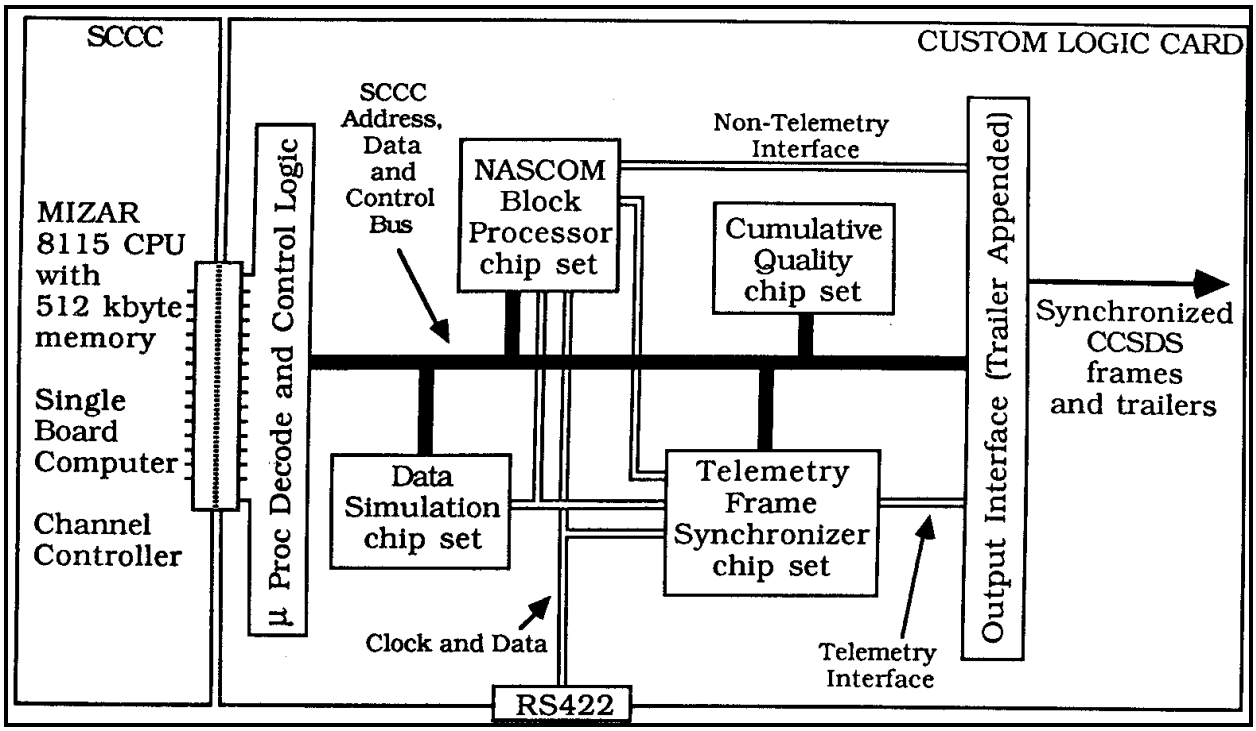

Figure 1 - Synchronizer Card

The SCCC is a dedicated processor which provides setup, self-test, hardware diagnostics, debug, and control over the custom logic card. Extensive software to control the card and provide complete status information has been written and integrated on the SCCC.

While operational, the custom logic card provides the hardware functions necessary to perform high speed NASCOM block processing, telemetry frame synchronization, real time frame trailer appendage, and cumulative quality generation. It can also perform data simulation for self-checking purposes. To further explain Figure 1 and to demonstrate how each of the four chip sets interact to form the Synchronizer Card, a brief overview follows.

Setup and control information (i.e. sync patterns, frame lengths) is transferred through the Microprocessor Decode and Control logic to all of the other subsystems from an operational program run on the SCCC. Self-test pattern data which resembles the mission data is also transferred to the Data Simulation Chip Set.

The NASCOM Block Processor Chip Set (NBPCS) can be enabled to accept data from either the Data Simulation Chip Set (DSCS) or from the RS422 interface. Data formatted in 4800 bit NASCOM Blocks is synchronized to the programmed sync pattern. Two output paths from this subsystem exist. For both paths the header (entire 144 bits) of each NASCOM Block can be read by the SCCC. If data is determined to be telemetry data, the NASCOM Block header and trailer is stripped away and a serial stream of only telemetry bits (fill bits ignored) is output to the Telemetry Frame Synchronizer Chip Set (TFSCS). If

the block is determined to be non-telemetry (i.e. command block) the entire block can be transported off the Synchronizer Card. Additionally, the NBPCS performs quality checks on each block received including cyclic redundancy code (CRC) and sequence checks.

The Telemetry Frame Synchronizer chip set (TFSCS) can be programmed to select data from either the RS422 interface, the DSCS, or the NBPCS. A complete synchronization strategy can be programed for the selected data stream. Complete search, check, lock strategies, and slip windowing is provided. Additionally the TFSCS has the ability to correct inverted or reversed frames. A status word for each frame is reported back to the SCCC. This status word contains sync mode, sync errors, slip indication, CRC errors (if applicable), and data type (forward, reverse, inverted, or true) of frame received. The TFSCS provides complete double buffering of frames and automatic output with framing control signals. Output control strobes allow for automatic status counting.

The Output Interface can be programed to select either the telemetry or non-telemetry data path. Quality data generated by the SCCC is appended to the selected output path. The output interface then controls the transfer of this annotated data to the next processing system.

The Cumulative Quality Chip Set (CQCS) accepts control strobes from the NBPCS, the TFSCS and from the SCCC and accumulates 32 status counts for up to 224 events ($\approx$24 million). These counts are read by the SCCC periodically and formatted into a complete status block. The status block can be formatted on a display terminal connected to the SCCC or communicated to a higher level system controller.

The Data Simulation Chip Set (DSCS) provides complete self-testing of all functions on the Synchronizer Card with high speed (up to 25 Mbps) simulation data. Once set up for output, the DSCS can provide independent output of a serial telemetry data stream. This stream can be programmed to provide any type of data (forward, inverted, reverse, or true) in any format for a known number of repetitions. By comparing the status results for the test run against known correct results, the SCCC can determine if the card is functioning correctly before activating it for operational data.

The four VLSI Chip Sets which make up the core functions of the Synchronizer Card are discussed in more detail in the following sections. A block diagram of each chip set is provided to assist in the understanding of each discussion. These chips sets can either stand alone or can be integrated together as they are on the Synchronizer Card described above.

NASCOM Block Processor Chip Set

The NBPCS consists of six chips connected to the SCCC through a standard memory mapped interface. [Figure 2] These six chips perform all of the functions necessary for synchronization to NASCOM 4800 bit blocked data and for extraction of all quality and telemetry data from the block.

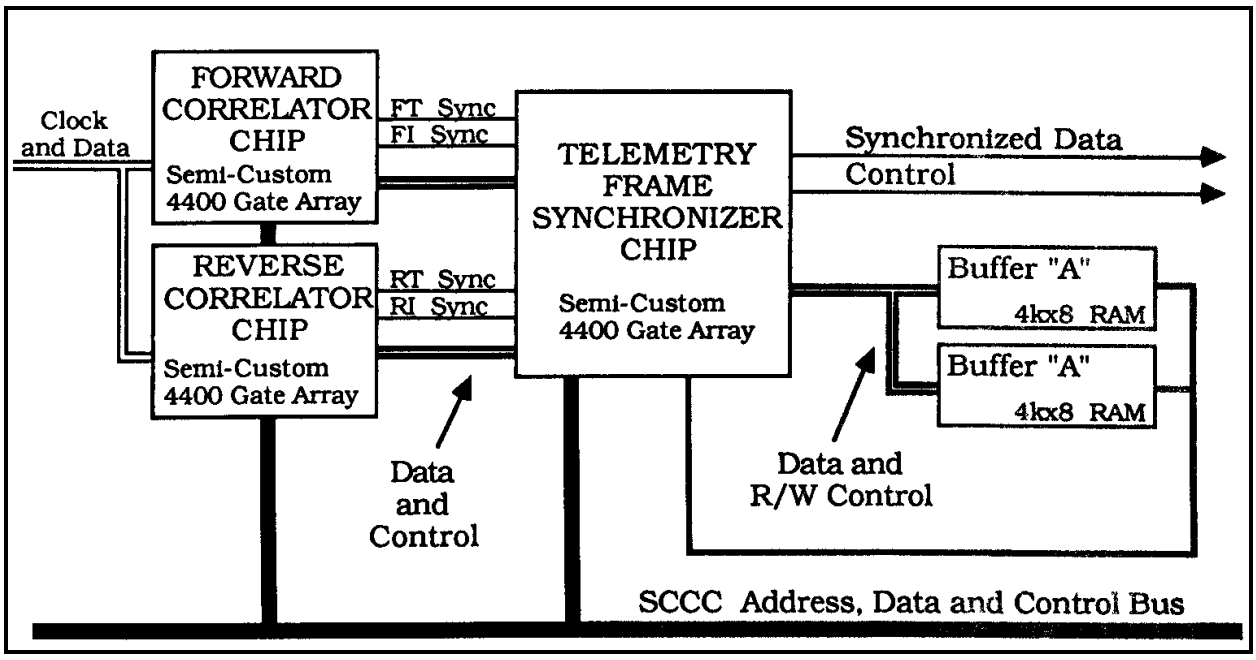

Figure 2 - NASCOM Block Processor Chip Set

The first function of the NBPCS is data correlation to the NASCOM 24-bit synchronization pattern. The Correlator Chip (a semi-custom 4400 gate array), which allows for up to a 32 bit programmable synchronization pattern with error tolerances, is used to indicate the beginning of a NASCOM 4800 bit block. With this indication of synchronization, the NASCOM Block Processor Chip (NBPC) (also a semi-custom 4400 gate array) begins to process the incoming NASCOM blocks. Three major functions are performed on each block by the NBPC.

For each block the entire NASCOM 144 bit header is stored as nine 16 bit words. This data is accessible through a 16-bit interface controlled by the SCCC. The SCCC can look at any of the words and determine block type and routing as well as extracting the timecode or any other required information. The SCCC receives two separate interrupts from the NBPC: one which indicates that the NASCOM Block header has been completely received and is available for reading, and a second which indicates that the last bit of the 4800 bit block has been buffered. This allows the SCCC time to determine and set up routing, check sequence and CRC errors, and perform cumulative quality tasks.

The second major function the NBPC performs includes data quality and sequence checks. A Cyclic Redundancy Check (CRC) of each block, using the standard 22 bit NASCOM CRC code, is performed. A sequence check for TDRSS type blocks is performed automatically. Error flags for the CRC, and sequence checks are output to a status register accessible through the SCCC bus.

Automatic buffering of telemetry and non-telemetry data is the third major task performed by the NBPC. For telemetry data, only the telemetry bits in the NASCOM data field are buffered and passed serially out through the telemetry clock and data outputs. Non-telemetry NASCOM blocks are stored in a separate double buffer and transferred to the Output Interface.

Telemetry Frame Synchronizer Chip Set

The TFSCS consists of five VLSI circuits connected to the SCCC through a standard memory map interface. [Figure 3] These five chips perform all of the functions necessary to correctly synchronize to each telemetry frame received, correctly buffer each frame, and output the frame to the next system element.

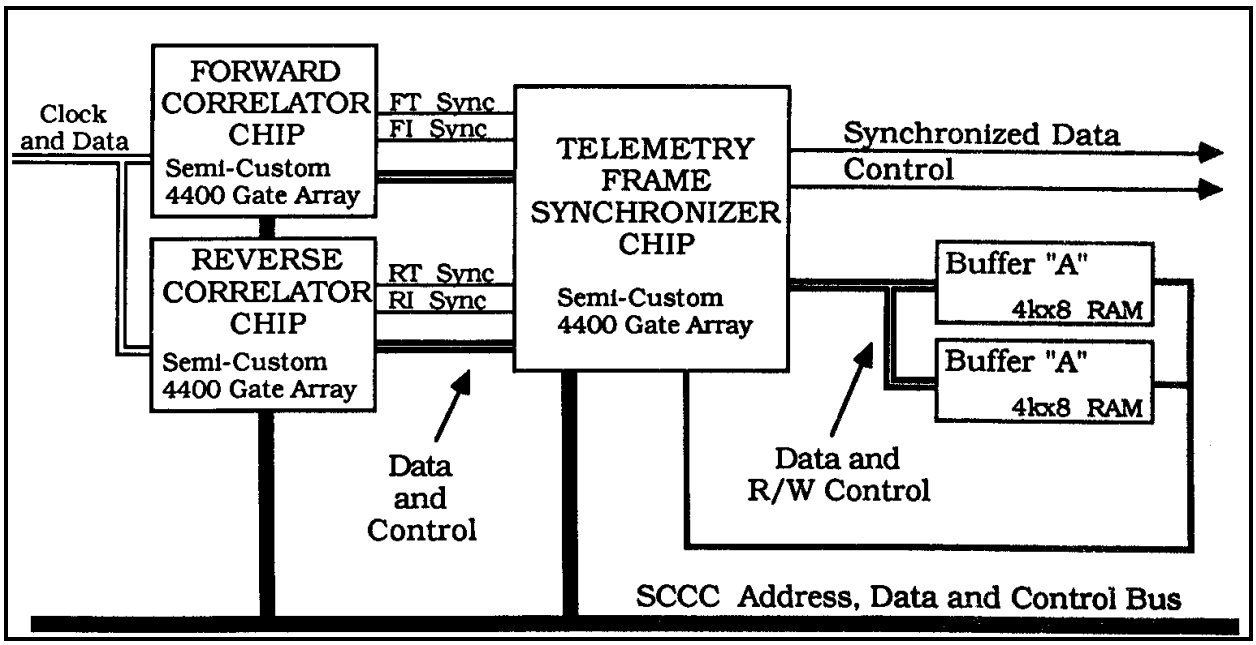

Figure 3 - Telemetry Frame Synchronizer Chip Set

The TFSCS accepts serial clock and data signals from either the NBPCS, the DSCS or directly from the RS422 interface on the Synchronizer Card. The chosen data and clock signals are fed into both of the TFSCS Correlators. These two correlators are the same chip used in the NBPCS. One correlator is programmed to look for a forward synchronization pattern while the other is programmed to look for a reverse

synchronization pattern. Each correlator outputs both a true sync and an inverted sync signal, and the number of synchronization errors found for each. These signals are fed into the Telemetry Frame Synchronizer Chip (TFSC). This gives the TFSC the ability to process any combination of forward true (FT), forward inverted (FI), reverse true (RI), and reverse inverted (RI) telemetry frames. Search, check and lock sync pattern error tolerances can be programmed for any of the four types of data. In this way both real-time and playback data can be processed if necessary in one chip set.

The TFSC can be programmed to accept or reject any of the four sync indications from the forward and reverse correlators (FT, FI, RT or RI) as a valid sync indication. Once a valid sync pattern has been accepted, the TFSC begins implementation of its pre-programmed synchronization strategy.

An optional best match strategy allows the TFSC to select the first sync pattern with the least errors before creating its sync pattern search window. The sync pattern search window is capable of a programmable (±3 bits) tolerance and ensures that the same size frame is buffered. A completely programmable search, check, lock and flywheel strategy ensures correct buffering and output of each frame.

A double buffering scheme allows the TFSC to obtain status information on each frame and correct for reverse and inverted frames if desired. Two commercial 4kx8 RAM chips separately addressed by the TFSC provide for the correct buffering of each frame. An automatic output path from the double buffers reads out each synchronized frame. A data valid signal indicates when each byte is valid out of the buffer and a control signal indicates the first and last byte of each frame for maintaining down line synchronization.

Status information collected for each frame processed includes, type of frame processed (FT, FI, RT or RI), mode of TFSC (search, check, lock or flywheel), sync pattern errors, and slip errors. The standard CCSDS CRC code for both forward and reverse is applied to each frame and indication of any errors in this check is also stored in the status register. Status for each frame is collected by the SCCC through an interrupt which is activated at end of each processed frame.

Cumulative Quality Chip Set

The CQCS consists of two Spectrum Accumulator Chips (a full custom device developed by Johns Hopkins Applied Physics Laboratory) each of which contains sixteen 24 bit counters. Toggling rates for each of the counters is in excess of 40 Mhz. This chip set provides for the accumulation of up to 32 separate hardware events. An event can be

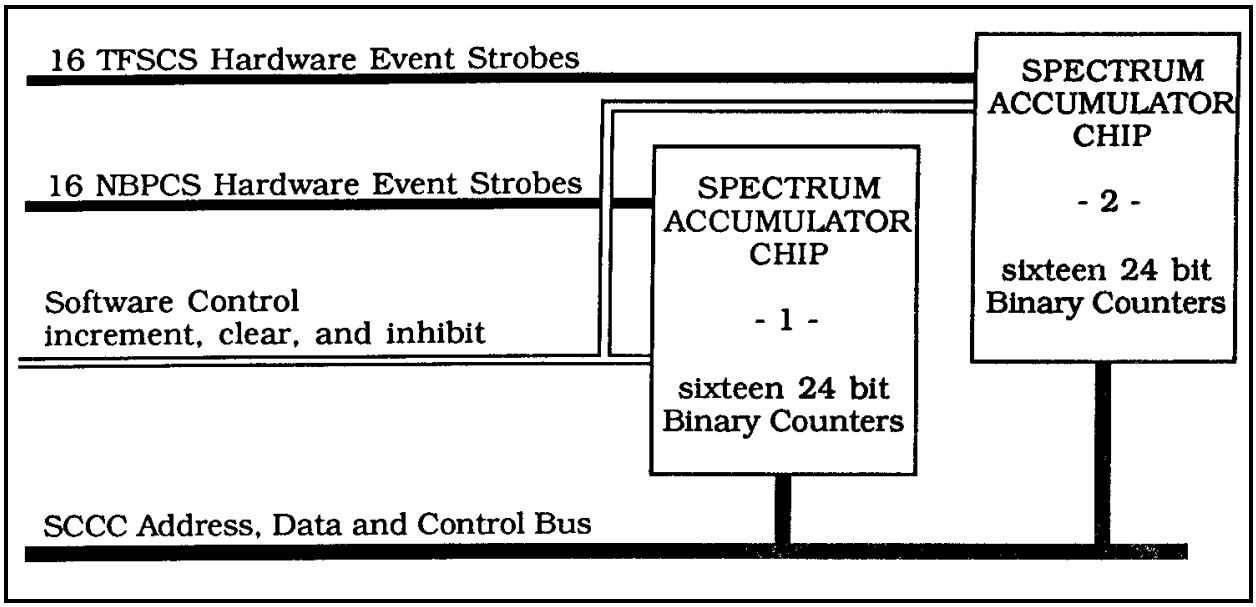

Figure 4 - Cumulative Quality Chip Set

assigned to any one of 32 counters each with programmable increment, clear and inhibit controls. A standard memory map interface enables the SCCC to read out any of the 32 bit counters in two steps onto the SCCC bus.

The first Spectrum Accumulator Chip is used to accumulate counts of events related to the NBPCS. Some of the 16 events counted include the number of blocks received and the number of times a sequence error was found. The second Spectrum Accumulator Chip is dedicated to counting events for the TFSCS. Examples of some of the 16 events counted include the number of telemetry frames received and the number of frames with slip errors. All of these counts along with other status information are gathered and formatted into a comprehensive status block that can be displayed on a display terminal connected to the SCCC or transferred by the SCCC to a monitoring system.

Data Simulation Chip Set

The DSCS consists of the Testchip (a 6000 gate semi-custom gate array) and a commercial 4kx16 RAM. This chip set provides for the independent generation of self-test data, for the Synchronizer Card. To provide this function, up to 1M bit of pattern data is downloaded from the SCCC through the Testchip [Figure 5] into the pattern data memory. This data can be formatted to look like expected mission data.

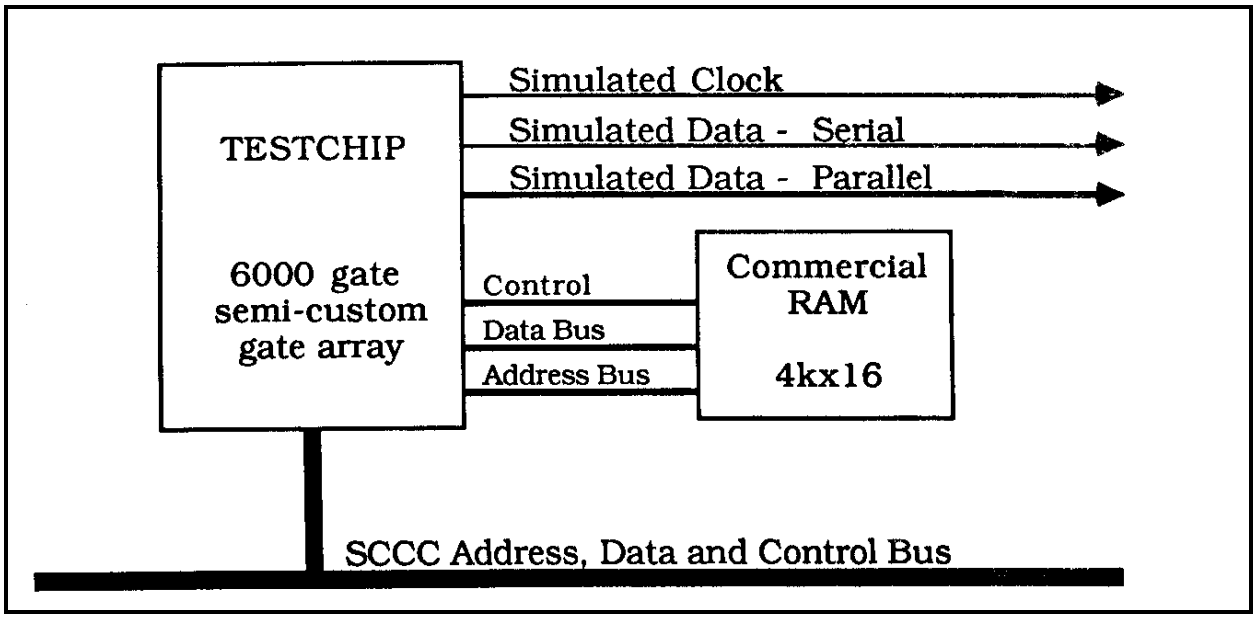

Figure 5 - Data Simulation Chip Set

The Testchip can be programmed to invert or reverse the pattern data, and transfer a known number of frames or blocks through either a serial interface or through an 8-bit parallel interface. Once enabled for output, the Testchip begins its programmed sequence and acts like an independent source of data. Output data rates in discrete increments from 1 Kbps to 25 Mbps can be programmed into the Testchip.

For extensive self-testing functions, the DSCS can be configured to use dual ported pattern memory. In this configuration one side of the pattern memory is controlled by the Testchip while the other side can be updated by a control processor (i.e. the SCCC). The Testchip can also be programmed to partition the pattern memory into two separate output buffers. In this way a control processor can update one partition while the other partition is being output. Complete updating of the entire partition or selected updating of data fields (i.e. sequence field, timecode field etc.) allows for simulation of a extensive (over 1 Gbyte) continuous data pattern.

Through the DSCS a complete checkout of a single function on a card or the entire data path of the card can be tested without the need for external test apparatus. Hardware or software problems on the card can be diagnosed and reported to a monitoring system before actual data is allowed to be processed.

CONCLUSION

A generic Synchronizer Card capable of providing standard NASCOM block, telemetry frame synchronization and quality control has been fabricated using VLSI technology.

Construction of the Synchronizer Card involved the development of four VLSI chip sets which can be integrated together or used independently in other applications. The application of VLSI technology to telemetry systems has resulted in a increase in performance, and a decrease in cost and size.

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NOMENCLATURE

CAE	Computer Aided Engineering
CCSDS,	Committee for Space Data Systems
CQCS	Cumulative Quality Chip Set
CRC	Cyclic Redundancy Code
DSCS	Data Simulation Chip Set
MSI	Medium Scale Integration
NASA	National Aeronautics and Space Administration
NASCOM	NASA Communication
NBPC	NASCOM Block Processor Chip
NBPCS	NASCOM Block Processor Chip Set
PACOR	Packet Processing
RAM	Random Access Memory
SCCC	Synchronizer Card Channel Controller
TFSC	Telemetry Frame Synchronizer Chip
TFSCS	Telemetry Frame Synchronization Chip Set
VLSI	Very Large Scale Integration
VMFE	Versabus Module Eurocard format