AN INTELLIGENT DIGITAL PHASE-LOCKED LOOP WITH INTEGRAL GAIN CONTROL, SIGNAL QUALITY AND LOCK DETECTION

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ABSTRACT

An intelligent digital phase-locked loop with integral automatic gain control, signal quality and lock detection suitable for implementation using current digital signal processing devices is presented. By exploiting information derived from these functions operating in unison, it is possible to realize improved performance in an adverse environment where fading or abrupt signal outages are encountered.

The system described consists of several functions operating under the direction of a stored program. The state diagram model of the program is discussed along with design considerations for the system elements. Various aspects of the system are simulated in the presence of noise and signal outage and compared to the performance of a conventional phase-locked loop.

INTRODUCTION

Phase-locked loops are an essential element in most communication systems. Currently, there is an increased interest in making maximum use of digital devices in the design of these systems. Digital implementations offer the obvious advantages of cost, size, predictability and reliability. Moreover, with digital elements operating under the supervision of a stored program, heuristic functions may be incorporated into loop operation as well as several other complementary functions. For low to moderate signal bandwidths, it is possible to realize communication systems using current digital signal recessing technology.

This paper examines the practicality of implementing an intelligent digital phase-locked loop (PLL) which operates in conjunction with the automatic gain control (AGC), signal quality and lock detector functions. The proposed system, as shown in Figure 1, utilizes a carrier and bit clock tracking loop and represents a typical communication receiver. The

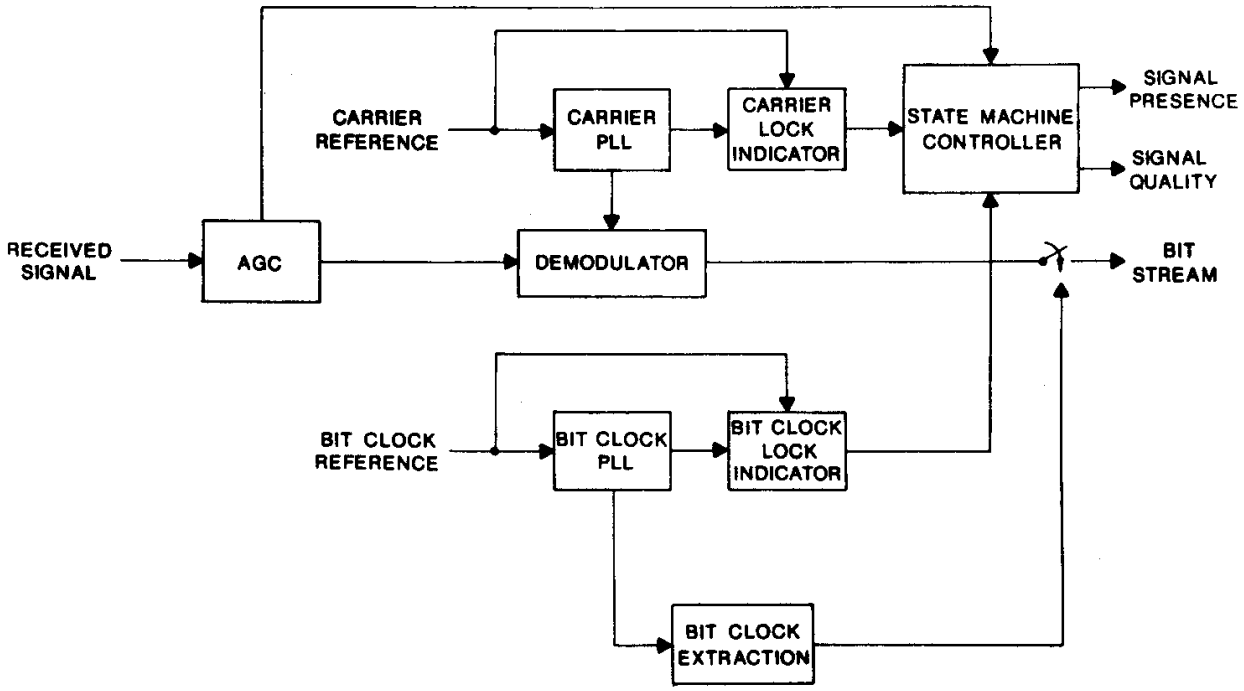


FIGURE 1. SYSTEM BLOCK DIAGRAM

principles presented herein can be applied to any system utilizing a phase-locked loop. However, the detailed system implementation will be application dependent. Therefore, this paper explains the operation in general terms with particular emphasis on identifying key system parameters and trade-offs.

SYSTEM DESCRIPTION

Digital Phase-Locked Loop

The PLL consists of a phase detector, loop filter and voltage controlled oscillator (VCO). In general, the loop is nonlinear due to the phase detector. However, the loop behaves linearly for small phase errors. Given this assumption, the PLL may be modeled as shown in Figure 2. An all digital PLL suitable for software implementation can be synthesized by the transformation of a conventional analog system, whereby the poles and zeros of a specified differential equation are mapped to the z-plane poles and zeros of a corresponding difference equation using the matched z-transform (1). Using this method, the first order analog PLL described by the closed loop transfer function

$$H(s) = \frac{K}{s + K} \tag{1}$$

can be transformed to its discrete equivalent

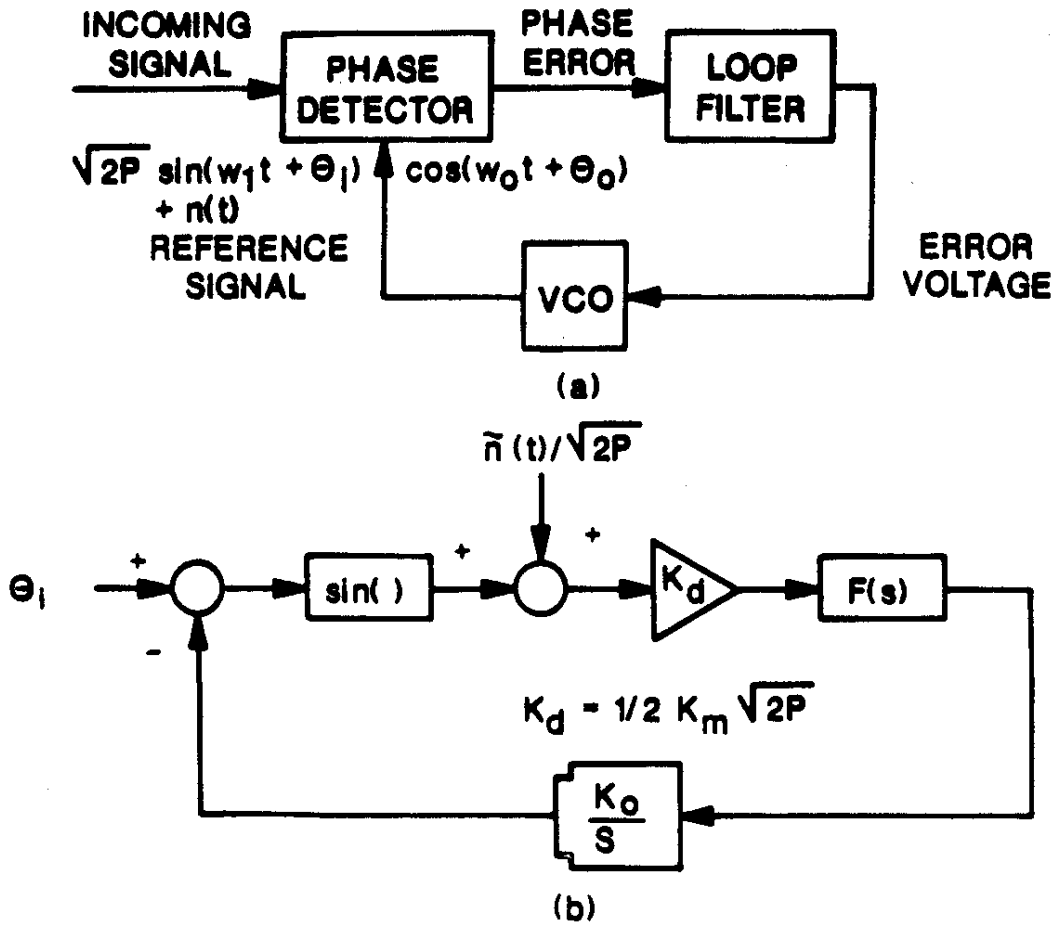


FIGURE 2. PHASE-LOCKED LOOP.
(a) BLOCK DIAGRAM, (b) LINEARIZED LOOP MODEL.

$$H^*(z) = \frac{K^*}{z - (1 - K^*)} \tag{2}$$

where K and K* are the collective loop gains for the analog and discrete PLL, respectively.

In the digital implementation, the VCO function can be implemented using table lookup techniques where the phase is updated using the recursive relationship

$$\theta_o(n) = \theta_o(n-1) + K_o\,\tilde{e}(n-1) \tag{3}$$

where K_o is the gain of the digital VCO and is included in the loop gain K*. The term ẽ (n) is the nth error sample out of the loop filter.

The phase produced by equation 3 can be added to a fixed step size to produce an index to a table containing sine (or cosine) values uniformly spaced around the unit circle (3). It can be shown that the step size required to produce a sinusoid of frequency f_o is given by

$$\Delta = N f_o T_s \tag{4}$$

where N is the number of entries in the table and T_s is the sampling period. Note that, for this case, the gain K_o is equal to N steps/2Π radians.

Taking the z-transform of equation 3 with some manipulation yields the discrete VCO transfer function

$$D(z) = \frac{\theta_o(z)}{E(z)} = \frac{K_o z^{-1}}{1 - z^{-1}} \tag{5}$$

where θ_o (z) and E(z) are the z-transforms of the discrete time sequences θ_o (n) and e(n). The loop filter gain can be determined by factoring out the VCO term. Doing so yields the result

$$K^* = \frac{1 - e^{-KT_s}}{K_o K_d} \tag{6}$$

where K_d is the phase detector gain.

Provided that the sampling rate is sufficiently high so that the discrete system accurately matches the analog system, the loop bandwidth can be approximated by

$$B_L \cong \frac{K}{4} \qquad \text{for a Type I Loop Filter} \tag{7}$$

where the bandwidth is in Hertz.

This technique can be extended for a type II high gain lag-lead network described by the transfer function

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{8}$$

where ω_n and δ are the natural frequency (radians/sec) and damping factor of the loop, respectively. Transformation of this system results in a loop filter of the form

$$F(z) = G_1 + \frac{G_2}{1 - z^{-1}} \tag{9}$$

where the loop filter gain terms G_1 and G_2 are given by

$$G_1 = \frac{1}{K_o K_d}\left(1 - e^{-2\zeta\omega_n T_s}\right) \tag{10}$$

and

$$G_2 = \frac{1}{K_o K_d}\left(1 - 2e^{-\zeta\omega_n T_s}\cos\left(\omega_n T_s\sqrt{1-\zeta^2}\right) + e^{-2\zeta\omega_n T_s}\right) \tag{11}$$

The loop filter is implemented as shown in Figure 3. The loop bandwidth can be approximated by

$$B_L \cong \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) \qquad \text{for a Type II Loop Filter} \tag{12}$$

for sampling rates in excess of 25 times the loop bandwidth (1).

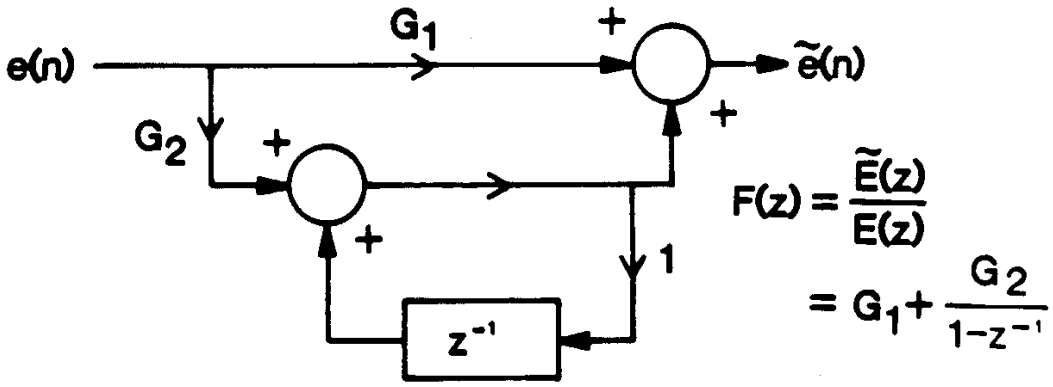


FIGURE 3. DISCRETE LOOP FILTER FOR A HIGH GAIN LAG-LEAD LOOP.

In most cases the first order PLL will be sufficient for the bit clock loop because the frequency uncertainty is limited to the accuracy of the transmit and receive oscillators. The steady-state phase error introduced by a fixed frequency offset is given by Gardner (2) as:

$$\varnothing_v = \frac{\Delta\omega}{K_{DC}} \qquad \text{for a Frequency Step} \tag{13}$$

in radians where K_{DC} is the DC loop gain and $\Delta\omega$ is the frequency offset in radians. The DC loop gain, for the first order loop, is the collective loop gain K.

Given that the transmit and receive oscillators are accurate within 100 ppm and loop bandwidth is 10 Hz, the steady-state phase error is approximately one degree at a nominal clock rate of 1200 baud. However, large frequency offsets are encountered in the carrier loop due to equipment mistuning and Doppler related effects. Furthermore, the frequency of the carrier loop can change with time as a result of vehicle or medium motion. For these cases, a type II loop is required to provide reasonable tracking performance. This loop has infinite d.c. gain and, therefore, zero steady-state phase error for a phase and frequency step. The tracking error (in radians) in the presence of a linearly changing frequency is (2):

$$\varnothing_a = \frac{\Delta\dot{\omega}}{\omega_n^2} \qquad \text{for a Frequency Ramp} \qquad (14)$$

where $\Delta\dot{\omega}$ is the rate of change.

Automatic Gain Control Circuit

The purpose of the AGC circuit is to maintain the input signal at a constant level, thereby providing accurate control over the PLL bandwidth and reliable indication of phase lock. In general, the AGC circuit does not discriminate between signal and noise. This type of AGC is referred to as a noncoherent AGC since the control voltage is derived by filtering (smoothing) the square of the incoming signal. Therefore, if the noise power exceeds the signal power, the AGC is driven primarily by the noise. Given that the AGC maintains a constant rms voltage, V_o, the adjusted signal amplitude, A, can be related to the SNR by:

$$A = \propto \sqrt{2}\, V_o \qquad (15)$$

where the signal is assumed to be sinusoidal and α is the signal suppression factor defined by the relation (4):

$$\propto = \sqrt{\frac{\rho}{1+\rho}} \qquad (16)$$

where is

$$\rho = \log^{-1}\left(\frac{SNR}{10}\right) \qquad (17)$$

For SNR's below 10 dB, the reduction in signal amplitude is no longer negligible and must be considered when selecting threshold levels. This problem can be overcome once phase lock has been achieved by using the coherent reference of the PLL to synchronously detect the signal energy. In this manner, the noise contribution may be suppressed through filtering with the noise rejection being inversely proportional to the filter bandwidth.

Although coherent detection will allow the AGC to track only the signal power, the receiver must still provide adequate dynamic range to preserve the total signal.

The peak-to-rms ratio (crest factor) is a critical AGC design parameter. Excessive loading will cause clipping of the received signal. On the other hand, insufficient loading will result in loss of dynamic range. The sum of a sinusoidal signal plus narrow-band Gaussian noise has a Ricean distribution (5). The probability density function can be integrated over the A/D range to determine the probability of clipping.

Selection of the AGC bandwidth is a final consideration. The AGC bandwidth will determine the attack and decay times of the AGC loop, thereby establishing the performance of the AGC during signal fades. Note that if the AGC bandwidth is on the order of the PLL bandwidths, the AGC will affect the tracking performance of these loops. A detailed analysis of the AGC is given by Victor and Brockman (6). The equations produced by Victor and Brockman can be transformed to the discrete domain using the same method discussed for digital PLL design.

Lock Indicator

The lock indicator can be implemented using the quadrature PLL reference signal. The filtered product of this reference with the PLL input is proportional to the instantaneous phase error weighted by the input signal amplitude. Since the AGC maintains a constant signal level, the output provides a measure of phase lock. Note, however, the signal suppression factor, α, should be considered in the selection of the lock indicator thresholds. For example, with a noncoherent AGC and a SNR of 0 dB the lock indicator will reach only 70.7 % of its full scale value (i.e., in absence of noise) as shown in Figure 4.

Signal Presence Detection and Signal Quality

The AGC control signal, when compared against a threshold, can be used to detect the presence of the signal. However, noise fluctuations in the control signal can cause false detections. The probability of false alarms will depend on the AGC bandwidth and noise level. Smoothing of the control signal for purposes of signal presence detection can be performed by additional filtering or by introducing hysteresis in the threshold detection. Hysteresis will prevent the signal presence function from continually being turned on and off when operating near the detector threshold. Signal quality can be ascertained using the AGC control signal and the lock detector levels. For example, the signal suppression factor, α, can be determined from the lock indicator level and, thus, the SNR can be computed from equations 16 and 17.

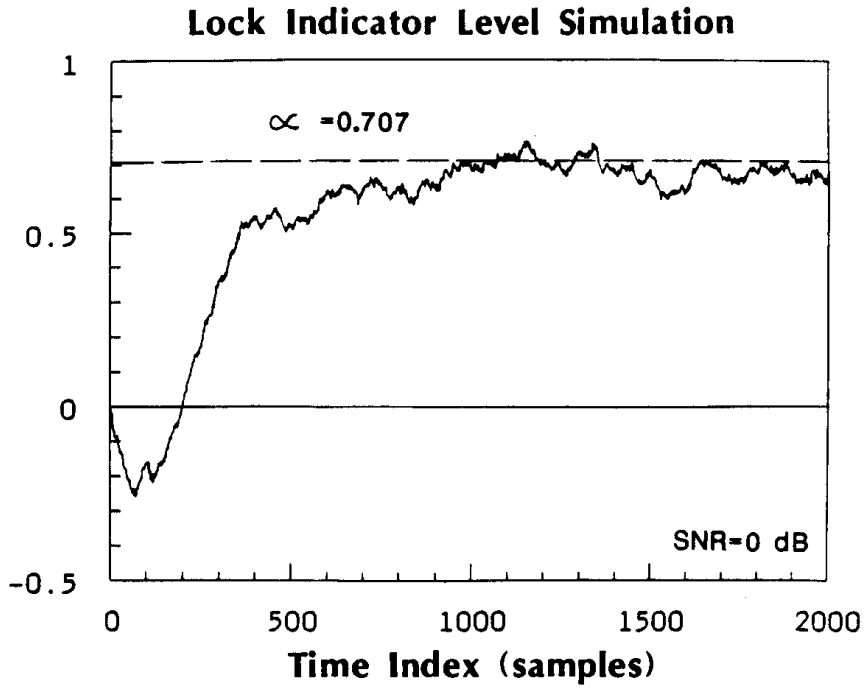
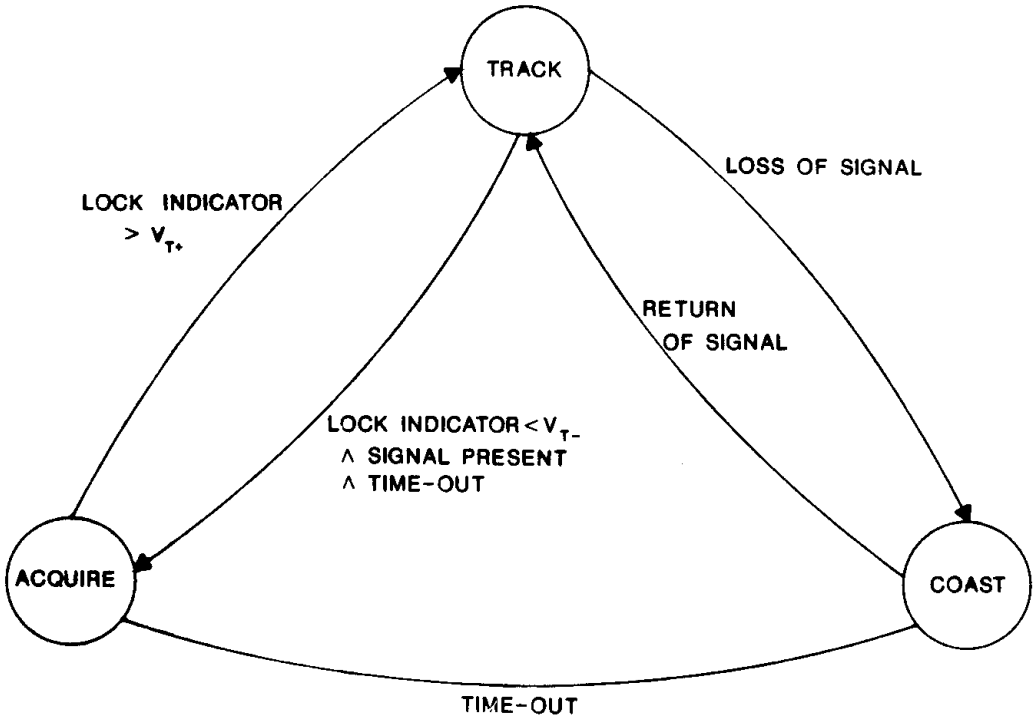


FIGURE 4. INFLUENCES OF NONCOHERENT AGC ON THE LOCK INDICATOR LEVEL.

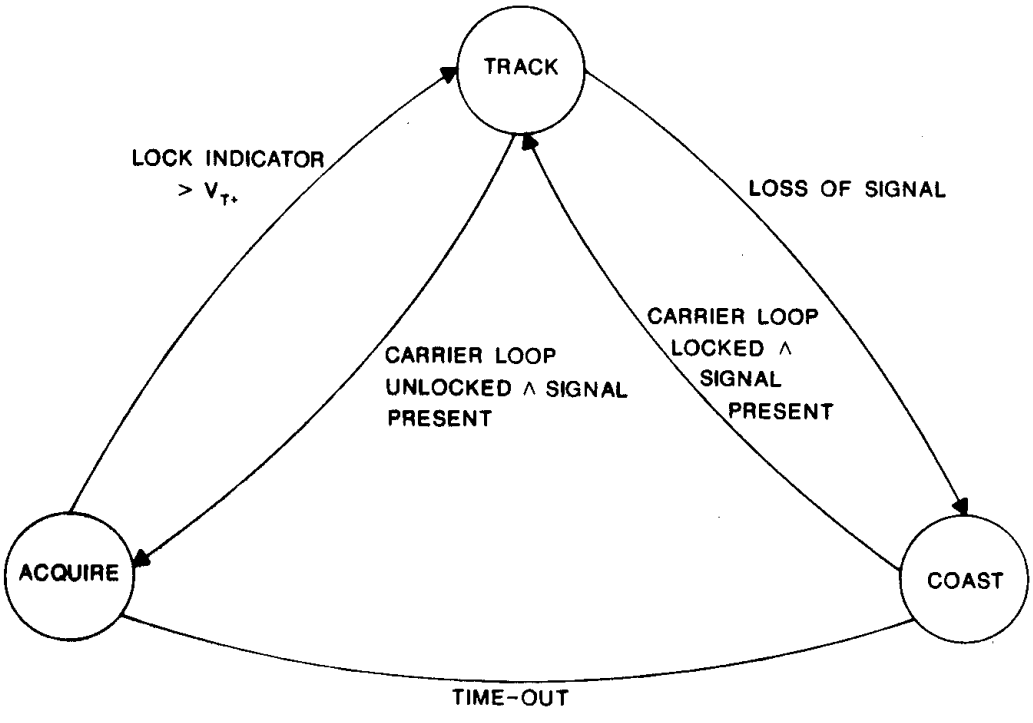
State Machine Controller

In this system, the state machine (or program) has access to all pertinent system parameters, allowing the PLL operation to be controlled accordingly. For example, using information from the lock detector, the carrier and bit clock loop bandwidths can be adjusted to provide rapid acquisition while preserving loop performance during tracking operation. That is, by switching loop coefficients the filter can be made to have a large bandwidth during acquisition and a narrow bandwith during tracking. Furthermore, the AGC error signal and lock indicator level can be used to evaluate signal quality which can then be used to control the carrier and bit clock loop operation during periods of signal fades.

Each PLL operates in one of three independent modes: acquisition, tracking, or coasting. The PLL is initially in the acquisition mode until phase lock has occurred. At this point, the PLL enters the tracking mode. The loop will remain in this mode provided that there is sufficient input signal and the loop remains locked. The loop will reenter acquisition if the lock indicator drops below threshold. However, if the input signal drops below a specified level, the controller will force the loop into a “coast” mode in which the loop is opened. Once the signal is restored, the PLL resumes tracking. If the signal is absent for an excessive period of time, the loop is forced back to the acquisition mode. The state machine diagrams for the carrier and bit clock loops are shown in Figure 5 a and b. Two



(A)



(b)

FIGURE 5. STATE DIAGRAMS, (a) CARRIER LOOP, (b) SIT CLOCK LOOP.

separate diagrams are required for the carrier and bit timing loops due to the dependence of the bit clock loop on the carrier loop.

The acquisition state is responsible for initially acquiring the frequency and phase of the input signal, thereby bringing the loop into a locked condition. This can be accomplished by using either self or aided acquisition methods. The selection of a particular technique is based on the system requirements (SNR, frequency uncertainty, allowable acquisition time, etc.). In self acquisition, the loop is simply enabled and allowed to acquire the frequency and phase of the input. Although simple, this process can be slow and unreliable. Aided acquisition techniques such as frequency sweeping (7), bandwidth widening, and frequency discrimination (8) can be used to assist the loop during acquisition.

Frequency sweeping is used when the initial frequency uncertainty is greater than the pull-in bandwidth of the loop. For a type II phase-locked loop the pull-in range is infinite. However, the pull-in time is inversely proportional to the bandwidth cubed (2). For this loop, a constant offset, proportional to the desired sweep rate, is fed directly into the integrator of the loop filter. The VCO is driven by a ramp, causing the frequency to sweep across the band, effectively searching for the input signal. This technique acquires faster than the self-acquisition method. However, the sweep should be disabled once the loop has achieved lock to reduce the steady state phase error and prevent the frequency estimate from drifting during periods of fading or outages. The lock indicator will determine when to disable the sweep function. The sweep rate should be slow enough to allow the loop to lock to the input signal. From Gardner (2), the maximum sweep rate is given by

$$\Delta\dot{\omega} = \frac{1}{2}\,\omega_n^2\left[1 - 2\left(\mathrm{SNR}_L\right)^{-\frac{1}{2}}\right] \tag{18}$$

where SNR_L is the signal-to-noise ratio of loop.

Bandwidth widening uses different loop filters for the acquisition and tracking functions. During acquisition, a large loop bandwidth is used to rapidly acquire the input signal. However, the larger the loop bandwidth, the more sensitive it is to noise and the larger the steady state phase error. Therefore, once lock is detected, the gains of the loop filter are adjusted to realize the narrow-band loop required for accurate phase tracking. Switching occurs when the lock indicator exceeds a pre-determined threshold. Figure 6 shows the instantaneous phase error for the multiple bandwidth PLL for a bandwidth ratio of 10. The wide and narrow bandwidth PLLs are plotted for comparison. Observation of the individual curves reveals that the hybrid loop acquires at a rate comparable to that of the

wide-band loop while maintaining a steady-state phase error equal to that of the narrow-band loop.

Note, however, that if the bandwidth ratio is too large or the loop is switched too soon, the loop may stall or slip, thereby prolonging acquisition. This phenomenon is shown in Figure 7 where the loop coefficients were switched prior to the loop filter integrator reaching steady-state. If the loop is switched prior to this point, the narrow-band loop may not be within its lock-in range. For this reason, a type I loop is less sensitive to bandwidth changes. Simulations show that bandwidth changes on the order of 100 are practical (as opposed to 20 for the type II loop).

Instead of switching bandwidths instantaneously, it is possible to make a gradual transition from the acquisition to the tracking filter. Moreover, this makes the selection of the lock indicator threshold less critical. As might be expected, the rate and method (e.g., linearly) of coefficient adjustment greatly influence acquisition. Further investigation is necessary to determine the rate and method for adjusting loop coefficients as function of system parameters (i.e., SNR, frequency offset and rate of change).

Excess periods of fading (or loss of signal) can result in loss of lock. Two separate phenomena occur at low signal-to-noise ratios (SNR), “cycle slipping” and “drop-lock” (2). Cycle slipping and drop-lock degrade the operation of the bit clock loop. Slipping one or more cycles of the bit clock loop is catastrophic when error correction and detection coding or data encryption is employed. If the influence of the carrier loop on the bit clock loop is neglected, cycle slips in the carrier will introduce isolated (local) errors in the vicinity of the signal fade. However, the carrier loop will tend to drift away from the acquired frequency causing the reacquisition process to be prolonged when the signal returns. The overall impact is to amplify the effects of the signal outage. To avoid this problem, the carrier and bit clock loops can be opened and allowed to “coast” through the fade. Once the AGC indicates the return of the signal, the loops are closed and allowed to resume tracking. Figures 8 and 9 illustrate the advantage of coasting through the signal outage for the carrier loop.

Coasting of the bit clock loop can be sustained for extended periods of time, generally on the order of seconds, because the frequency uncertainty is small. Under these circumstances, phase coherence of the bit clock can be maintained throughout the fade. On the other hand, maintaining the correct phase of the carrier loop is impractical due to the system dynamics associated with the carrier frequency. Since the bit clock loop is generally coupled to the carrier loop, it is necessary to ensure that the carrier loop has reacquired before returning to the tracking mode.

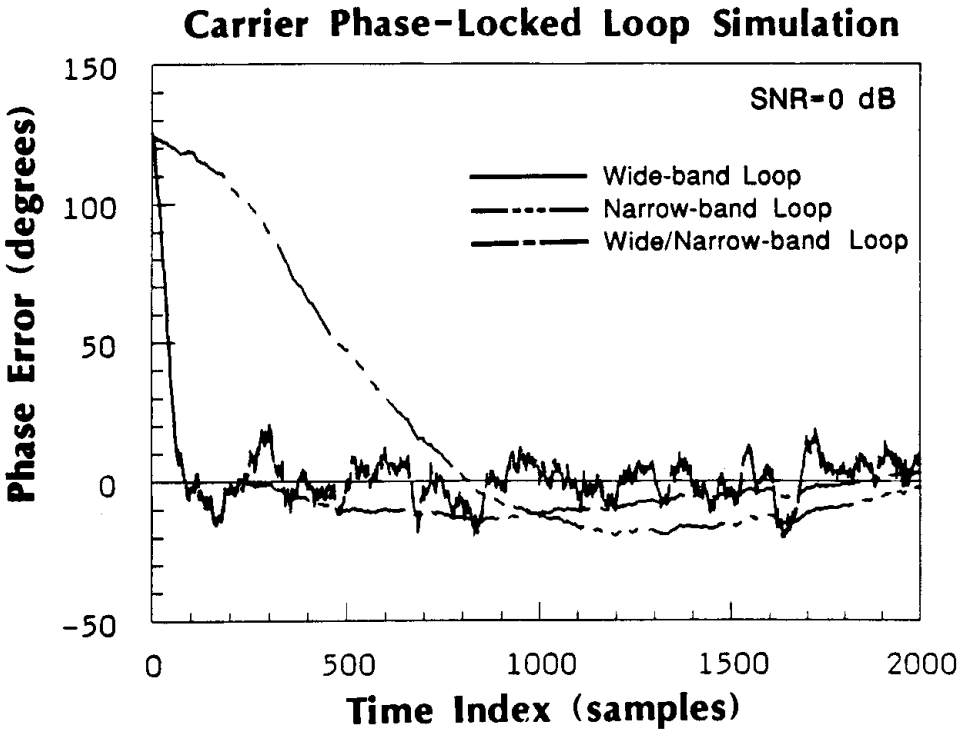


FIGURE 6. MULTIPLE BANDWIDTH LOOP SIMULATION.

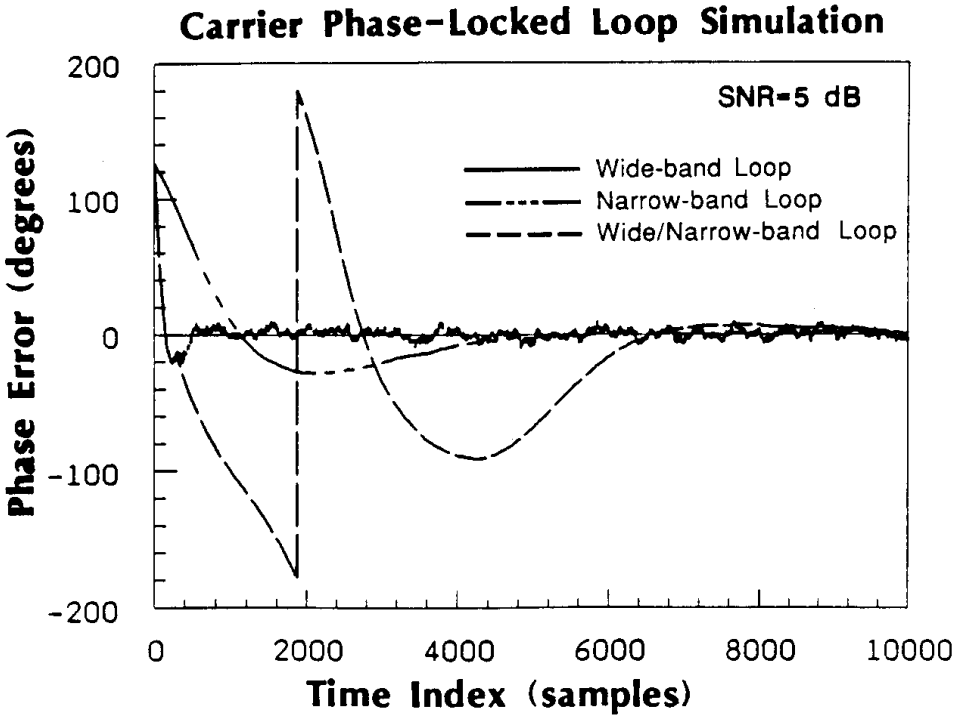


FIGURE 7. CYCLE SLIPPING PHENOMENON IN THE MULTIPLE BANDWIDTH LOOP SIMULATION.

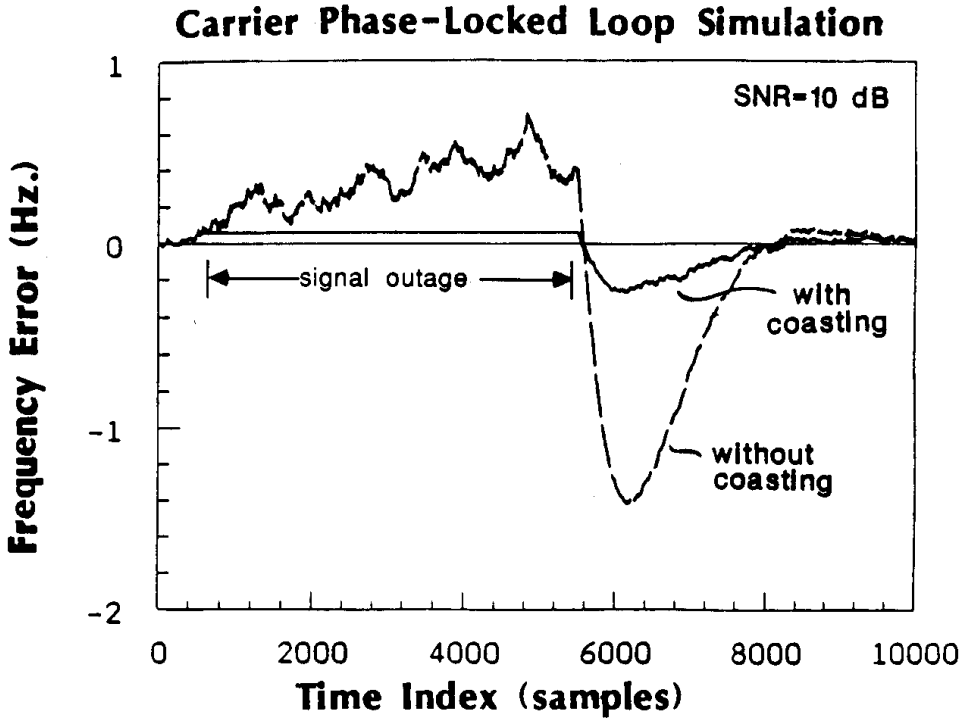


FIGURE 8. COASTING OF THE CARRIER LOOP (FREQUENCY ERROR).

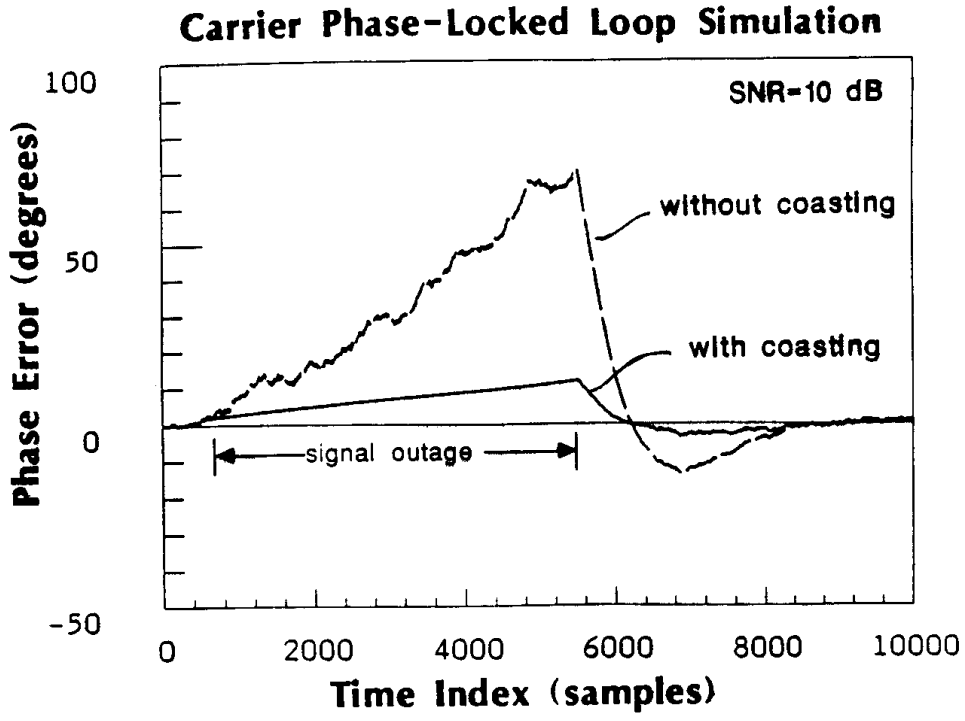


FIGURE 9. COASTING OF THE CARRIER LOOP (PHASE ERROR).

In practice, there exists a delay between the signal outage and recognition of loss of signal. As a result, the loops can be frozen with incorrect system states. To alleviate this problem, delayed loop state variables (i.e., frequency and phase) can be saved such that when loss of signal is detected, the loop is updated with these values. The delayed variables must extend beyond the lag time of the outage detector. Only retention of the frequency state variable of the carrier loop is practical due to the system dynamics.

If the response time of the outage detector is long, it is possible that the bit clock loop may have already slipped a cycle. For this case it is necessary to use a second VCO which shadows (lags) the bit clock loop VCO. Thus, when an outage is detected, the shadow VCO phase is updated at the nominal rate until the carrier loop has regained phase lock. Note that the shadow VCO is used for bit extraction.

CONCLUSION

In conclusion, the system design of an intelligent PLL with integral AGC, signal quality and lock detection was presented. By exploiting information from the AGC, lock detector and signal quality it is possible to realize a PLL with improved performance over its conventional counterpart. The design issues were discussed for a typical communication receiver employing both a carrier and bit clock PLL.

The system was shown, through simulations, to exhibit marked improvement in the areas of acquisition/tracking and signal outage in comparison to the conventional loop. However, the method and implementation are application dependent. Moreover, there remain several areas which require further study. In particular, the allowable bandwidth ratios and rate of change need to be quantified in terms of system parameters by analytical methods. Selection of the thresholds were chosen empirically for the simulations shown. A more rigorous approach to threshold selection is needed.

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