Digitized Doppler Signal Processor

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ABSTRACT

At the present time there is a requirement for developing an airborne approach for processing radar doppler video data into digital PCM format compatible with current IRIG standards. Techniques for digitizing the doppler video presently exist, but have limitations due to the fact that the data is processed and represented in the time domain. These limitations can be mainly attributed to the high bit rates required for quantizing the dynamic nature of the doppler signal. Therefore, an alternate approach was selected by which the video doppler data is converted and represented in the frequency domain. The time to frequency domain conversion is accomplished with a digital Part Fourier Transform (FFT) implemented in conjunction with a quadrature translator. This method will provide a means by which the doppler signal can be represented as a quasi-static spectrum. The advantage in this application is that only the spectral data which contains relevant engineering information will be processed. The resultant system will thereby minimize the transmission bit rate and maximize the dynamic range for the purpose of signal analysis. The paper will describe the implementation and work performed on the digitized doppler signal processor along with the potential application in PCM systems requiring spectral signal analysis.

INTRODUCTION

The doppler signal processor is being developed in response to a DoD mandate to securing video doppler. The project has been in development for approximately one and half years with the goal of providing a system that is capable of digitizing video doppler in the frequency domain. It is important to note that the quality of the doppler data must not be comprised by the system. The intention is to improve over the current resolution that are being obtained, since the system will eliminate sources of distortion caused via the channel and recording interfaces. All doppler processing will be performed in flight thereby reducing the time and effort required by the analyst. The processed doppler data can then be interrogated for flight performance information and miss-distance calculation.

At this time the doppler signal processor is being evaluated by doppler analysts. The analysts have addressed some limitations within the doppler signal processor that requires attention. These limitation are due mainly to system noise and the weighting coefficients. Different weighting functions are being evaluated for determining which one provides the best trade off between bin spreading and signal detection. The test set-up involves the doppler signal processor interfaced to a high speed tape recorder and a oscillograph line scanner. The tape recorder is used for reproducing actual flight data with the line scanner yielding the hard copy output. This hard copy data represents the doppler data in a frequency verses time format which is then compared to actual data derived from an analyst. The points of interest in the comparison are signal distinctness and the ability to determine doppler resolution, especially at the end-game, or point of interception.

DISCUSSION OF THE PROBLEM

Currently there is a growing requirement to encrypt telemetry signals for new system designs, as well as refurbished versions of existing designs. There continues to be a major requirement to encrypt the traditional doppler processor output signal as part of the single data link. The demand for encryption will become greater in the future as DoD programs become more sensitive.

Currently the goal of telemetry systems is to telemeter via a single PCM link. This PCM link encodes all of the analog signals that need to be observed including the doppler information. The encoder converts the analog data into a structured digital format. The resultant digital format can contain a large amount data representing the values of the sensors being measured. The amount of data within the format is directly proportional to the number of channels being measured, the frequency response of the channels, and word resolution.

The main problem in the past has been that the digitizing of the doppler signal would require a large amount of bandwidth to transmit over an RF link. For a digitized 200KHz doppler signal the minimum bit rate required would be 8MHz, assuming an 8 bit word resolution with 5 samples per Hertz of the input.

DISCUSSION OF THE PROPOSED SOLUTION

The problem remains that the doppler signal must still be digitized since the goal is to interface the resultant data to an encryptor. Therefore a technique of data reduction is necessary. The data reduction must be sufficient to be compatible with other telemetry systems such that the total bandwidth is within the limits of standard encryptors and transmitters. The reduction method must also maintain the doppler signal fidelity and minimize any distortion caused by the conversion and processing of the digitized data.

The doppler signal by definition is generally a single set of frequencies representing a frequency shift. This frequency shift represents the combined relative velocities of three different vectors. The first velocity vector being the source that is illuminating the target, the target being the second velocity vector. The final velocity vector is the missile itself which will mix the doppler shifted frequencies from the two sources (illuminating source and target) and end lip with a combined doppler signal. This resultant doppler signal now represents a function of the closing velocity of the missile to the target relative to the illuminating source.

A solution to the problem of transmitting the doppler signal digitally employs a FFT technique. This FFT technique is an algorithm that will convert a time domain signal to a frequency domain representation. In other words the FFT algorithm will perform a spectrum analysis of the doppler signal. This frequency domain signal will now represent the doppler signal as a semi-static group of frequencies instead of a complex and dynamic signal requiring a large bandwidth to transmit. The technique of FFT signal processing will enable both doppler data reduction and facilitate in doppler roll-off calculation.

The advantages of a digital approach is the implied airborne data reduction and virtual error free data transmission with a lower bandwidth contribution. Data reduction will also reduce ground station miss distance calculation error since the received data can be optimally processed by a personal computer. The output from the computer will be a print out of the doppler roll-off and calculated miss distance. The digital approach also allows for considerable flexibility in system to system design and software changes. Additionally, digital designs allow for greater environmental stress in terms of operating temperature, shock, and vibration without changing the circuit behavior.

THEORY OF OPERATION

The specific application of the doppler signal processor is to provide a means of digitally representing video doppler with minimum bandwidth. In order to digitally encode video doppler there must first be some assumptions made on the characteristics of this data. The first premise is that the doppler analyst does not require the full spectral details on the video doppler. The spectral region of interest lies in-between the main clutter return and target doppler. This region of interest represents a bandwidth of approximately 64KHz. The other premises are the spectral resolutions which incorporate two interdependent variables, bin bandwidth, and time. Bin bandwidth will define the individual frequency components that can be resolved. The time variable is the period for which it takes one discrete FFT to be completed, in other words the minimum time resolution. This means that every millisecond there is one spectral output. The determination for this time resolution is derived from the fact that the system hardware can process a 256 point FFT in a little under 1ms.

Tieing all of the above requirements together along with some relationships that exist between discrete time and frequency domains, the following system parameters can be equated. The first relationship to observe is that of the sampling rate T and sampling window period t_p (refer to figure 1)[1].

$$T = \frac{1}{f_s}$$

$$t_p = \frac{1}{F}$$

Where f_s is the frequency domain span (64KHz) and F the bin frequency bandwidth. Since the doppler signal processor is a discrete system the following equations can be used where N is the number of discrete points (256).

$$t_p = NT$$

$$f_s = NF$$

Recombining the above equations will yield a set of equalities which relate the time domain sampling rates to the frequency domain resolution.

$$T = \frac{1}{NF}$$

$$t_p = \frac{N}{f_s}$$

Therefore substituting in the known quantities the sampling window rate for one discrete FFT will be 4ms which will also define the bin frequency bandwidth to be 256HZ. This will further produce the sampling rate required for the system which is equal to 64KS/s.

There remains the problem that the system hardware is capable of generating a 256 point spectrum at 1ms intervals, but according to the system constraints an FFT will require 4ms to collect the samples. A solution to this problem would be to collect samples for four FFT's each being staggered by 1ms (refer to figure 2). The depiction represents a circular buffer that models the data storage and processing tasks. The buffer will in effect turn counter clockwise in 16us increments. This will in effect produce a 75% sampling overlap. Thereby producing a system capable of analyzing a 64KHz regions of doppler with 256Hz and 1ms resolution. Note that the sampling rate is increased by four times (256KS/s), thereby separating neighboring samples by 4us with successive samples within the buffer separated by 16us.

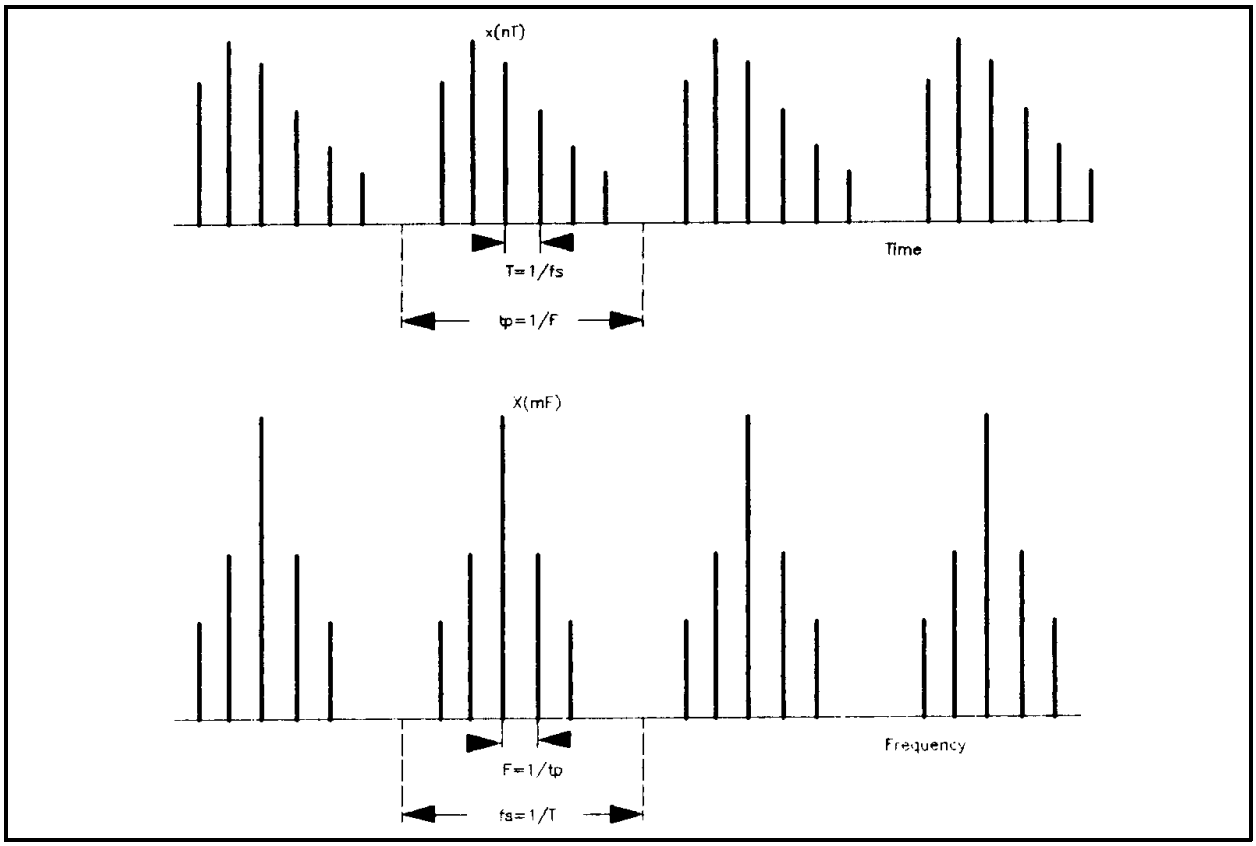

Figure 1. Depiction of the relationship between discrete time and frequency

ANALOG PROCESSING

The video doppler will first be translated to the proper frequency range with a pair of analog multipliers. These multipliers will generate two pairs of harmonics corresponding at:

$$f_{doppler} + f_{stno} \text{ and } f_{doppler} - f_{stno}$$

$$f_{doppler} + f_{costno} \text{ and } f_{doppler} - f_{costno}$$

A pair of matched eighth order elliptic filters will provide a 32KHz cut-off frequency for all of the generated harmonics. Therefore only frequency elements below 32KHz will continue to be processed, and for all intents and purpose the first set equations will have no contribution since under normal circumstance these components are above the 32KHz cut-off. Note that frequencies below the carrier (sine and cosine) will produce a positive frequency and those above a negative result. This indicates a phase reversal on the negative frequency components, in other words the sine and cosine effectively switch multipliers which becomes sine and cosine. In the positive frequency domain the sine will lead the cosine components where as in the negative domain the cosine will lead the sine component. This will become an important factor within the FFT algorithm. The effect can be viewed as if the 0Hz reference is moved by the frequency carrier offset (refer to figure 3). The processor will subsequently perform the FFT algorithm between +32KHz from the frequency offset.

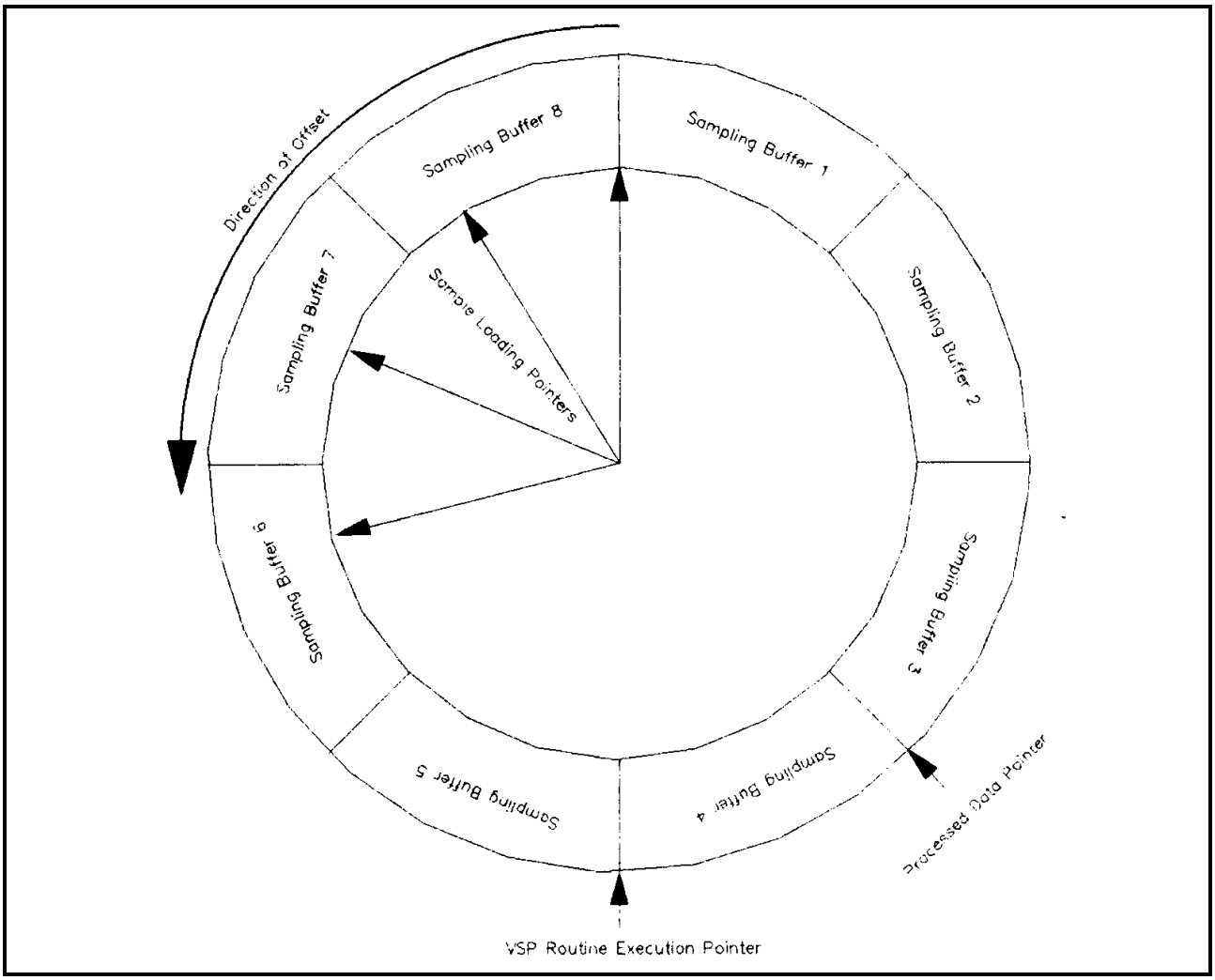

Figure 2. Depiction of the sampling buffer strategy

The sine, cosine generator is a implemented with a numerically controlled oscillator (NCO). These oscillators can switch frequencies on the order of 2us and have frequency range from 0 to 20MHz with better then 1Hz resolution. The NCO operates by counting phase increments and outputs the corresponding trigonometric coefficient. An NCO will in effect adjust the step size (360°/x) in older to determine the frequency, sampling a set sine wave at various intervals. The only drawback is the there are spurious components generated (-55dbc) which might or might not effect the working frequency domain, any spurious components outside the domain are filtered.

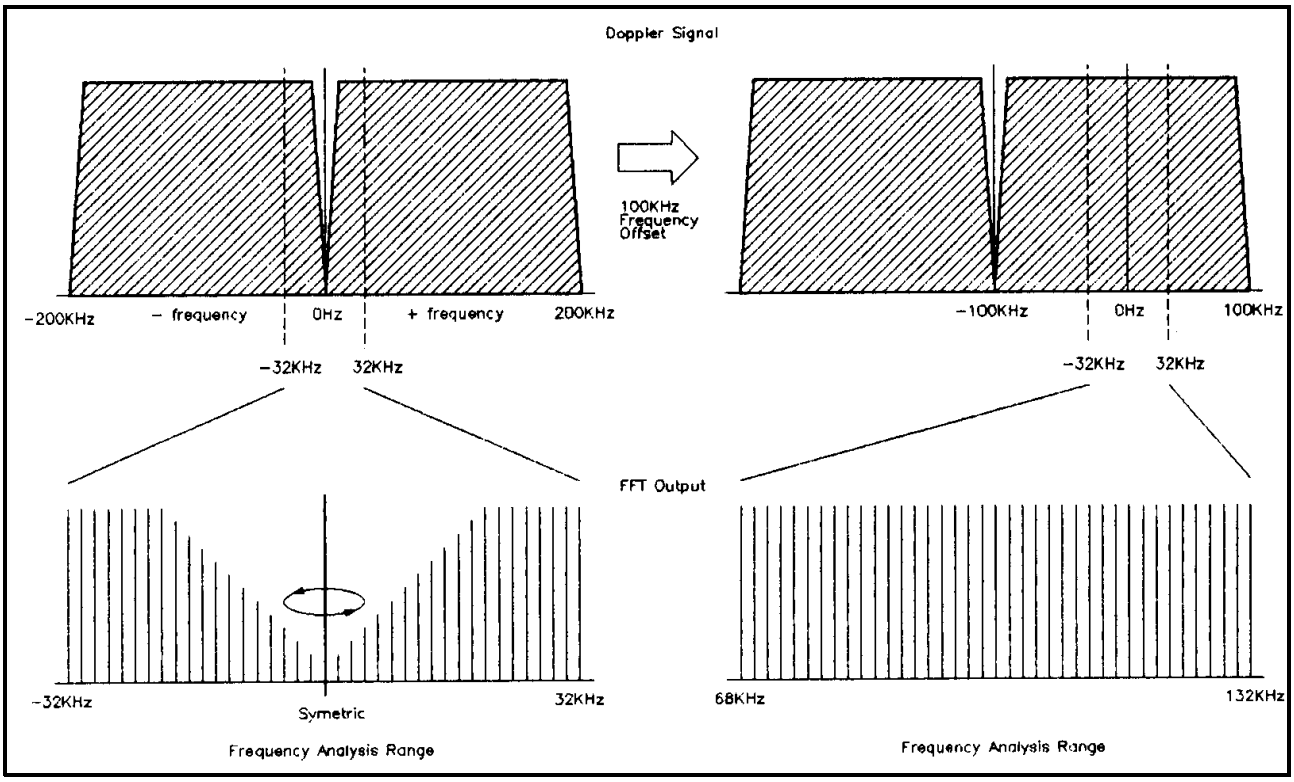

Figure 3. Depiction of the quadrature translation of the doppler signal

The two A/D converters are synchronously sampling the processed video doppler at 256KS/s 4us), four times the frequency window spectrum. The converters will in effect be creating complex (real and imaginary) numbers for the processors. Four time oversampling is provided because of the time resolution required for the doppler signal processor, which is 1ms. In order to collect 256 complex data points at 64KS/s would take 4ms. The oversampling of the doppler data will also in effect sample overlap, which will prevent sudden changes in the frequency spectrum.

DIGITAL PROCESSING

The doppler signal processor is implemented around two signal processors (refer to figure 4), DSP (Digital Signal Processor), and a VSP (Vector Signal Processor). Each processor is responsible for a different set of operations. These operations are defined by the data processing requirements on the system, which are data collection, domain translation, compression, and formatting.

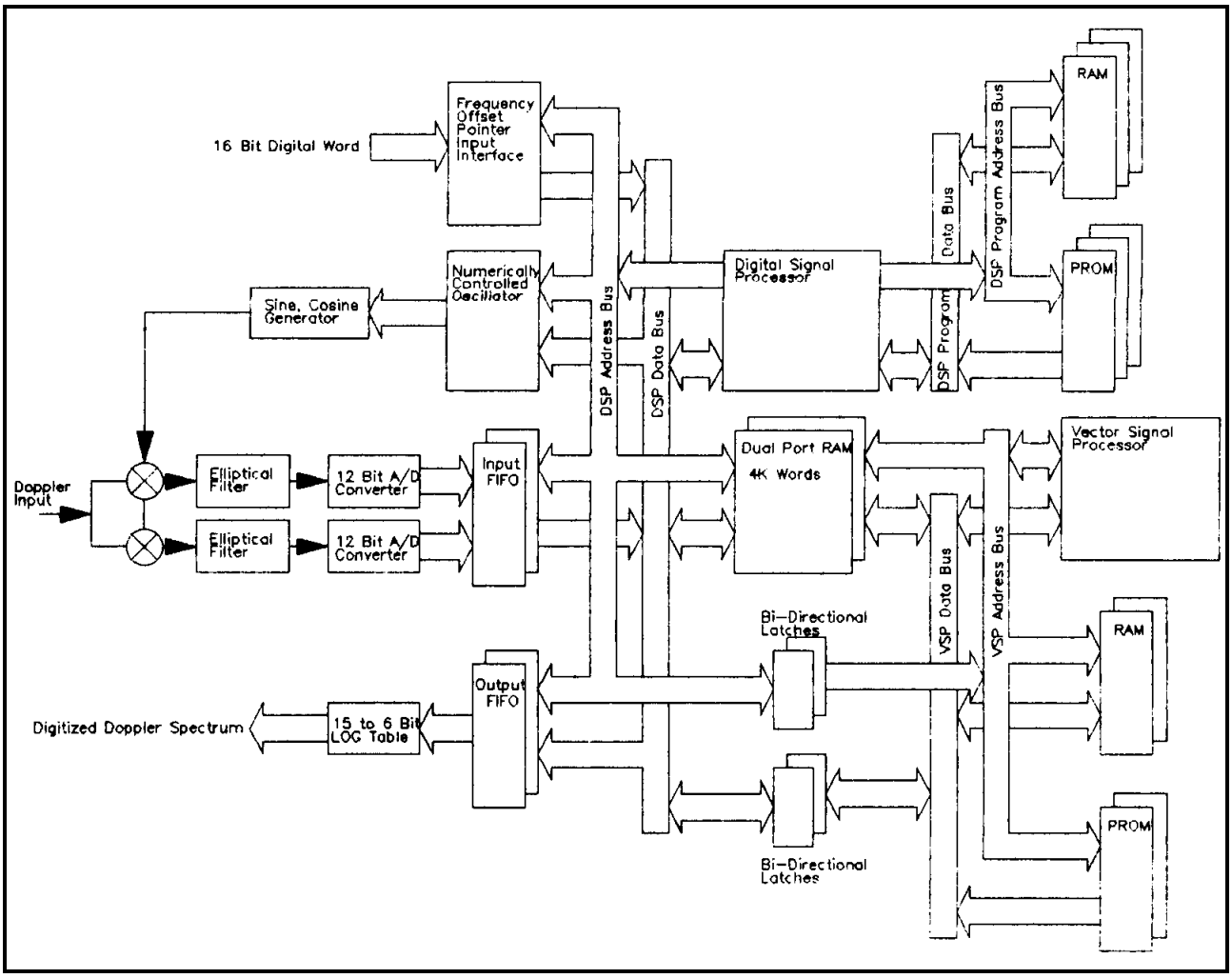

Figure 4. Block diagram of the Doppler Signal Processor

The digital signal processor is a commercially available device operating at 50MHz. The function of the digital signal processor is for the manipulation of the pre-processed and post-processed FFT data by transferring, compressing, and formatting. Since the vector signal processor is occupied, converting data via the FFT algorithm, another processor is required for the post-processing. The VSP also requires a host processor for initiating program execution by writing to an internal register. A standard microprocessor or microcontroller will be too slow in this application since the bus speeds are only around 3us. The DSP on the other hand have bus speeds on the order of 80ns, approximately 30 times quicker. Another important facet of the DSP is the separate data and program bus which facilitate multiple data manipulations on a single instruction word.

The pre-processing aspects of the system entails weighting [2] the incoming digitized data and placing the data in the proper sampling buffer. Weighting, also known as windowing, the incoming data is intended for the reduction of calculation leakage, a phenomena which occurs in discrete signal processing. The leakage has the effect of spreading the spectrum

when the input signal frequency components are not integer multiples of the bin frequencies. Bin frequencies being separated by 256Hz in this system. The sampling buffers in the doppler signal processor are employed for the temporary storage of data and subsequent FFT execution. The windowed data is placed in one of eight separate sampling buffers in memory. The sampling buffers are implemented with dual port RAM which facilitate both the DSP and VSP access without the need to interfere on to the processor bus.

The post-processing phase is responsible for transferring the resultant FFT data to the output FIFO's (first in, first out memories). The output data is then converted from a 15 bit to a 6 bit data word via a logarithmic table stored in programmable read only memory (PROM). This method of compressing the data will maintain the dynamic range of the signal without losing any spectral information. The goal is to determine the presence of a signal in the doppler frequency domain, not necessarily the absolute energy in that signal component.

The vector signal processor is the subsystem responsible for converting the real-time doppler data into a frequency spectrum, better know as a discrete FFT. On the current implementation of the system a discrete commercial multipurpose processor is used for providing the FFT function and magnitude calculations. The vector signal processor functions by being loaded with 256 complex vectors every millisecond. The vector is defined as a complex number, with real and imaginary components. The resultant output is a 256 point magnitude spectrum which is completed before the next set of complex vectors are loaded. All FFT and magnitude processing functions are controlled via software and reside on the vector signal processor bus.

SOFTWARE

The software for the system is divided into the two signal processors each executing specific tasks. The VSP executes primarily the discrete FFT and magnitude algorithms. Whereas the DSP controls mainly system operations and data manipulation between the various interfaces.

The VSP software actually contains eight separate FFT with magnitude routines stored in PROM. Each routine will process one of the eight sampling buffers. For example, the first routine will process solely sampling buffer 1. By using this method there is no processing time devoted to figuring out buffer addressing sequence. The DSP will initiate software executions by writing the start address of the routine into the VSP instruction base register. The program will first execute a 256 point discrete FFT using a Cooley-Tukey algorithm [3] followed by a magnitude calculation on the resultant vectors. The magnitude calculation is performed via a vector rotation algorithm. This is where a vector is

successively modulated by a 45°, 22.5°, and 11.25° phase. The real axis of the vector will now contain the projected magnitude of that vector with a maximum possible error of 1.9%. The, total time required to perform a routine is 980us.

The DSP is the principal controller for the doppler signal processor yet currently remains idle most of the time. The software is interrupt driven, the interrupts occurring at 1ms intervals with the software taking 250us to complete. The software initialization consists of generating a windowing coefficient table within the DSP program RAM and setting-up the sampling buffer address pointers. The coefficient table is structured in a manner that allows the DSP to sequentially multiply the digitized input doppler data and place the result in the sampling buffers. The interrupt flag is activated when the input FIFO indicates half-full status, 256 vectors, which occupies 512 words. At which point the DSP will now execute a set software modules. The first is to initiate the VSP with the address pointer of the previously filled sampling buffer. Next is the removal of the 256 vectors in the input FIFO which are then windowed and placed in the appropriate sampling buffer. The final two tasks are placing the completed FFT results, 256 words, into the output FIFO and up-dating the NCO frequency output. At the end of these tasks the DSP will run an infinite loop, suspended until the succeeding interrupt.

APPLICATIONS

The candidate application for the doppler signal processor is a system design for digitizing all of the provided analog TM signals on the Standard Missile Program. The problem being that of updating the existing standard missile TM systems for future requirements, specifically encryption. The existing TM system is a DKT-61 which is currently configured as a PCM and FM-FM system. The purposed design for the doppler signal processor will be to replace the FM-FM analog system with a full digitized system. The digitized system will remain compatible with existing bandwidth allocations, mechanics, and data measurement specifications.

Other Applications include the addition of extra NCO’s which can then provide multiple spectral analysis on a signal. Each sampling buffer will be assigned a different frequency domain to process. Thereby allowing doppler tracking on more then one target.

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3. J. W. Cooley and J. W. Tukey, *An Algorithm for the Machine Calculation of Complex Fourier Series* Math. Computation, Vol. 19, 1965.