ANALYSIS OF AN ADAPTIVE SEQUENTIAL PROBABILITY RATIO TEST TYPE OF PCM FRAME SYNCHRONIZER

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ABSTRACT

A simple adaptive algorithm is employed in the determination of operating parameters for a sequential probability ratio test (SPRT) type of PCM frame synchronizer. Performance data over a wide range of bit error rates are obtained by computer simulation. These data show a significant improvement in lock-to-search transition performance of the SPRT over the so-called conventional type of synchronizer.

INTRODUCTION

One recurrent problem in data communications is that of timing or synchronization at the receive end. For the case of a serial bit stream three types of timing are generally important:

1) bit synchronization (reconstructing a master clock)
2) word synchronization (properly dividing bit groups into words)
3) frame synchronization (grouping words into the proper relative format).

Obviously, bit synchronization must be the first timing acquisition since all other events occur at some sub-mulitple of the bit rate. After a bit clock is derived then word and frame timing acquisition can be attempted. For many data communications systems the orientation of words within each frame is constant so that word timing and identification are functions only of frame timing. To establish this framing function a unique and constant bit pattern is inserted into the data stream once per frame. Once proper frame synchronization is established then all subsequent timing and data manipulation follows directly from the a priori knowledge of the frame structure. Therefore, the system performance depends on the ability to find the frame synchronization pattern after the bit clock has been regenerated.

Much work has been done, and continues to be done, on the research of optimal bit synchronization. However, the state-of-the-art in communications equipment today allows for the assumption that the bit synchronizers operate sufficiently well in a dynamic environment so that the effects of imperfect bit timing will not be considered in the study of optimal frame synchronization. In other words, in a dynamic environment, the bit synchronizer is expected to provide an accurate bit clock in conditions that are otherwise too poor to allow frame synchronization or any utilization of the data. Supporting evidence for this assumption can be found in emperical results, as in Nichols and Cox [1].

This paper concentrates on the optimallity of frame synchronization of a serial bit stream in a data communications system. For all practical systems this data is subject to corruption by noise in the transmission medium. Characterization of this noise and of the corresponding errors in the data depends heavily on the nature of the particular transmission medium in use. However, many systems are accurately modeled by the data stream corrupted by additive white gaussian noise and corresponding bit errors which are independent and identically distributed. This is most often assumed in radio transmission systems and will be assumed for this analysis. The problem then becomes two-fold:

1) finding the frame synchronization pattern in the serial bit stream, subjected to some bit error probability p, when initially out of sync
2) determining the loss of synchronization when initially in sync.

Another assumption that is helpful in defining the problem is that the bit stream is random at loss of synchronization. This assumption is made on intuitive grounds since most high efficiency communications systems tending to minimize bandwidth would also maximize the entropy of the bit stream. For analysis this condition is equivalent to subjecting the data to a bit error probability of one-half (p =0.5).

The previous statements of system characteristics and assumptions allow the consideration of optimallity in frame synchronization. In the first case where the system is initially out of sync, defined as the Search mode, a procedure which minimizes the expected acquisition time can be considered as optimal. This notion is compatible with high efficiency communications, where the value of the information transferred by each word is high. In the second case where the system is currently in sync, defined as the Lock mode, a procedure which minimizes the expected time to return to Search after loss of synchronization can be considered optimal. Since the Search-to-Lock procedure must be executed after a loss of sync it follows that minimizing the return to Search time also minimizes the loss of information. Unfortunately, the optimization of these two procedures is somewhat contradictory since minimizing the Search-to-Lock time tends to increase the probability of incorrectly identifying a random pattern as the correct one. Conversely, minimizing the Lock-to-Search time tends to increase the probability of not

identifying a true synchronization pattern when it is present. With these concepts of optimallity and the identification of some of the important statistical elements of the problem some review of previous work in this field will be valuable.

BACKGROUND

Before going further two definitions will be helpful.

$\alpha \equiv$ probability of accepting an incorrect pattern

$\beta \equiv$ probability of rejecting a correct pattern

Much of the present commercial equipment providing frame synchronization functions perform statistical tests on groups of candidate sync patterns. To pass from Search-to-Lock these “conventional” synchronizers require that the candidate pattern correlate with the correct pattern to a certain degree, say within x bit errors, for a certain number, say y, of consecutive frames. Thus, for a given bit error probability optimum values of x and y can be evaluated relative to the constraints of α and β. Here it is seen that α and β must be selected to satisfy the operational requirements of the communications system.

Rather than looking at this as a pattern sequential identification problem Van de Houten [2] proposed an improved approach of bit sequential testing based on the idea of the Sequential Probability Ratio Test(SPRT) treated by Wald [3]. If α is set equal to β then Van de Houten finds that the SPRT relationship is

$$-L < \Sigma I - K\Sigma J < L \qquad (1)$$

where

$\Sigma I \equiv$ the number of correct bits in a test of n samples (bits)

$\Sigma J \equiv$ the number of error bits in a test of n samples (bits)

$K \equiv$ the weighting factor for the error bits

$L \equiv$ the decision threshold.

The interpretation of the relation in (1) is as follows. Each bit of the candidate pattern is tested in sequence as it arrives. If the received bit agrees with the corresponding bit of the correct pattern then the ΣI sum is incremented, but if it disagrees then the ΣJ sum is incremented. The term $\Sigma I - K\Sigma J$ is evaluated after every bit is received. If this amount is

equal to or greater than L then the Lock mode criterion has been met, but if this amount is equal to or less than $-L$ then the Search mode criterion has been met. If this amount is between $-L$ and L , that is if the relationship in (1) is true, then there is no decision made at that time and the test continues with the next bit in sequence. It can be seen that this procedure most often results in partial pattern testing which has some advantage, at least intuitively, over the integral pattern testing of the conventional method. Van de Houten derives the expressions for the parameters, K and L , which are

$$K = \frac{-\ln 2p}{\ln 2(1-p)} \tag{2}$$

$$L = \frac{\ln \frac{1-\alpha}{\beta}}{\ln 2(1-p)} \tag{3}$$

A modification to this procedure which fixes the test interval to integral pattern samples was done by Straehley [4]. Although the performance is sub-optimum in an analytical sense to Van de Houten's method, it does have some value for practical implementations. Also of value is Straehley's comparison to the performance of an optimized conventional procedure. With this previous work sited a continuation to the analysis of a statistical frame synchronizer with adaptive decision parameters is in order.

METHOD DEVELOPMENT

The major factor which kept Van de Houten and Straehley from realizing a truly optimal synchronization method was the inability of the synchronizer to match the decision parameters to the operating environment. As can be seen from (2) and (3), the values of K and L are a function of α, β, and p . As mentioned before, α and β are selected to satisfy certain data requirements of the system. For this analysis they will be considered equal and fixed. Due to the dynamic environment, however, a priori knowledge of the bit error probability, p, is not available. To circumvent this obsticle both authors selected a fixed value for p and evaluated K and L from (2) and (3). Obviously, for any other value of bit error probability the fixed decision parameters would be mismatched. By selecting the worst-case environment, that is the maximum p, the statistical properties of the SPRT yields a much lower mismatch for the Search-to-Lock process than for the Lock-to-Search process. This is very fortunate since any out-of-Lock condition inhibits the estimation of the present value of p . Once in Lock, though, an estimate of the bit error probability can be made and the decision parameters can be adapted to improve the Lock-to-Search process.

When in Lock an estimate of p is made every frame by averaging the current measurement with the estimate from the previous frame. In a simple recursive expression it is given as

$$p_{k+1} = \frac{1}{2}\left(\frac{x_k}{N} + p_k\right) \tag{4}$$

where

x_k ≡ the number of bit errors in frame k

N ≡ the number of bits in the frame sync pattern.

After frame k the values of K and L are adapted by using (2) and (3) with p_{k+1}. Since (4) produces an estimate of the bit error probability which converges in the limit to the mean of x/N it will converge to actual value of p. Consequently, the adapted values of K and L will converge to the optimum values matched to the actual environment. This adaptive process significantly improves the Lock-to-Search time over the fixed p methods.

ANALYSIS AND RESULTS

At this point the analysis should begin with a formal definition of the synchronizer performance. Two performance measures must be used since the Search-to-Lock process cannot be adaptive while the Lock-to-Search process can be.

The Search-to-Lock Process: Synchronizer operation, when initially in the Search mode, attempts to find a pattern in the serial bit stream which has a high correlation with the correct pattern. It is known that the bit timing is correct, but the data quality in terms of bit error probability is unknown. To execute the SPRT some initial values of K and L must be chosen requiring an assumption of the initial fixed bit error probability, p_o. An engineering decision must be made here since any arbitrary p_o will incur different penalties at the two environmental extremes. If p_o is set high then α, the probability of accepting an incorrect pattern, increases over the desired value for low bit error probabilities. Conversely, if p_o is set low then β, the probability of rejecting a correct pattern, increases over the desired value for high bit error probabilities. The value of p_o=0.21, second highest in the bit error probability data set, was used for this analysis on the assumption that resynchronization is often required on radio links when the transmission is recovering from a deep fade. In this case the initial bit error probability is expected to be high thus minimizing the effects of sub-optimal decision parameters.

The performance measure of the synchronizer in this mode is defined as the expected number of bits required to go from Search to Lock. Thus,

$$P_{S \to L} \equiv E(N)_{S \to L} \tag{5}$$

$$= \sum_{n=1}^{\infty} n \Pr\{\Sigma I - K\Sigma J < L \text{ in } n-1 \text{ bits}\} \Pr\{\Sigma I - K\Sigma J \geq L \text{ in } n \text{ bits}\} \tag{6}$$

A theoretical optimum for $P_{S \to L}$ can be found for any static environment by using the K and L values matched to the actual p. This optimum $P_{S \to L}$ provides a baseline of performance by which the actual perforance can be measured in terms of misadjustment. The definition of misadjustment used in this analysis is the difference between actual performance and optimal performance normalized to the optimum. Thus,

$$M_{S \to L} \equiv \frac{P_{S \to L|\text{actual}} - P_{S \to L|\text{opt}}}{P_{S \to L|\text{opt}}} \tag{7}$$

The evaluation of $P_{S \to L}$ by (6) directly is extremely difficult for the general case. The SPRT is sensitive to the sequential order of correct bits and error bits so the set of allowable sequences satisfying the conditions of (6) is a subset of all combinations of sequences of length n. Determining which of these combinations are the proper ones is a tedious task. An alternate approach was taken for this analysis in which the Search-to-Lock SPRT process, flow charted in Figure 1, was simulated and the number of bits needed to obtain Lock for each trial was averaged over 2000 trials. The results of this simulation are given in Table 1 which includes the bit error probability data set, corresponding K and L values, optimal $P_{S \to L}$, actual $P_{S \to L}$, and $M_{S \to L}$. Note that since the Search-to-Lock process is not adaptive the misadjustment depends only on the actual bit error probability and not on the trial number.

The Lock-to-Search Process: After entering the Lock mode the synchronizer operation stays in that state until changes in the environmental conditions warrent a return to Search. At this time a loss of synchronization occurs and the serial bit stream becomes a sequence of bits which have equal probability of being a “one” or a “zero”. When correlating this bit stream with the correct pattern the synchronizer operates with an effective bit error probability of one-half. The synchronizer must detect this condition as soon as possible and return to Search thereafter to minimize the out-of-sync time. The performance of the SPRT for this Lock-to-Search process is measured as the expected number of bits needed to revert from the Lock mode to the Search mode. Thus,

$$P_{L \to S} \equiv E(N)_{L \to S} \tag{8}$$

$$= \sum_{n=1}^{\infty} n \Pr\{\Sigma I - K\Sigma J > -L \text{ in } n-1 \text{ bits}\} \Pr\{\Sigma I - K\Sigma J \leq -L \text{ in } n \text{ bits}\} \quad (9)$$

Synchronizer operation in the Lock mode provides a means by which the bit error probability can be estimated. Since the correct pattern is known and its correlation with the incoming pattern determines which received bits are in error then an estimate of p for that frame can be made by dividing the number of errors, x , by the number of bits in the sync pattern, N . This value is averaged with the previous averaged estimate, according to (4), and that result is used in (2) and (3) to get new values of K and L. Beginning with some initial condition, p_o, the value of p_{k+1} will converge in the limit to the mean of x/N , which is the true bit error probability. It follows that as the estimate of the bit error probability converges to the true p the calculated values of K and L will approach their optimum values. A flow chart of this adaptive Lock-to-Search SPRT process is given in Figure 2.

The misadjustment for the Lock-to-Search process is similar to that in (7) with the addition of the adaptive iteration index. Thus,

$$(M_{L\to s})_k \equiv \frac{(P_{L\to s|\text{adap}})_k - P_{L\to s|\text{opt}}}{P_{s\to L|\text{opt}}} \quad (10)$$

Here $(P_{L\to S|\text{adap}})_k$ is evaluated as in (9) with the values of K and L calculated using p_k. This definition produces a misadjustment measure based on the expected value of the bit error probability estimate for each iteration. A computer simulation was employed to find the optimum performance values for the same bit error probabilities given in Table 1, and these are shown in Figure 3 along with a fitted curve. Figure 4 shows the misadustment for various bit error probabilities versus the iteration index. These curves were derived from Figure 3 and the expected value of p_k from (4). As a final analysis the performances of the adaptive and fixed parameter Lock-to-Search SPRT processes were compared. The improvement factor, defined as the normalized reduction of the performance measure, $P_{L\to S}$, is given in Table 2 for each bit error probability. Here,

$$I_{L\to s} \equiv \frac{P_{L\to s|\text{fixed}} - P_{L\to s|\text{adap}}}{P_{L\to s|\text{adap}}} \quad (11)$$

where $(P_{L\to S|\text{adap}})$ is taken as the value after convergence.

CONCLUSIONS

The purpose of this research was to analyze the performance of an adaptive frame synchronizer operating on a serial bit stream with errors. The Sequential Probability Ratio Test was used to determine the synchronization status with the adaptive algorithm tending to optimize the decision parameters while in the Lock mode. Results of this analysis are given in Table 2 for bit error probability values ranging from 10^{-6} to 0.25. Improvement is seen for all bit error probabilities below 0.21, the non-adaptive value, as expected. The steepness of the misadlustment curves shown in Figure 4 indicates that the adaptive algorithm is expected to perform well and convergence to the optimum should occur, on the average, in less than twenty iterations for the range of bit error probabilities of interest.

As a matter of completeness the SPRT synchronizer operation in the Search mode (non-adaptive) was analyzed and the results given in Table 1. Selecting a worst-case operating environment of p=0.21 yielded acceptable results if frame synchronization patterns in excess of sixteen bits in length are employed.

The results of this analysis are quite general and can be interpreted for lumped or distributed frame synchronization pattern groupings. The performance overall is very good with the improvements made by the adaptive process being excellent.

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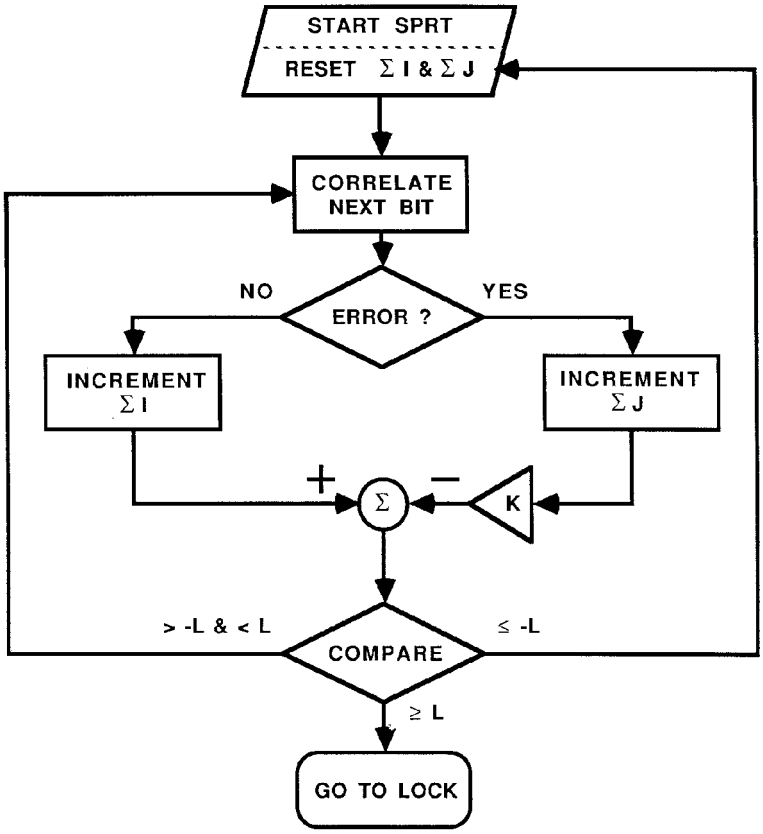

Figure 1 - Search-to-Lock SPRT Flow Chart.

TABLE I
Search-to-Lock SPIRT parameters, performance measures, and misadjustment values.

Bit Error Probability	K	L	Performance		Misadjustment
			Optimal	Actual	
0.000001	13.3	18.9	14.0	21.0	0.50
0.00001	13.3	15.6	14.0	21.0	0.50
0.0001	13.3	12.3	14.0	21.0	0.50
0.0008	13.3	9.3	14.1	21.1	0.50
0.006	13.4	6.4	14.6	21.4	0.47
0.02	13.7	4.8	15.8	22.3	0.41
0.06	14.6	3.4	20.3	25.0	0.23
0.10	15.7	2.7	26.0	29.1	0.12
0.17	18.2	2.1	39.8	40.5	0.02
0.21	20.1	1.9	53.0	53.0	0.00
0.25	22.7	1.7	72.3	74.7	0.03

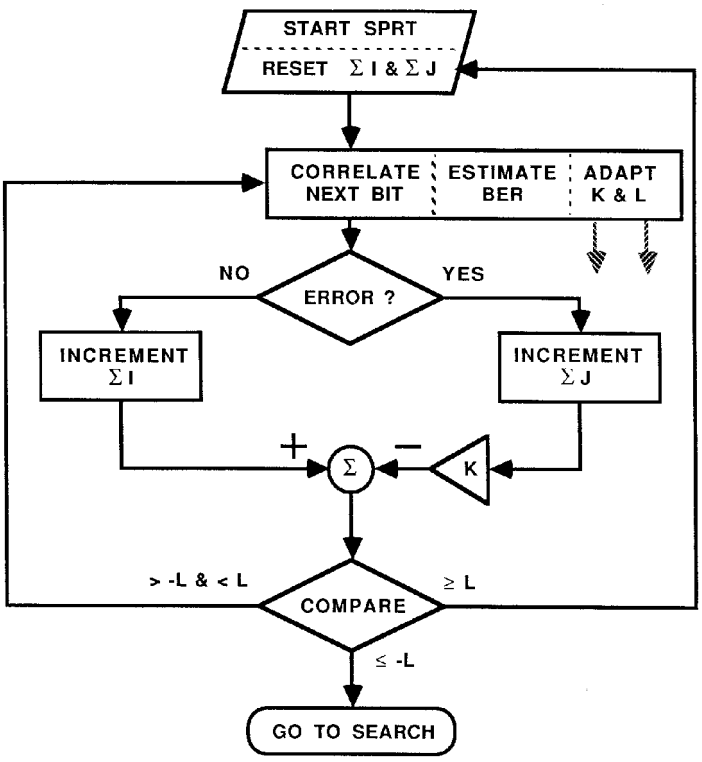

Figure 2 - Adaptive Lock-to-Search SPRT Flow Chart.

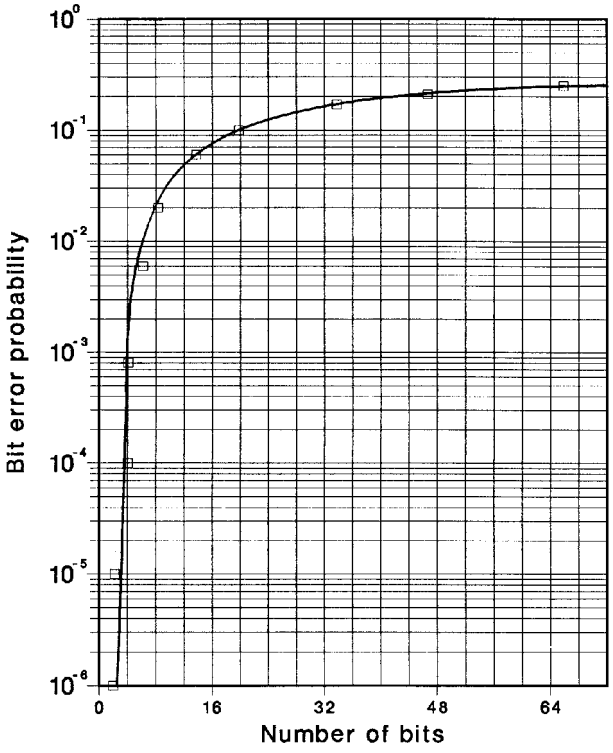

Figure 3 - Optimum Lock-to-Search SPRT Performance

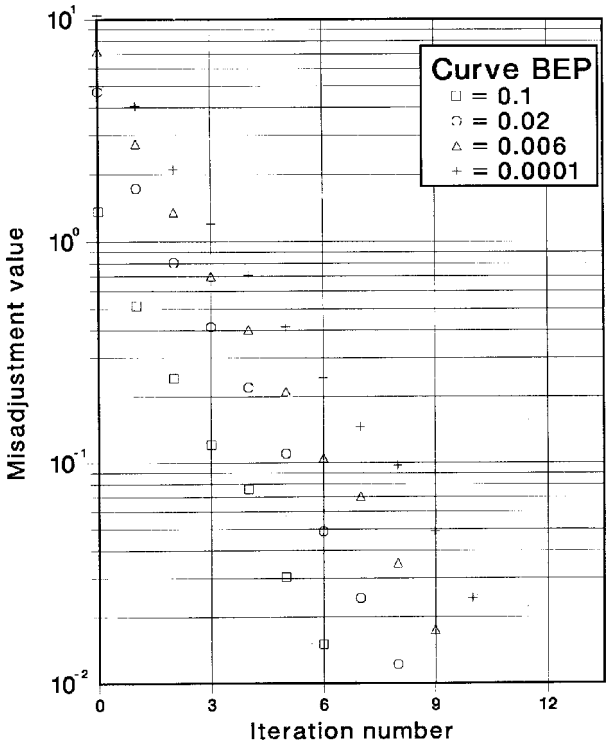

Figure 4 - Lock-to-Search Misadjustment for adaptive SPRT

TABLE II
Lock-to-Search SPRT performance measures and improvement factors.

Bit Error Probability	Performance		Improvement Factor
	Fixed	Adaptive	
0.000001	46.7	2.00	22.4
0.00001	46.7	2.30	19.3
0.0001	46.7	4.10	10.4
0.0008	46.7	4.10	10.4
0.006	46.7	6.20	6.50
0.02	46.7	8.30	4.60
0.06	46.7	13.7	2.40
0.10	46.7	19.8	1.40
0.17	46.7	33.8	0.38
0.21	46.7	46.7	0.00
0.25	46.7	65.9	-0.29