THE REAL-TIME TELEMETRY PROCESSING SYSTEM III

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ABSTRACT

The Navy's Real-time Telemetry Processing System (RTPS III) is a third generation system. Designed and built by Computer Sciences Corporation (CSC), RTPS III will support the demands of the Navy flight test community well into the 1990's. The RTPS III is custom-crafted using CSC's system development methodology which blends the best features of the current Navy RTPS system and previously proven CSC systems.

A major objective of CSC's RTPS III design is the continuation of existing Navy user interfaces. The transition from the existing system to the integrated RTPS III has also been facilitated by the incorporation of common interfaces to Navy applications software, thus ensuring "new system" acceptance. RTPS III is designed to include a powerful front-end capable of Engineering Unit conversions at more than 200,000 samples per second (sps) per telemetry stream with expansion to 500,000 sps. It will include networking concepts which allow the simple addition of additional subsystems should expansion be required. RTPS III also supports both secure and integrated modes of operation for classified and unclassified processing.

The CSC design, a custom combination of proven and new development, results in a Navy system which meets tomorrow's flight test requirements today. Other benefits to NATC are a modular, cost-effective solution with lower life-cycle costs, and a broader range of possibilities for evolving and reconfiguring the system to service new applications and users.

Key Words

Telemetry
Real-Time
Graphics
Naval Air Test Center (NATC)
Flight Test

INTRODUCTION

RTPS III, based upon proven concepts and already accepted user interfaces, represents an inexpensive and low-risk, evolutionary system growth pattern.

RTPS I and II were developed during the 1970's and have supported over 15,000 flight test operations on both fixed wing and rotary wing aircraft. RTPS has been an effective system and an essential part of the way tests are conducted at the Naval Air Test Center (NATC) at Patuxent River, Maryland. Prior to the development of the RTPS III specification, the Navy developed an RTPS III prototype. This prototype allowed the Navy to validate design concepts and performance requirements for RTPS III, as well as reducing the potential costs associated with its development. RTPS III retains all of the functionality and the best of the existing heavily utilized operational features of RTPS I and II, and the RTPS III prototype.

The system architecture of RTPS III is based upon a proven Navy system architecture. Its capability has been extended by CSC using proven hardware and software techniques from telemetry systems now supporting the most sophisticated levels of flight testing. The CSC design includes the integration of Navy and CSC software, blended to take full advantage of engineering investments already established in the Navy prototype as well as CSC developed systems. The result is RTPS III, an economical yet proven design, with a high probability of being accepted by the user community.

THE RTPS III ARCHITECTURE

The RTPS III architecture includes 5 identical streams and a file system. The file system consists of a pair of identically configured processors, and is connected to each stream through a high-speed serial network. As shown in Figure 1, each stram consists of three processors connected by a high-speed Shared Memory Subsystem. The SMS, a custom CSC design used successfully on other projects, has an on-board memory cycle time of 150ns to allow rapid asynchronous retrieval of critical telemetry data by each of the three stream processors.

The SMS is the heart of the stream, being fed by the telemetry front-end over three interfaces onto a separate memory bus with a rated capacity of 4 megawords per second. The SMS makes current data available to the Data Channel Preprocessor, the Display Host Processor, and the Applications Processor within the stream. All intra-stream communication occurs during CSC's interprocessor communications software which accesses the SMS and queues external interrupts. This software provides for the transfer of messages between processors, as well as activation/termination of tasks in one stream processor by another.

THE STREAM

The initial RTPS III delivery consists of two separate and identical streams. The expansion to additional streams is easily acccomplished because each stream is connected as an additional network node.

Each stream is comprised of the following subsystems:

The Telemetry Decoding Subsystem (TDS)

The TDS, shown in Figure 2, represents a hardware front-end design which will accept up to four 10 Mbit PCM wavetrains and a multiplexed FM input. It has been enhanced with the use of a bus-oriented, modular PCM front-end. A bit-slice processor in the TDS performs hardware EU conversions and limit checks at rates of 120,000 sps per processor card. The system will be delivered with two processor cards with expansion for three additional cards should rates beyond 240K sps per stream be required.

Several new features have been added to the TDS to support special Navy requirements. A separate card has been added to allow the user to perform several types of minor-frame data quality checks in the front-end hardware, thus freeing up the host CPU to perform more critical functions. Another card has been developed to allow the front-end hardware to buffer up specific configurations of measurement data in two modes for use by the host. In sequential mode, the card may be used to archive or log data on mass storage devices such as disks or magnetic tapes. In the external mode of operation, the card can be used to create two-dimensional current value buffers with historical “depth” in the host computer memory. These array buffers include a selectable number of samples of a unique measurement that can be used by a software program to drive array processors or other special analysis routines. The card may also generate group arrays which are selectable groups of measurements in memory rather than a single measurement. Each RTPS III stream contains two of these cards. one is used for generating current value tables with depth, and the other for recording engineering data directly to high-speed digital tape.

The TDS is a true 32 bit front-end, which also supports rapid format changes. A parallel interface is used for the real-time transfer of entirely new wavetrain acquisition synchronization and processing parameters. Word time slots are used for preempting data during different phases of support. Decom lists may be preloaded, preassigned, and automatically changed when a precursor on the wavetrain identifies the phase.

Data Channel Preprocessor (DCP)

The DCP, shown in Figure 3, is a general purpose processor, dedicated to the acquisition tasks within RTPS III. It is responsible for the management and organization of data such that EU converted information may be limit checked, reprocessed, and output to EU tape and strip chart recorders. CSC's software design allows standard EU conversions to be performed in high-speed front-end hardware. However, should the user desire more sophisticated EU conversion algorithms, they may be performed in the acquisition software of the DCP.

Measurement limit checking may be performed using hardware and/or software techniques. The front-end hardware supports a variety of programmable limit checks. In addition, two classes of limit checking are provided within the Data Channel Processor: Measurement Limit Checking and Conditional Limit Checking. Standard measurement limit checking is available in the DCP on those measurements not limit checked in the front-end. These measurements may include those requiring special EU conversions in the DCP, or derived measurements transferred back through shared memory following processing by a user's analysis software in the Applications Processor. Conditional limit checking in the DCP allows the user to automate the data evaluation process by specifying multiple sets of measurement conditions as a single limit. The measurement is limit checked, and the results stored and maintained in shared memory for use by the display or applications processors.

As mentioned previously, the DCP provides high-speed EU tape recording at 160 Kwords per second. The DCP also utilizes a CSC designed and developed strip chart interface. Without CPU intervention, this device is capable of driving strip chart recorders at an aggregate rate of 512,000 samples per second, or 128 strip chart recorder pens at 4,000 samples per second each. The unit extracts either raw or EU data from the stream shared memory and performs the appropriate DAC scaling and number conversions. The EU data output includes special EU converted and derived EU measurements from the DCP and Applications Processor Subsystem (APS), respectively. Stripchart channels and functions are assigned by the user in setup mode from the Display Host Processor.

Display Host Processor (DHP)

The DHP, shown in Figure 4, is connected to other stream processors through the high-speed Shared Memory Subsystem. The DHP supports specialized data output on color and monochrome graphics devices within the Project Engineer Station (PES). Critical Measurement Displays, located above the PES consoles, provide alphanumeric readouts on user-selected critical measurements at all times during an operation. Eight strip chart recorders are also contained within the PES control room to allow instantaneous viewing

and hardcopy recording of 64 separate measurements. Each SCR is housed in a slope front console, designed by CSC to allow easy data evaluation and annotation by project engineers.

The RTPS III PES user-interface is designed to be identical to the prototype system. Functionally, however, two features have been added to extend the usefulness of the station during real-time operations. The first is the display data recall function. Recall provides the ability to record plot set data in real-time, which the PES operator may recall in “instant replay” fashion during the operation. Historical data for all planned plots are recorded on disk during the operation whether or not they are currently being viewed. These data are indexed by time so that they may be recalled for subsequent viewing or processing. Additional recall measurements may be added or accessed by specifying a measurement name, or a measurement group. Eighty million data samples may be saved in a “wrap” file at rates up to 50,000 samples per second. Simultaneous recording and recall is supported. The recall data are also available to both the Display Host Processor and Applications Processor for special user analysis.

The second custom feature within the PES is a “no-freeze” hardcopy for the 23" monochrome and 19" color displays. Each 23" monochrome PES display will have a dedicated hardcopy engine, custom-designed by CSC. Upon PES operator request, the hardcopy engine will capture each image to be printed without interruption to the screen. It will output the image to a laser printer capable of supporting a resolution of 300 points per inch and a speed of six hardcopies per minute. Four megabytes of memory will be dedicated to the buffering of display images to allow reasonable storage for “high-activity” periods. This entire operation is entirely transparent to the user and requires no resources from the display controller or the Display Host Processor.

The 19" color display hardcopy will only utilize off-the-shelf hardware components. Redundant controllers and CSC developed disk spooling software allow a hardcopy to be generated without slowing down, stopping or otherwise disrupting the display screen presentation.

Applications Processor Subsystem

The Applications Processor Subsystem (APS), shown in Figure 5, includes the Applications Processor and interfaces to the Shared Memory Subsystem and an array processor to support the user’s project specific processing. Utilizing a dedicated machine for this purpose alleviates normal problems associated with user/system software conflicts and resource contention.

In addition to the SMS, physical access is also provided through a network data link from the APS to the File System. These two interfaces are controlled by CSC-developed application interface software. This software receives requests from application software to retrieve telemetry measurements and associated parameters from the DCP for processing, and provides results through the Shared Memory Subsystem to the Data Channel Preprocessor and Display Host Processor. The APS also provides the path between the File System Processors and other stream subsystems for transfer of instrumentation files, user setup files, and stream initialization and termination control.

THE FILE SYSTEM

The File System is shown in Figure 6. It is dedicated to the Telemetry Engineer Station (TES) activities, as well as appliction program development at individual user terminals. The File System is composed of two identical processors, network interfaces, shared memory and dual-ported disks. Each File System processor operates using identical software to process and control the file system and TES functions. This architecture allows a single file system processor to perform file system functions in the event of failure of the alternate processor. Shared memory is used to provide interprocessor communications, failure monitoring and semaphoring to maintain system integrity.

The TES console contains remote controls and status displays for each of the five streams of the Final RTPS III configuration. Color monitors (15") are utilized to allow simple menu entry of set-up data in a fashion consistent with that familiar to NATC TES operators. The TES also contains a Front End Status Display which allows any operator to independently select and monitor time and status information from any stream.

The File System consists of the File System Processor (FSP) , the disk resident system files, and the File System Services (FSS) to support the system files. The system files and their support services are designed to be processor independent; thus the identical software provides these support services on both the FSP and Applications Processor Subsystem of a stream when the stream is operated in the secure or standalone mode.

The stream interface between the File System Processors and all RTPS III streams is provided by the network hardware and software. A CSC-designed switch is included on each stream to physically disconnect the stream from the FPS when necessary.

SYSTEM OPERATION

RTPS III is controlled by Telemetry Engineers and Project Engineers. The system is designed so that each of the user interfaces is the same, regardless of whether they are running in Integrated or Secure modes of operation.

The RTPS III system has been designed to maintain an operational mode consistent with the prototype RTPS. Engineers will find minimal differences in controlling and monitoring an operation using RTPS III or the prototype. The differences are due to the blending of enhanced capabilities rather than changes to current techniques. One of the major capabilities added is the independent File System control of multiple streams. The system may now be configured in an integrated mode, in which the File System remains connected to the stream, as well as in a secure mode, in which the File System is disconnected. Once disconnected, the File System and TES functions are accomplished at the Applications Processor Subsystem (APS).

SUMMARY

CSC's own proven software designs, based upon a proven Navy user interface, provide a low-cost and low-risk design approach for the Naval Air Test Center. CSC software places particular emphasis on TM acquisition processing, compiler data base architecture, high-speed data recording, and data recall. A hierarchical software design allows the RTPS III user to process real-time EU algorithms in real-time acquisition software, and special user analysis software in either the Applications or Display Processors. As NATC flight test personnel apply these more sophisticated flight test techniques in real-time, they should experience a reduction in the cost of each flight test with this third generation of their Real-time Processing System.

CSC's software and hardware architecture for RTPS III represents a low-risk, third generation real time telemetry system, which has grown from proven concepts from previous Navy and CSC developed systems. The system includes features which promote reconfigurability, and system growth for new applications. These features include hardware and software commonality across all stream and file system processors, common user interfaces, and a distributed architecture which eliminates obvious throughput bottlenecks.

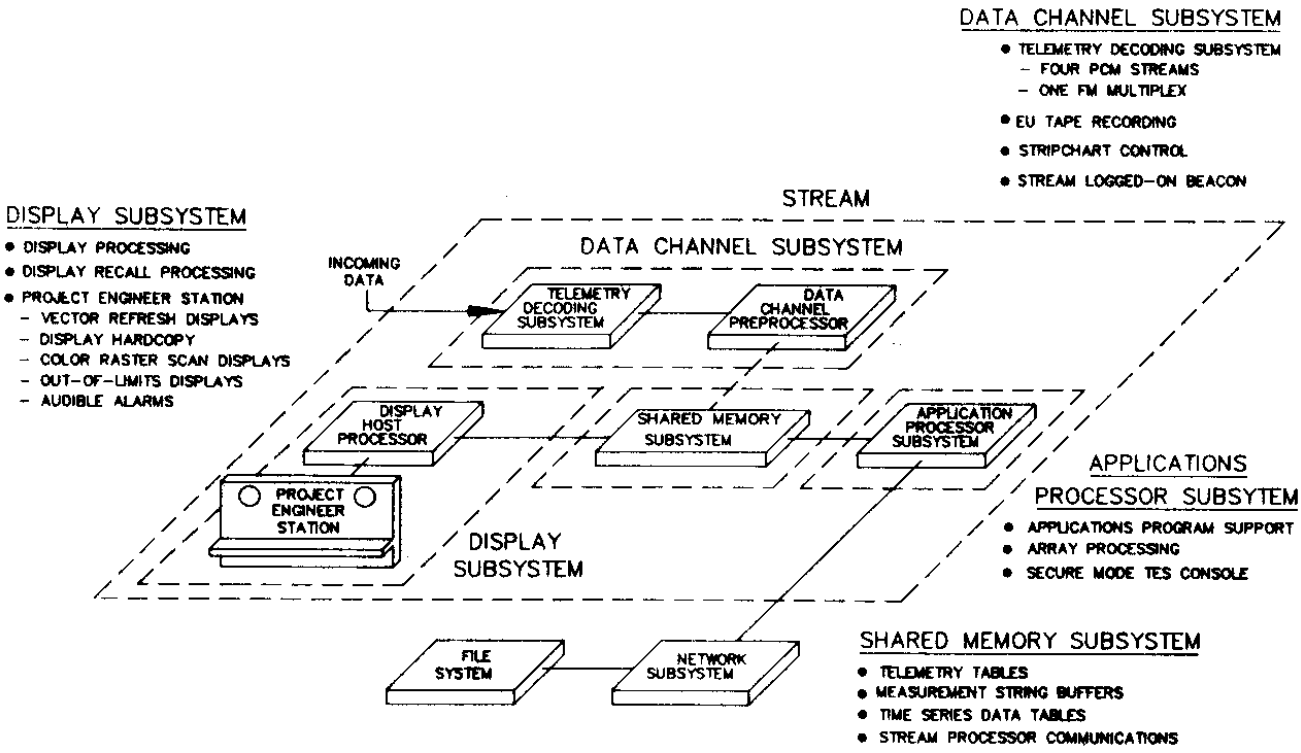

Figure 1. RTPS III System Architecture (After Reference 1)

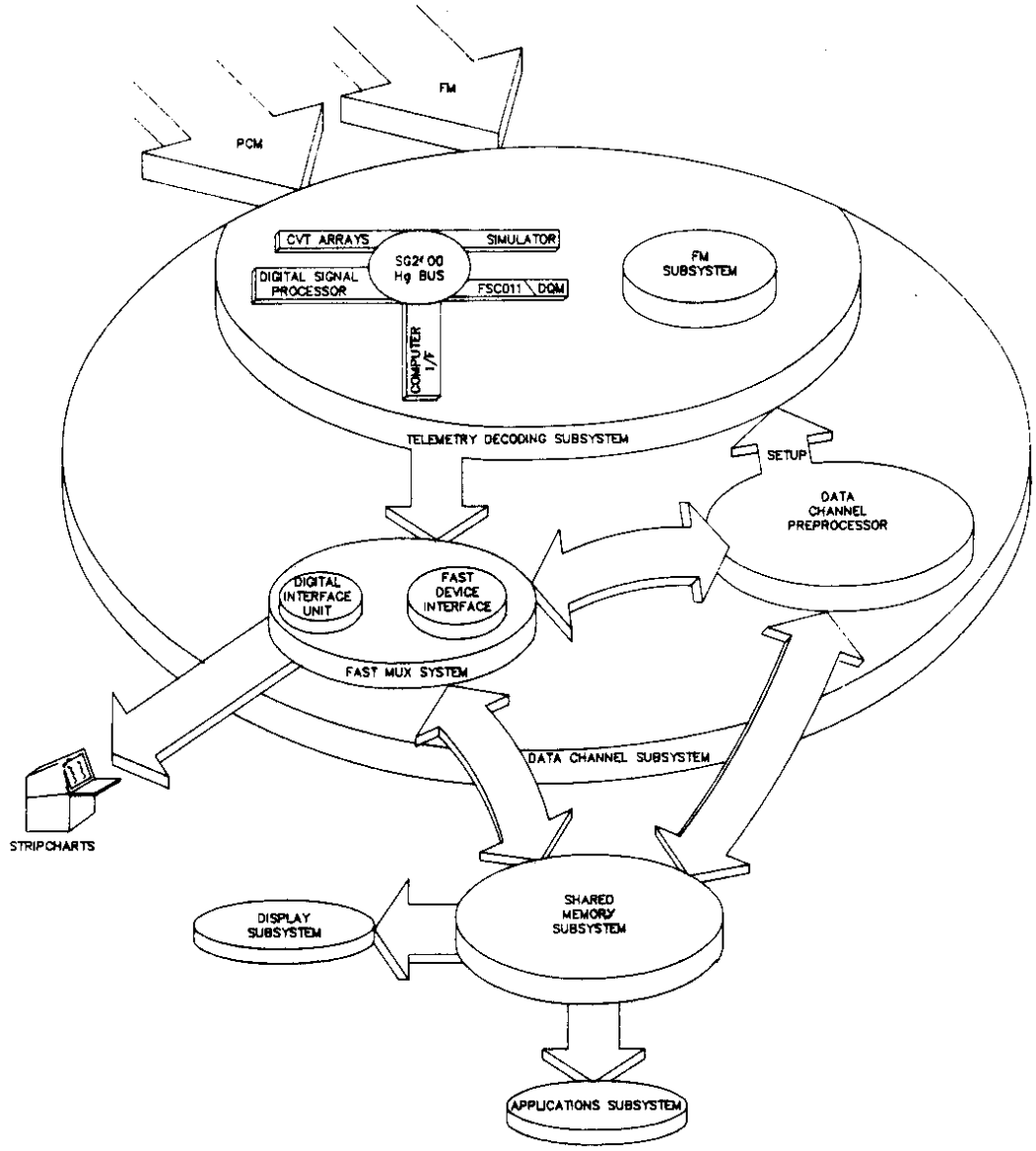

Figure 2. Data Channel Subsystem
(After Reference 2)

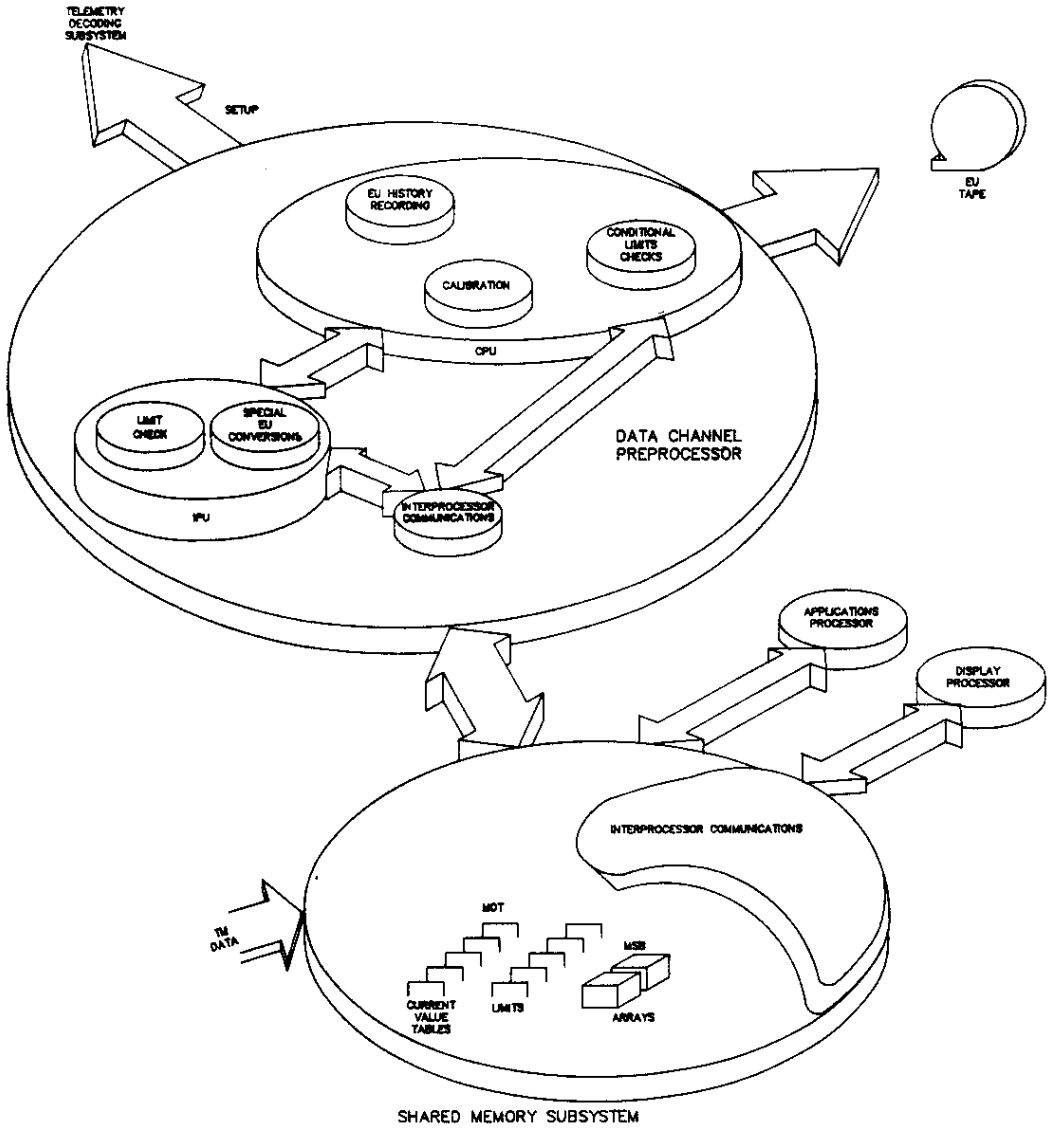

Figure 3. Data Channel Preprocessor (After Reference 3)

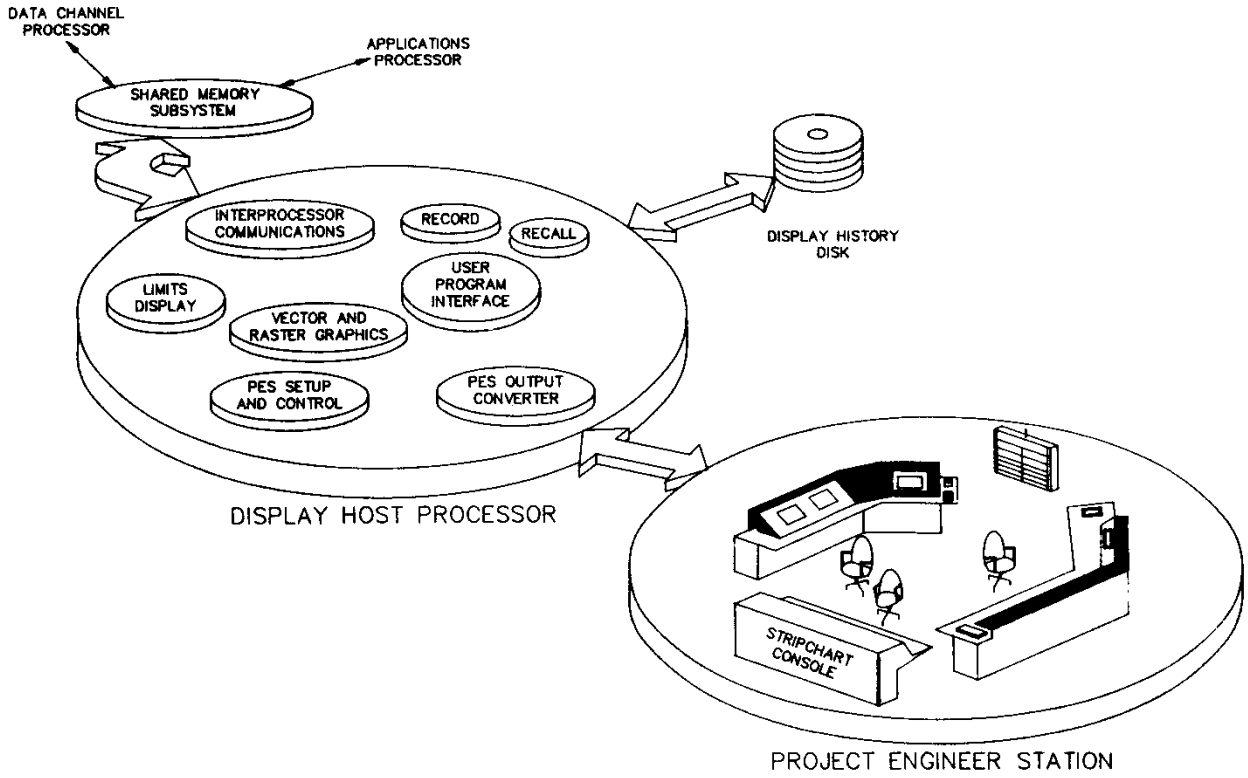

Figure 4. Display Subsystem (After Reference 4).

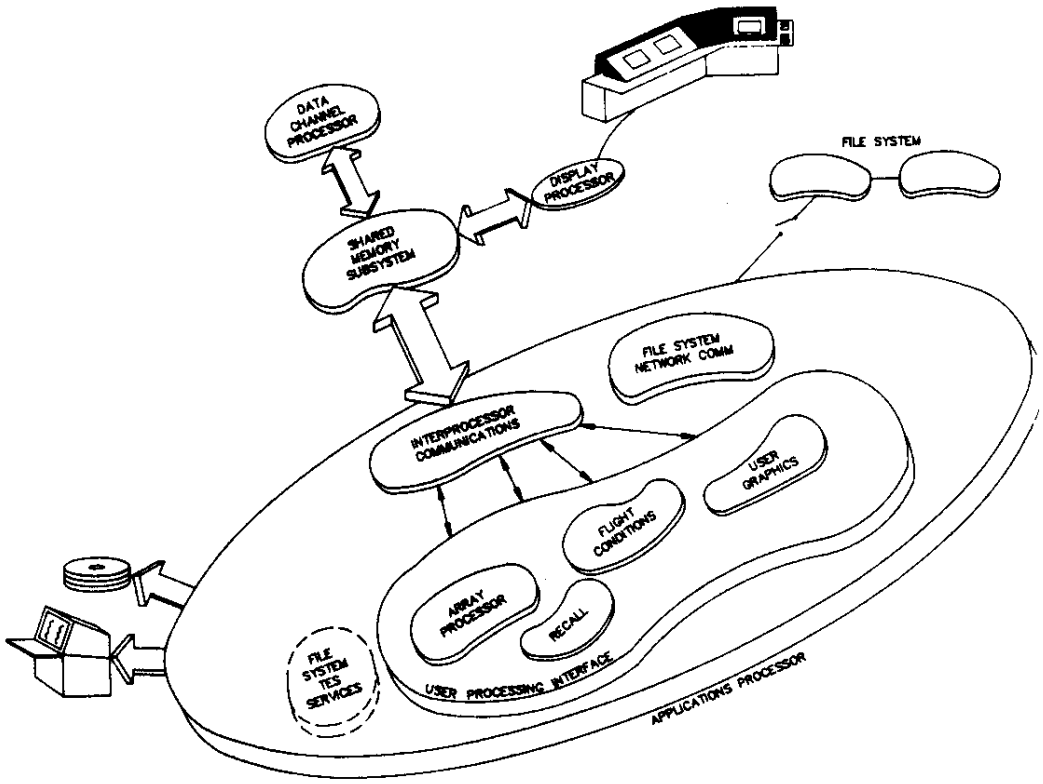

Figure 5. Applications Processor Subsystem
(After Reference 5)

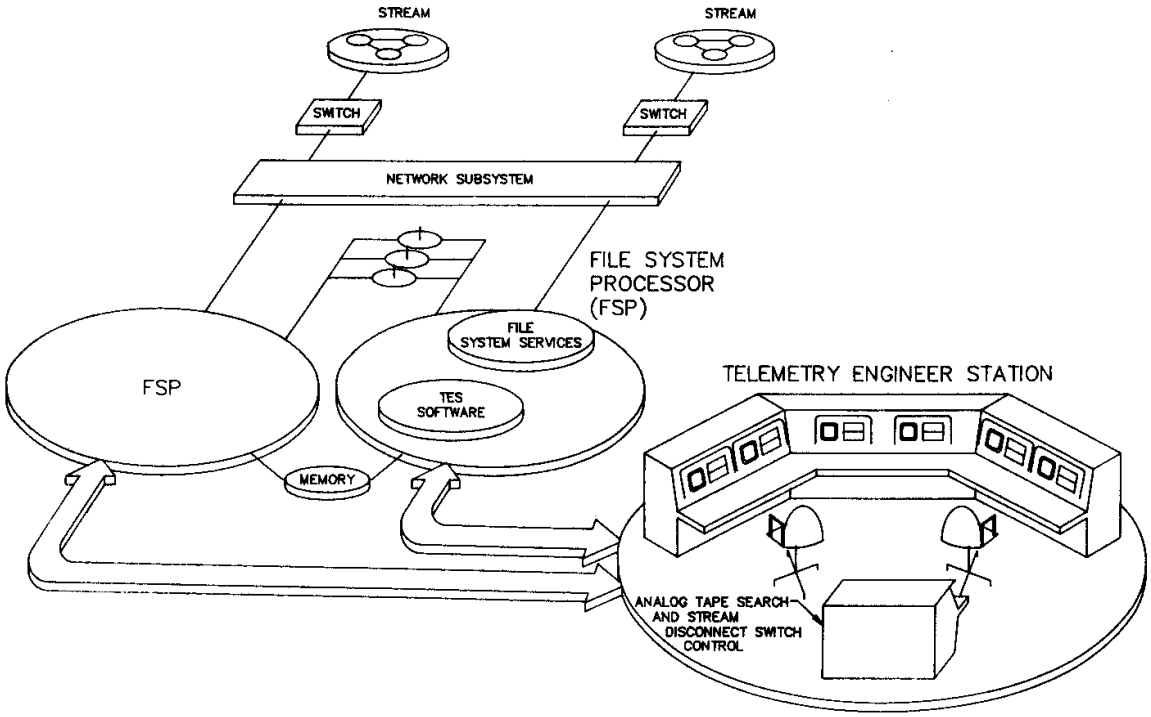

Figure 6. The File System
(After Reference 6)