NEW CONCEPTS IN PCM ENCODING

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ABSTRACT

The Pulse Coded Modulation (PCM) Encoder Systems used in telemetry have gained enormous flexibility for various applications because the input data channels and frame sync codes are programmable via the EEPROMs or UVEPROMs. The firmware in the current PCM Encoder Systems can be readily tailored for a specific application to monitor numerous types of analog channels, as well as digital channels. However, the current PCM Encoder Systems require several types of strap options which dictate not only a limited choice of gains and offsets, but also a fixed choice of the premodulation filter characteristics.

The brain of the 1000 PCM Encoder is the Digital Signal Processor (DSP) which eliminates the fixed premodulation filter characteristics via digital filter functions, and also eliminates strap options via general purpose microprocessor functions.

INTRODUCTION

PCM Encoding is one of the most widely used data acqusition techniques in Telemetry Systems. The implementation of a microprocessor or a sequencer has been considered for a total programmability of the PCM Encoder. The PCM System which uses EEPROMs or UVEPROMs with a simple counter circuit will, in most cases, provide the necessary functions for programmability of the PCM Encoders. Therefore, the use of a microprocessor or a sequencer is an overkill capability, unless the system requires an UP/DOWN link capability or other intelligent functions. Even if the implementation of such an overkill is justified, the premodulation filter characteristics are not dynamically programmable. i.e., an incomplete task in terms of a total programmability.

The 1000 PCM Encoder System is designed to eliminate the above deficiencies by configuring the system via software, including the premodulation filter coefficients. The software system configuration is achieved via the Initialization Routine. This system completely eliminates strap options, and enables the realization of a standardized hardware

(i.e., off-the-shelf PCM Encoder system) for Various applications in programmable data acqusition systems.

SYSTEM DESIGN APPROACH

The underlying design criteria for the new system, in generalized form, consist of the following:

1) Implementation of the Digital Signal Processor.
2) The data rate shall be at least 2 MBPS in BIO form or 1 MBPS in NRZ form.
3) The system configuration shall be realized via software (i.e., no strap options).
4) Standardization of hardware except for the number of input modules.
5) Universal bus structure for the input modules.
6) Maximum number of input channels of up to 64 thousand.
7) Maximum current drain by the standardized modules shall not exceed 700mA.
8) Maximum current drain by each Analog module or Bi-level module shall not exceed 20 mA.
9) Minimum number of input channels per Analog module shall be 16 for differential and 32 for single ended.
10) Minimum number of input channel words per Bi-level module shall be 4 with 12 bit resolution.
11) Physical dimension for each input module shall not exceed 1.6" x 1.5" x 0.4".
12) Physical dimension for each module comprising the standardized hardware, except the Power Supply, shall not exceed 1.6" x 2.5" x 0.8".
13) The physical dimension of the Power Supply module may vary from 1.6" x 2.5"x 0.8" to 1.6 x 2.5" x 2.0" depending upon the system.
14) Utilization of LID packaging for surface mounting of chip carriers.

DIGITAL SIGNAL PROCESSOR

The Digital Signal Processor (DSP) is the brain of the 1000 PCM Encoder System. The DSP is capable of handling both general purpose microprocessor functions and digital signal processor functions. The control functions of the time multiplexed input channels, data conversion with desired gains and offsets, and initialization routines are achieved by the general purpose microprocessor functions of the DSP. However, the digital filter functions of the premodulation filters are achieved by the digital signal processor functions of the DSP.

INITIALIZATION ROUTINE

After the “power-up” reset, the system enters Initialization Routine to configure the following parameters:

1) Bit Rate
2) Resolution
3) Gains and offsets for analog channels
4) Input channels for the format
5) Premodulation filter coefficients

In addition to the parameters mentioned above, frame sync codes and super-com/sub-com channels can be programmed via EEPROMs in the User Memory module.

STANDARDIZATION OF THE HARDWARE AND UNIVERSAL BUS FOR INPUT MODULES

Figure 1 illustrates a simplified system block diagram of the 1000 PCM Encoder. The standardized modules in the system consist of the following:

1) 1000 PS1 (Power Supply, 28 VDC input, DC-DC Converter)
2) 1000 DSP1 (Digital Signal Processor module)
3) 1000 UMEM1 (User Memory module, 8k x 16 EEPROM)
4) 1000 CTL1 (Control Logic module)
5) 1000 AD1 (Analog to Digital Convertor module)
6) 1000 DA1 (Digital to Analog Convertor module)

The universal bus structure accelerates the interchangeability of the input modules without altering software unless the users wish to reformat the input channels in the frame.

HARWARE DESIGN APPROACH
FUNCTIONAL DESCRIPTIONS OF THE INPUT MODULES

Although there are numerous types of input modules for various applications, most systems will include some form of Analog Multiplexers and Bilevel Multiplexers. Only Differential Analog Multiplexer (DAM) and Bilevel multiplexer (BM) will be discussed in this paper since they are the most commonly used type of input modules.

The outputs of the Low Level Amplifier signals are coupled to the input side of the DAM module. The desired sequence of the input channels are programmed in the User Memory. The outputs of the DAM module are multiplexed in time division and fed to the Analog to Digital Converter (ADC). The appropriate gain and offset adjustments are then made via the general purpose microprocessor function of the DSP, which eliminates the need for Programmable Amplifiers.

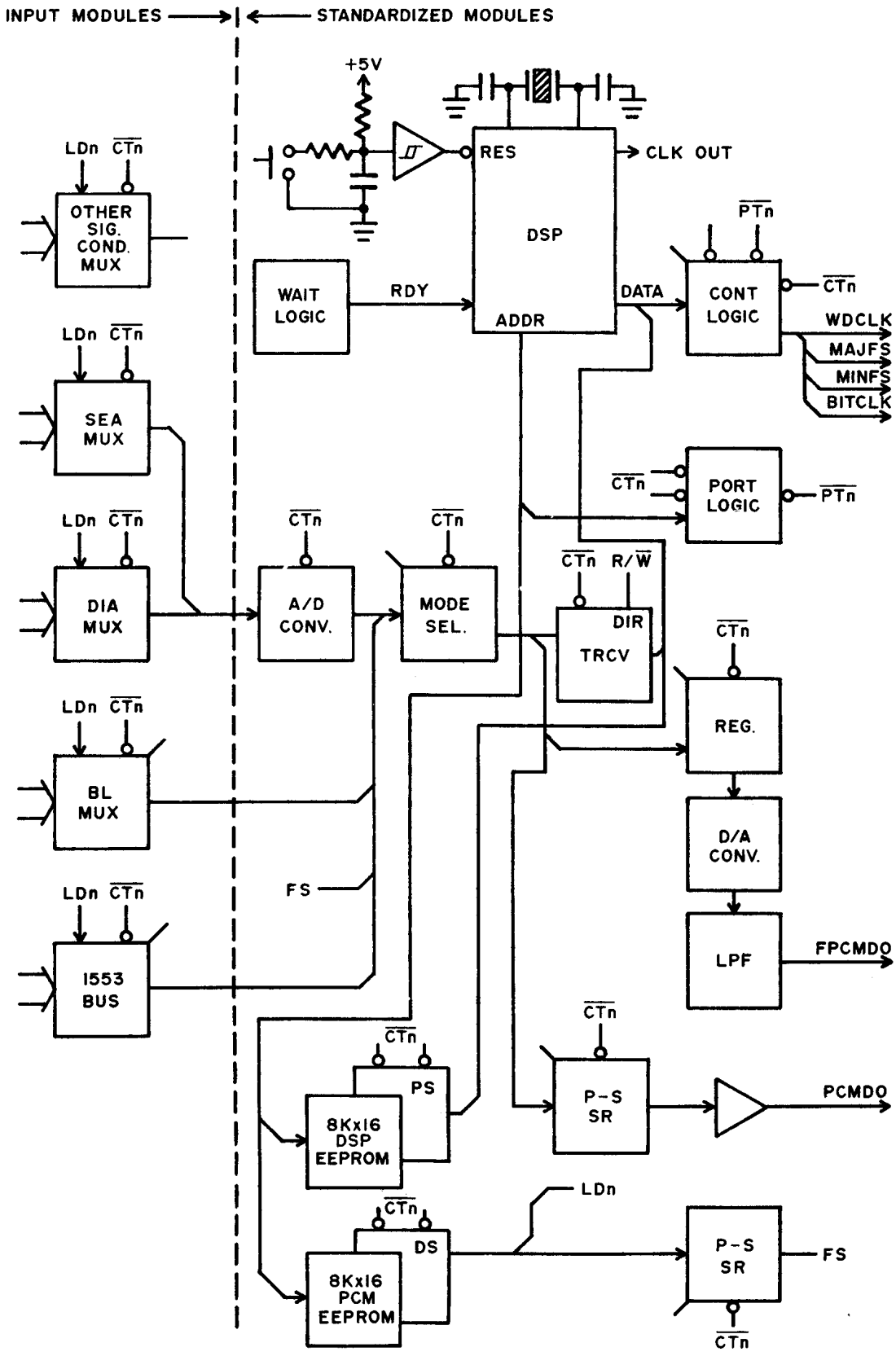


FIGURE 1
A SIMPLIFIED SYSTEM BLOCK DIAGRAM OF THE 1000 PCM ENCODER

The digital input signals are coupled to the BM module. The outputs of the BM are multiplexed in time division and subsequently shifted in serial form. The serial output data of the BM are then fed to the Mode Select logic circuit of the ADC module.

FUNCTIONAL DESCRIPTIONS OF THE ADC MODULE

The ADC module consists of mode select logic and analog to digital converter circuits. One of the limiting factors in real time processing is the conversion rate of the ADC. The ADC module receives analog input signals with full scale range of +/- 10 volts from the Analog Multiplexer modules. The ADC converts the analog input signal to a digital output with 12 bit resolution. The converted digital output data are then shifted in serial form before being sent to the mode select logic. The mode select logic receives serial data from bilevel multiplexers, analog to digital converter, and frame sync codes. The desired output mode (i.e., NRZ, BIO, M/S) are selected during the initialization routine along with the corresponding DSP routines.

FUNCTIONAL DESCRIPTIONS OF THE CONTROL LOGIC MODULE

The Control Logic Module generates Bit Clock, Word Clock, and other control signals to steer system's data paths from/to the DSP module. When the DSP is executing instructions from the program space, the steering logic circuit is disabled to prevent data flow from/to the I/O ports. When the DSP executes instructions from the I/O space, the steering logic circuit is enabled to read and write data from/to the I/O ports. The desired Bit Clock and Word Clock rates are selected via initialization routine.

FUNCTIONAL DESCRIPTIONS OF THE USER MEMORY MODULE

The User Memory module consists of 8k x 16 EEPROMs and logic circuits. The maximum number of input data channel is 64 thousand, provided that there is a sufficient power in the system to handle the large number of Input modules. The EEPROMs are addressed when the DSP executes instructions in the data space. Programming the desired sequence of the input data channels and frame sync codes (Format) is accomplished via an external connector (RS-232) from the IBM PC. When the frame sync code channels are addressed, the data is shifted in serial form before being sent to the mode select logic circuit of the ADC.

FUNCTIONAL DESCRIPTIONS OF THE DSP MODULE

The DSP module consists of Wait logic, Porting logic, EEPROMs (8k x 16), and a Digital Signal Processor (TMS320C25). Although the DSP can be operated up to 10 Mhz, the actual system clock frequency is reduced to 4 Mhz to avoid an excessive Wait state

generation during the fetch cycle. The EEPROMs are enabled when the DSP executes instructions from the program space. Executing an instruction from the program space requires one Wait state. The codes for the Digital Filter routines will be down loaded to the Block 0 of the data space during the initialization routine. Therefore, the Digital Filter routines are executed without a Wait state. The Porting logic circuit controls the data paths of I/O ports.

FUNCTIONAL DESCRIPTIONS OF THE DAC MODULE

The processed data from the DSP are transferred to the Digital to Analog Converter (DAC) in parallel form. The filtered portion of the data is then converted to an analog form via the DAC. The output of the DAC is fed to the low pass filter to remove glitches due to high frequency switching of the DAC. The unfiltered portion of the data is fed to the parallel to serial shift registers to form a serial PCM data output.

SOFTWARE DESIGN APPROACH

There are four design tasks in the software design; namely, Initialization Routine, PCM Routine, DSP Routine, and Output Routine. In order to realize the real time process with 4 Mhz system clock, 1 Mhz Bit clock, and 12 bit resolution, the total number of codes in PCM, DSP, and Output routines should not exceed 48 machine cycles. Figure 2 illustrates the memory map and a simplified flow chart of the system. Refer to appendix A for the program in the TMS320C25 assembly language.

SUMMARY AND CONCLUSIONS

One of the many highlights of new concepts in PCM Encoding is the implementation of the DSP in real time process which eliminates tedious ways of configuring the system by the use of strapping. The system configuration via software, including the premodulation filter characteristics in digital filter, is the most significant improvement. Therefore, the standardization of hardware for the PCM Encoder in the Telemetry system is realizable.

REFERENCES

1. Atlanta Signal Processor, Inc. 1985, Digital Filter Design Package.
2. Oppenheim, Alan V. and Schafer, Ronald W., 1975, Digital Signal Processing.
3. Rabiner, Lawrence R. and Gold, Bernard, 1975, Theory and Application of Digital Signal Processing.
4. Texas Instrument, 1986, TMS32C25 User’s Guide.

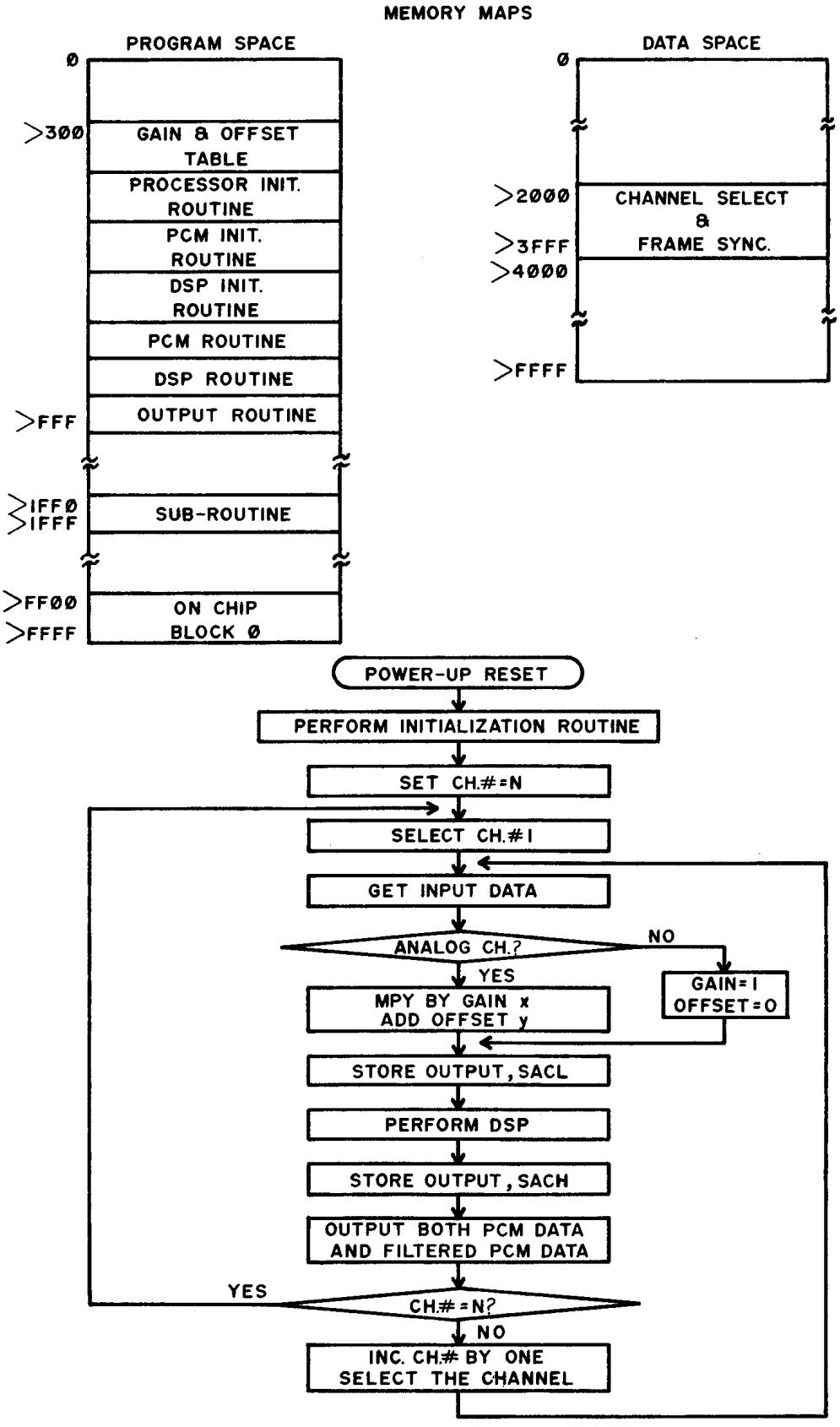
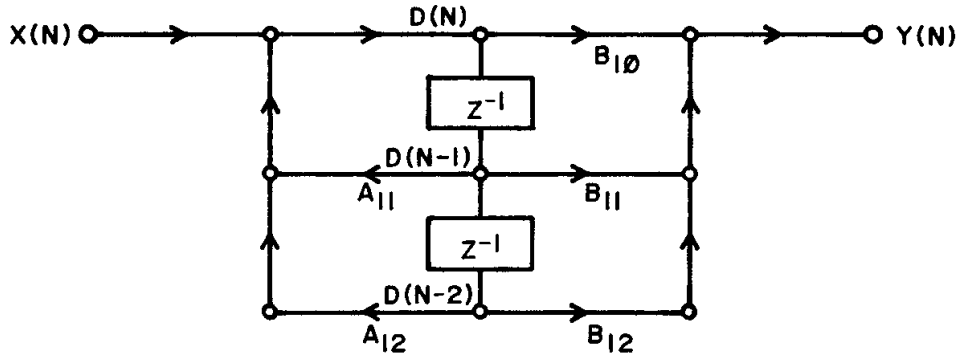


FIGURE 2
FLOW CHART OF THE SYSTEM SOFTWARE

APPENDIX A

A typical second order, single stage, IIR low pass filter:



D(N) = A11 * D(N-1) + A12 * D(N-2)
Y(N) = B10 * D(N) + B11 * D(N-1) + B12 * D(N-2)

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LAC     XN,15       GET VALUE OF X(N) IN Q15 FORM
LT      DN1         LOAD T REG. WITH D(N-1)
MPY     A11         MULTIPLY T REG. BY A11
LTA     DN2         LOAD T REG. WITH D(N-2) AND ACCUMULATE
                    PREVIOUS PRODUCT
MPY     A12         MULTIPLY BY A12
APAC
SACH    DN,1        STORE THE RESULT IN D(N)
ZAC
MPY     B12         MULTIPLY T REG. BY B12
LTD     DN1         LOAD T REG. WITH D(N-1), ACCUMULATE
                    PREVIOUS PRODUCT, AND MOVE DATA
MPY     B11         MULTIPLY T REG. BY B11
LTD     DN          LOAD T REG. WITH D(N)
MPY     B10         MULTIPLY T REG. BY B10
APAC
SACH    YN, 1       STORE THE RESULT IN Y(N)
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