QUATERNARY MODULAR ADDER WITH APPLICATION IN CORRELATIVE CODING TECHNIQUES

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ABSTRACT

A general tendency in the digital communication systems is toward multi-level signalling in order to increase the information rate over a fixed bandwidth channel. Multiple valued logic circuits hold the promising potential for this application. including digital modulation, signal power spectrum shaping and coding techniques.

Thispaper will present a novel design of quaternary modular adder circuit using multi-semiconductor technology — *BI-CMOS* process. This circuit demonstrates many advantages in improving noise margin and speed as well as in reducing transistor counts and chip areas. Some comparison with its binary counterpart and *SPICE* simulation results will also be given.

Due to growing interest in multiple-level signalling combining with multiple-valued logic technology in digital communication systems, this paper will also discuss the application of modular adder in correlative coding techniques for spectral shaping. where quaternary modular adder performs efficiently in encoding input signal of non binary form at the transmitting end and in reconstructing the original data input at the receiving end. It also can allieviate the pin and interconnection requirements for equivalent information transfer.

INTRODUCTION

Multiple-valued logic (*MVL*) has many potential applications in the broad field of communications. For example, at the chip level, *MVL* can alleviate the pin problems that limit development of *VLSI* technology. The pin limitation leads to the necessity to time-share binary signals on data channel and *I/O* pins, which in turn involves speed restraints, testing difficulties and other problems. Multi-valued signalling holds the promising potential to reduce the pin number requirements for an equivalent information transfer and to increase the packing density in the sense that more information could be processed per

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unit volume. Thus a general tendency in the digital communication systems is toward multi-level signalling in corperating with *MVL* circuits to increase the information rate over a fixed bandwidth channel.

Recently the approach to design and implementation of *MVL* systems has been to demonstrate, for a specific technology, circuits to realize a complete set of algebraic connectives. Modular adder is an integral part of these algebraic operations. It is a basic building block in Modular algebra, and it can also be viewed as a generalized cyclic gate in Post algebra. Minor modification of this adder would result in a multiple-valued full adder which is used widely in various digital signal processing and arithmetic units. Since modular adder is one of most flexible gate bridging a variety of *MVL* algebras, many versions of modular adder circuits have been proposed and designed. Although different semiconductor technologies have been tried, the existing *MVL* can generally be grouped into three different technologies with different signal representations as follows:[1]
(a) MOS and CMOS technology using voltage signal representation.
(b) Bipolar technology using current signal representation.
(c) Charge couple device (*CCD*) technology using charge signal representation.

All of above three technologies have their own advantages and disadvantages: *MOS* and *CMOS* technology, owing to its high density and lower power consumption. made itself first choice of semiconductor technology for *VLSI* design. Bipolar *IC* technology has fastest switching time and most suitable for current circuit design and current steering technique such as in *ECL*. *CCD* logic is actually dynamic *MOS* logic. It is, however, not well developed and tested technology for *MVL* circuit. As a matter of fact, modular adders (or full adders) have been designed and simulated many times in the first two technologies: either *CMOS* or Bipolar, simply because they are most sophisticated *IC* technologies thus far. However, it is not clear at this moment whether *CMOS* or *ECL* technology is best suited to our application. Our purpose, in this chapter, is trying to use a novel *BI - CMOS* technology to design a current-mode quaternary modular adder.

BI - CMOS Technology

At present almost all contrubutions to *MVL* modular adder circuit design have exclusively restricted themselves to one single semiconductor technology, but this is not always necessary. In fact, combining two or more semiconductor technologies together to *MVL* circut chip design can result in relatively ideal performance in some cases, or can trade off for desired performance in some other cases, as we will see later in this paper. Particularly we are very interested in combining CMOS and Bipolar technologies. not only because they are fully developed technologies, but also because they have very similar fabrication processes. This will result in a novel *BI - CMOS* technology for *MVL*.

The process for *BI - CMOS* technology, starting with *N*-type wafer, can be briefly outlined as following:

(1) Grow a *P*-type epitaxial layer on the surface of the wafer. This layer is the substrate of the chip.

(2) Diffuse Phosphorous into *P*- substrate to form *N*-well where either *PMOS* transistors or *NPN BJT* transistors will be placed,

(3) Grow Silicon Dioxide (SiO_2) to define active areas for *PMOS*, *NMOS* and *BJT* transistors.

(4) Diffuse Boron into *N*-well where *NPN BJT* are defined to form base regions.

(5) Grow a thin layer of Silicon Dioxide. This is the gate oxidation for both *PMOS* and *NMOS* transistors.

(6) Deposit Polycrystalline Silicon to form gates for both *PMOS* and *NMOS* transistors.

(7) Dope P^+ impurities into *N*-well where *PMOS* transistors are defined to form drains and sources for these *PMOS* transistors, meanwhile to form the base ohmic contacts for *NPN BJT* transistors.

(8) Dope N^+ impurities into the following three regions:
(a) into P^- substrates where *NMOS* transistors are defined to form sources and drains for these *NMOS* transistors.
(b) into *NPN BJT* base regions to form emitters of *NPN* transistors.
(c) into *N*-well where the ohmic contacts will be placed.

(9) Mask to open contact windows.

(10) Metallize for connections in the chip.

CIRCUIT DESIGN AND OPERATION

The modular adder design is based on current mode consideration simply because addition can be achieved through current summation by wired connections. The unit logic current is chosen as $100\mu A$ since we use both *CMOS* technology and *BJT* technology. At biasing current = 100 μA, *BJT* has relatively high current gain B_f($B_f > 100$) [2] and *MOS* transistor has relatively large driving current, therefore the circuit speed is expected to be improved with reasonable power consumption. The power supply voltage level is chosen

as *Vcc = DC.* 5*v*, which is suited to both *CMOS* and *ECL* circuits. Figure 1 shows the *BI - CMOS* quaternary modular adder circuit schematic.

The circuit can be divided into two stages: input stage and output stage. The input stage is current-voltage converters, which will sense the input curret and convert it to corresponding voltages driving the second stage. *CMOS* technology is chosen to design the input stage. In Figure 1 *PMOS* transistor M_1 is diode-connected to sense the input logic current (0- 700μA corresponding to logic number 0-7). *PMOS* transistors M_2 and M_3 replicate this input current. M_2 and *NMOS* transistor M_4 together form a current-voltage converter which will produce a voltage signal to steer the current in an *ECL* pair formed by *NPN* transistors Q_1 and Q_2. If the input current is equal to or greater than the logic level 4 (400 μA in current), then Q_1 will turn on and a 400μA current will be subtracted from the replicated input current by M_3. Thus, *NMOS* transistor M_5 only experiences the input current molulo 4. *NMOS* transistors M_6, M_7 and M_8 replicate this modulo 4 input current, together with *PMOS* transistor M_{10}, M_{11} and M_{12} form three current-voltage converters to produce voltage signals driving the second stage. The second stage is made up of four ECL pairs formed by *NPN* transistors Q_1 and Q_2, Q_3 and Q_4, Q_5 and Q_6, Q_7 and Q_8. Q_1 - Q_2 pair, as mentioned above, offers a 400μA current necessry for modulo 4 operation, while the other three *ECL* pairs are driven by three current-voltage converters in the input stage. Note that the three *ECL* pairs have an identical voltage reference. Every *ECL* pair will output an unit logic current (100μA) whenever its input voltage exceeds this voltage reference. Therefore the Q_3 - Q_4 pair alone will output one unit logic current when the input logic current is 1 unit or 5 units; both Q_3 - Q_4 pair and Q_5 - Q_6 pair will together output 2 unit logic current when the input logic current is 2 units or 6 units; the Q_3 - Q_4, Q_5 - Q_6 and Q_7 - Q_8 pairs will together output 3 unit logic current when the input logic current is 3 units or 7 units. Finally if the input current is zero or 4 units, the output will be zero. This is, obviously, a modular 4 operation and the current summation is performed at the input node through wired connections.

This circuit takes advantages of both *CMOS* technology and *BJT* technology. Since specifying (*W*/*L*) ratio is easy and geometrically matching *MOS* transistors can be done precisely. designing the input stage by *CMOS* technology is able to precisely replicate the input current and provide accurate unit logic current for output. Meanwhile great discrimination in current-voltage converter outputs can be obtained since the active loads in these converters can be easily changed through specifying (*W*/*L*) ratio for *PMOS* transistors M_6,M_7,M_8 and *NMOS* transistors M_4,M_{10}, M_{11}, M_{12}. For the second stage, differential pairs are used to form threshold detectors. They will provide fast switching speed due to the current steering nature of *ECL* technique. Because *ECL* pairs are cascaded with current voltage converters, large transition gain of modular adder is achieved due to multiplication of the two stage gains. Note that in this circuit only one

voltage reference is used. This voltage reference is provided by three diode connected *NPN* transistors in series. i.e Q_{10}, Q_{11} and Q_{12} since the voltage drop between base and emitter of *BJT* is very stable. All of these yield better noise margins for the circuit. An improved Wilson current source is designed using *CMOS* technology, which provides the biasing current for the *CMOS* current-voltage converters in first stage and the steering current for the differential pairs in second stage. Diode-connected *NPN* transistor Q_9 is used in this current source to obtain the stable reference current.

4μ(*Lemd*a = 2μ) *IC* fabrication process is used. The transistor parameters in this circuit are very close to pratical parameters used in industry, therefore the process is feasible.

SIMULATION RESULTS AND COMPARISONS

Spice 2*G* program is used to simulate *BI - GMOS* quaternary modular adder. Figure 2 shows its transfer function. Note that here we have obtained excellent noise margin: the input noise margin at every logic level is allowed up to around 40% unit logic current value (i.e. + 40 μA) and within this range the output deviation at every level is less than 5% of unit logic current value (i.e, + 5 μA). Power consumption of this modular adder is less than 8 *mW*. When an identical modular adder is loaded, the delay time of this circuit is less than 290 μS in the worst case, and less than 100 μS on the average.

This circuit requires totally 40 devices, i.e, 12 *PMOS*, 15 *NMOS*, 12 *NPN* transistors and one resistor for Wilson current source. The total chip area is estimated as less than $8 \times 10^{4} cm^{2}$. This is, as matter of fact, very conservative estimation. If the resistor in Wilson current source can be fabricated through some other process such as base diffusion, base pinch, or epitaxial resistance, the total chip area will be further reduced by a factor of 2 or more. Minor modification of this adder would result in a multiple- valued full adder, three more transistors are needed to obtain carry-out, resulting in total device count equal to 43 .

In binary case a total of 42 devices are required to realize one binary full adder by *CMOS* technology [3], therefore two binary full adders are needed to implement same function as the quaternary full adder does, the total device count thus is equal to 84. This implies that *BI - CMOS* quaternary adder, in addition to reduce the connections and interconnections, can reduce the device count by a fact of 48% when compared with binary *CMOS* implementation. A comparison with existing All-*CMOS* quaternary full adder is listed in Table 1 [4].

APPLICATIONS

Since the implementation with quaternary logic is more pertinent to some operations in digital signal processing and computing, the quaternary modular adder will find itself in a variety of applications. One promising application, perhaps, is the digital filter design using *MVL* and Delta modulation [5]. The *VLSI* implementation of digital filter by combining Multiple-valued logic and residue number system arithmetic has also been developed [6]. Recently, the optoelectronics also pays more attention to *MVL* [7]. Digitally computing using signed-digit number representation will be more efficient if *MVL* adder is used [8]. Here we discuss one of multiple level signalling techniques in digital communication, i.e. the "correlative coding for spectral shaping".

There are two basic methods for shaping the signal power spectrum: one is by filtering the waveform (in the frequency domain), the other is by coding the signals (in the time domain). Correlative coding is the process of converting the original two level signal into (typically) a three level signal and introducing a controlled level of *ISI* [9]. The correlative coding/filtering can be modelled as in Figure 3(a). This block diagram can be redrawn as a single "conversion filter" which can be used to process binary or multi level signals as shown in Figure 3(b).

The encoder is included to prevent a phenomenon called error propagation, which occurs when a received error causes additional errors in succeeding symbols due to the inherent symbol correlation. At "A_t" , the data appears in a nonbinary form and has 2^n levels. The symbols are uncorrelated and each represents two or more binary digits. The encoder converts the *R*-level input, consisting of independent digits, into a *R*-level source with a memory extending over a fixed number of digits, (typically one or two). Next, level conversion is accomplished by using a level conversion filter. Such a filter causes an overlap of pulses and introduces a controlled amount of *ISI*. As a consequence, the number of levels at "C_t" is $2R - 1$. Correlation properties are inherent in such a waveform. In addition, it is possible to associate each level with the non-binary input at "A_t". At the receiving end, the reconverter reconstructs the original data input at "A_t" by identifying each digit independently, without resorting to the past history of the correlative waveform. In this way received errors do not cause additional errors in the succeeding symbols.

One specific encoding and conversion process for the *R*-level case is

$$A_t = B_t + Z^{-2} B_t \ (mod\ R) \tag{1}$$

$$C_t = B_t - Z^{-2} B_t \ (algebraic) \tag{2}$$

$$C_t \ mod\ R = A_t \tag{3}$$

where Z^{-2} corresponds to a two symbol delay. At the receiver, A_t is determined by simply performing the operation $C_t \ mod \ R$.

Error detection is done by first determine whether the extreme levels (top and bottom) correspond to the present and past digits originating from the encoder and digital memory. A comparison is made at the sampling instants of the extreme level digit of C_t. If there is a disagreement an error is indicated and the memory is reset to the correct state. A comparison is done when the extreme levels are present because only the extreme levels are formed in a unique way in correlative systems. Intermediate levels may be formed in more than one way and are therefore not suitable for the detection of errors. Figure 4 provides an example of the error detecting process for $R = 4$.

Of course, the modular adder can find its application in this correlative coding systems: Equation (1) for encoding is actually a modular addition operation. Equation (3) for receiving is also a modular addition operation.

The correlative coding systems have advantages when compared to zero memory systems in their error detection capability. Error detection in zero-memory systems requires a certain amount of redundancy in the symbols sent. Correlative systems have finite memory and this can be utilized to monitor and detect errors without introducing redundant digits at the transmitter.

CONCLUSION

In this paper, a novel *BI - CMOS* technology realization of quaternary modular adder has been presented. This technique yields the circuit of better performance. such as excelent noise margins, lower power consumption, less chip area and improved speed. *Spice* simulation results have proved these performance improvements. Some comparisons with existing All-*CMOS* full quaternary adder and binary *CMOS* adder have been given, which show the promising future of *MVL* and *BI - CMOS* technology. One application of modular adder in digital communication systems. i.e, correlative coding system, has been discussed, which shows advantages when compared to zero-memory system in their error detection capability.

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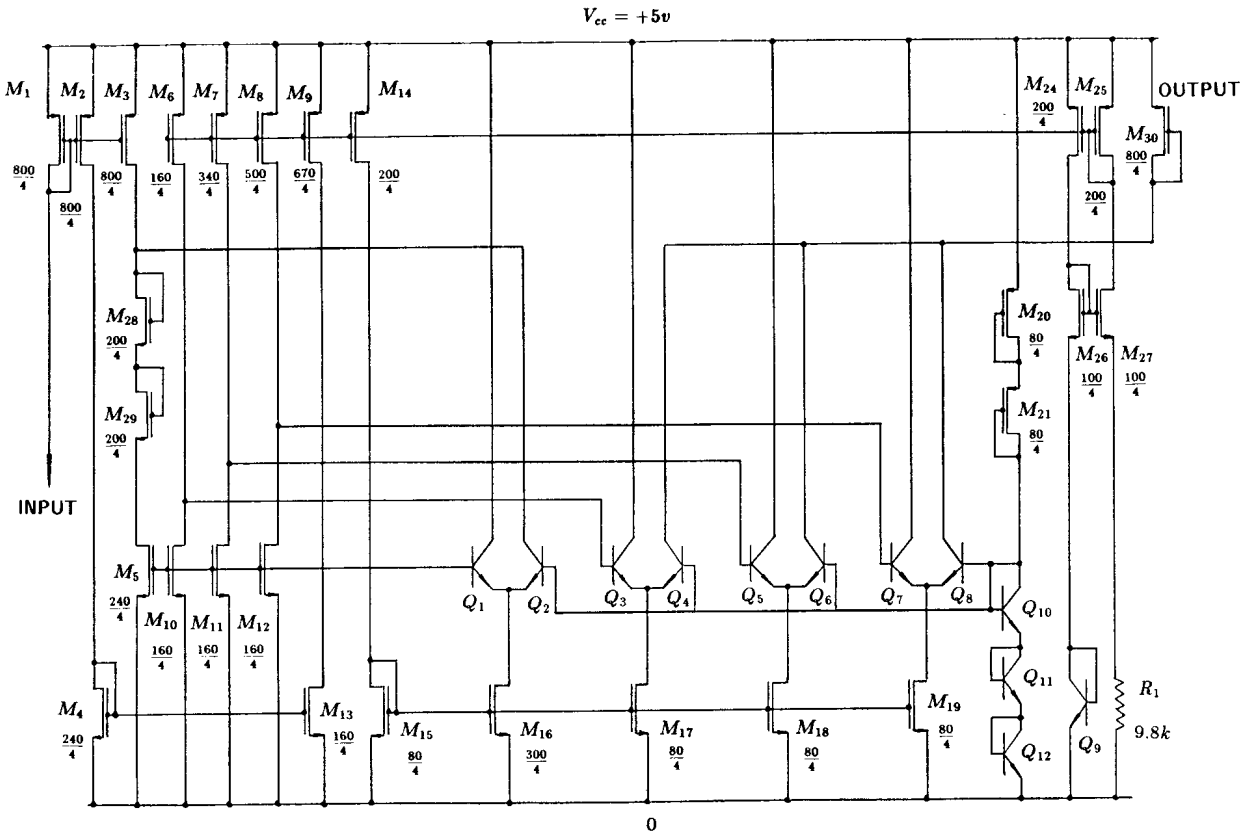

FIGURE 1 *BI - CMOS* QUATERNARY MODULAR ADDER

**** DC TRANSFER CURVES TEMPERATURE = 27.000 DEG C

****

IIN	I(VO)
0.000D+00	4.838D-12
1.000D-05	5.087D-12
2.000D-05	5.912D-12
3.000D-05	6.570D-12
4.000D-05	6.990D-12
5.000D-05	6.620D-09
6.000D-05	9.779D-05
7.000D-05	1.005D-04
8.000D-05	1.005D-04
9.000D-05	1.005D-04
1.000D-04	1.005D-04
1.100D-04	1.005D-04
1.200D-04	1.005D-04
1.300D-04	1.005D-04
1.400D-04	1.005D-04
1.500D-04	1.212D-04
1.600D-04	2.001D-04
1.700D-04	2.009D-04
1.800D-04	2.009D-04
1.900D-04	2.009D-04
2.000D-04	2.009D-04
2.100D-04	2.009D-04
2.200D-04	2.009D-04
2.300D-04	2.009D-04
2.400D-04	2.021D-04
2.500D-04	2.580D-04
2.600D-04	3.005D-04
2.700D-04	3.013D-04
2.800D-04	3.013D-04
2.900D-04	3.013D-04
3.000D-04	3.013D-04
3.100D-04	3.013D-04
3.200D-04	3.013D-04
3.300D-04	3.013D-04
3.400D-04	3.013D-04
3.500D-04	2.008D-04
3.600D-04	6.975D-12
3.700D-04	4.916D-12
3.800D-04	5.029D-12
3.900D-04	5.329D-12
4.000D-04	6.076D-12
4.100D-04	6.589D-12
4.200D-04	6.947D-12
4.300D-04	6.826D-11
4.400D-04	2.192D-05
4.500D-04	1.004D-04
4.600D-04	1.004D-04
4.700D-04	1.004D-04
4.800D-04	1.004D-04
4.900D-04	1.004D-04
5.000D-04	1.004D-04
5.100D-04	1.004D-04
5.200D-04	1.004D-04
5.300D-04	1.004D-04
5.400D-04	1.032D-04
5.500D-04	1.915D-04
5.600D-04	2.007D-04
5.700D-04	2.007D-04
5.800D-04	2.007D-04
5.900D-04	2.007D-04
6.000D-04	2.007D-04
6.100D-04	2.007D-04
6.200D-04	2.007D-04
6.300D-04	2.008D-04
6.400D-04	2.030D-04
6.500D-04	2.584D-04
6.600D-04	2.954D-04
6.700D-04	3.003D-04
6.800D-04	3.009D-04
6.900D-04	3.010D-04
7.000D-04	3.011D-04
7.100D-04	3.011D-04
7.200D-04	3.011D-04
7.300D-04	3.011D-04
7.400D-04	3.011D-04
7.500D-04	3.011D-04
7.600D-04	3.011D-04
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8.000D-04	3.011D-04

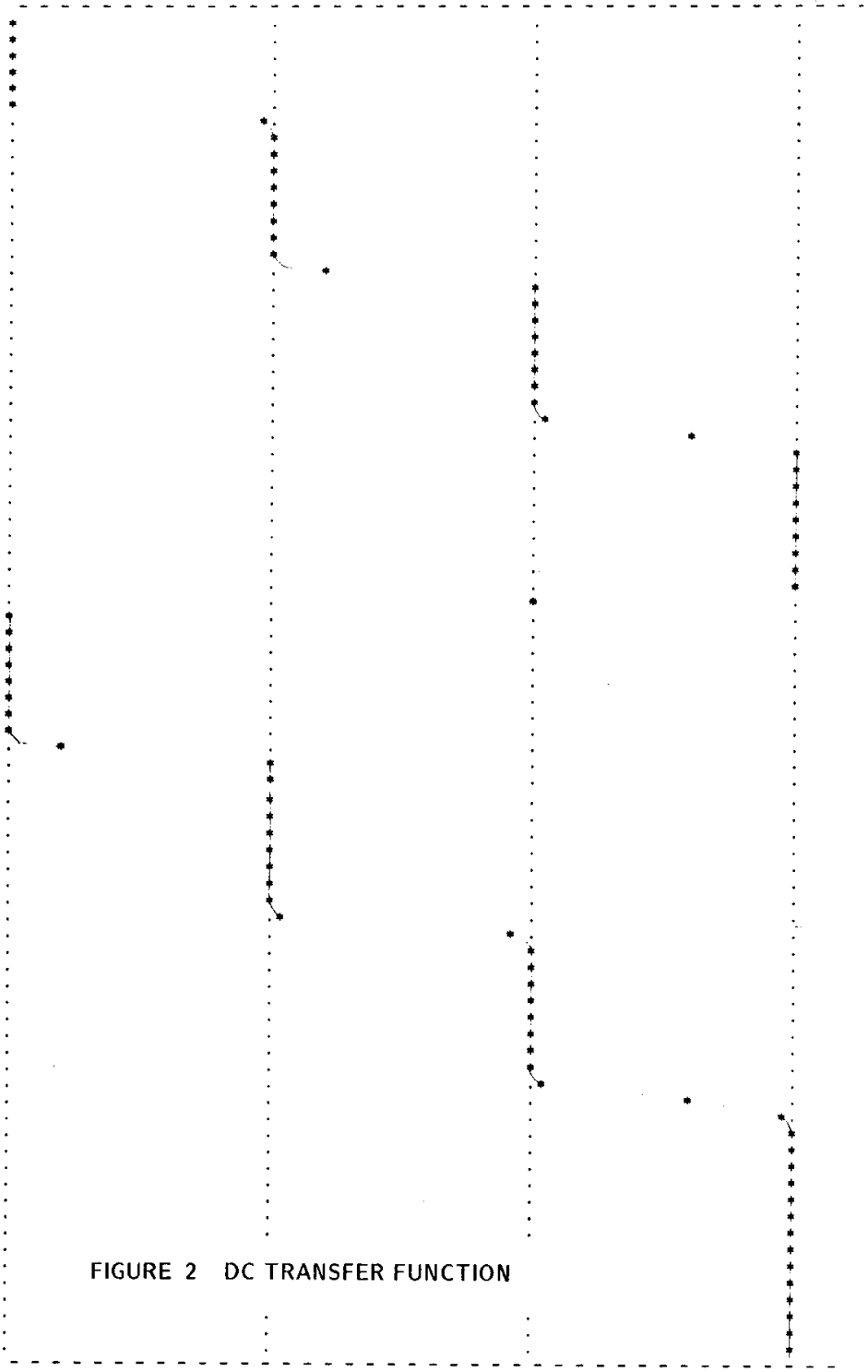

FIGURE 2 DC TRANSFER FUNCTION

Table.1 Comparison of *BI - CMOS* and All-*CMOS*

Quaternary Adder

Technology	All-*CMOS*	*BI - CMOS*	Remark
Power supply	5*v*	5*v*	Same
Device Count	74**	43	Save 46%
Chip Area	$< 16.7 \times 10^{-4} cm^2$	$< 8 \times 10^{-4} cm^2$	Save 52%
Power Consumption		$< 8mW$	
Worst Case Delay	375*nS*	290*nS*	Faster
Noise Margin		Output Deviation Less Than 5% Unit for Input Range within 40% Unit	

**See Reference [4] for Existing All-*CMOS* Quaternary Adder

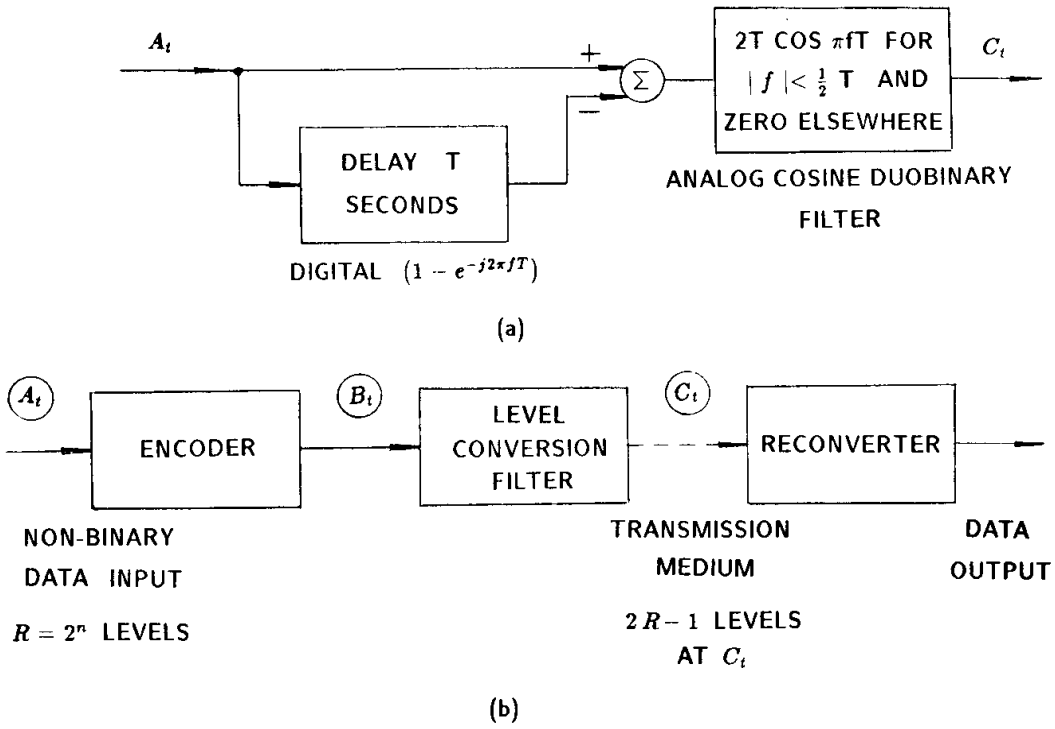

FIGURE 3 PARTIAL RESPONSE SIGNALLING

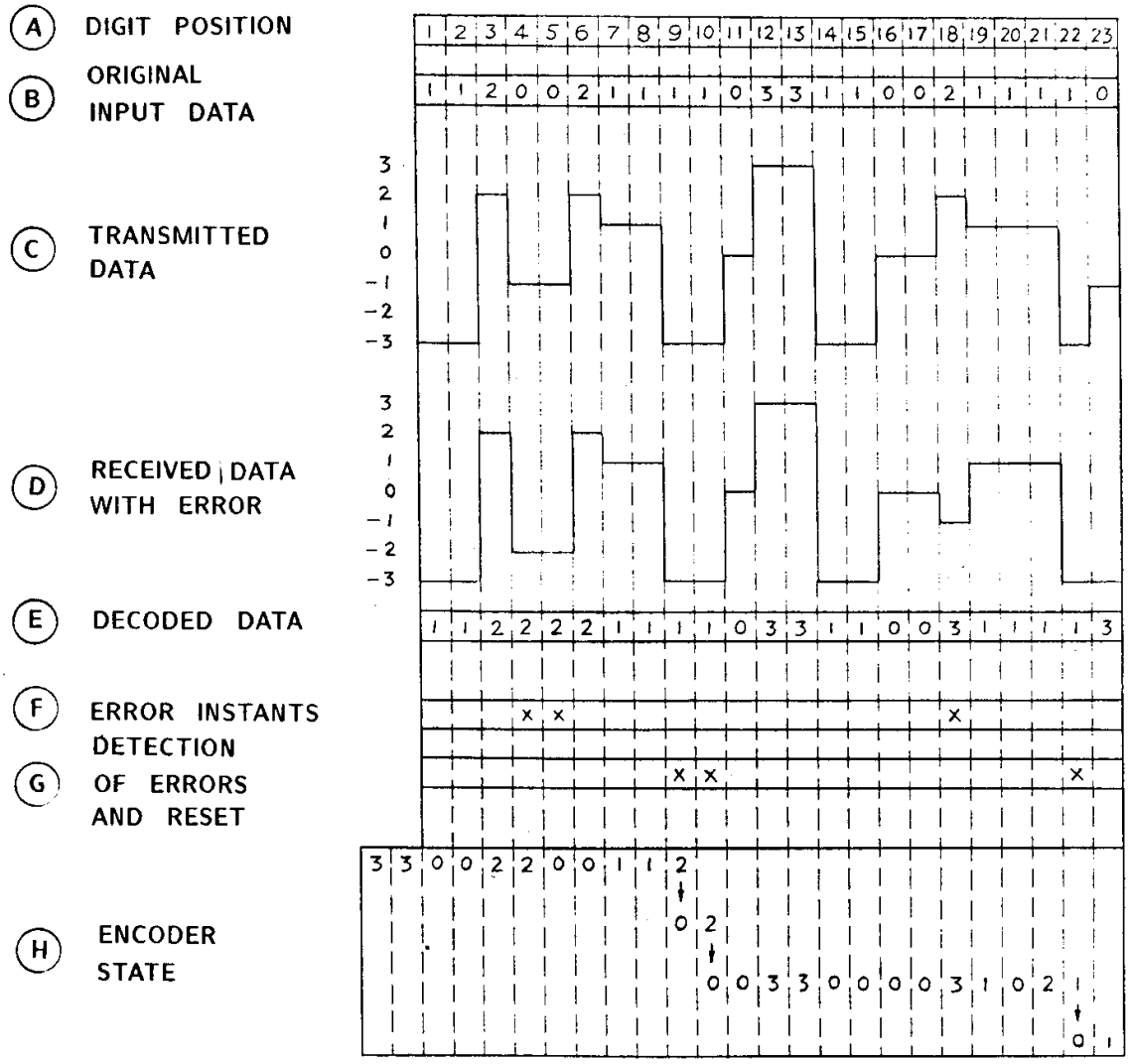

FIGURE 4 ERROR DETECTION FOR $R = 4$