A SURVEY AND COMPARISON OF MULTIPLICATION TECHNIQUES FOR ANALOG VLSI

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ABSTRACT

This paper addresses the problem of analog multiplication for analog VLSI implementation, with particular emphasis on multiplication accuracy (low intrinsic noise) and speed.

High-speed low noise analog multiplication for analog VLSI has very important implications in analog signal processing, signal generation, signal detection and ultra precise frequency and phase control.

The various candidate multiplier mechanisms and circuits proposed todate are surveyed and a comprehensive comparison of them developed, leading to the conclusion that the Steerable Localized Injection Multiplier (SLIM) holds the greatest promise for low noise and high speed analog VLSI multiplication.

INTRODUCTION

The true multiplication operation is one of the most important mathematical operations in almost all hardware implementations of systems. Briefly, an analog multiplier in general is a three-terminal device that will perform the mathematical operations of multiplication, division, square root, and others by appropriate terminal connection.

Figure 1 shows a functional block representation of an analog multiplier.

Analog multipliers are available as two-quadrant multipliers and four-quadrant multipliers. Four-quadrant multipliers which are the present industry standard multipliers can accept

inputs of any polarity and produce outputs with the correct sign. These devices make possible analog solutions to analog problems with simplicity, sophistication and low cost.

Mathematically the multiplier provides a natural extension to the analog capabilities of the operational amplifier, But just as operational amplifiers do not just amplify, multipliers do not just multiply[2]. A multiplier, a modulator. a frequency converter and a voltage-controlled attenuator are all really functional variations on a single circuit. Many circuit functions required in communication systems can be derived by way of analog multiplication[3]. Sonic multipliers have extremely wide bandwidths so they can be used in all sorts of RF circuits is well as in their more traditional low frequency applications. A multiplier can be used in a simple wattmeter circuit (that just multiplies voltage by current) as well as in autocorrelation circuits to enhance signal delectability in communications systems. Two or more linear equations may be coupled through a multiplication process. An analog multiplier opens up a whole realm of nonlinear differential equations. True multiplication is a crucial requirement in[4],[5].

- Modulation and Demodulation: These in essence, are multiplication processes. The term “multiplier” and “modulator” are interchangeable in when the time functions are considered to represent signals. Figure 2 models a “balanced modulator” as simply an analog multipliers[6].

- Automatic Gain Control: AGC is used when a constant output magnitude is required, despite variations of the input.

- Cross-correlation: This mathematical operation can be modeled as a multiplier followed by a lowpass filter. The phase difference between two sinusoidal signals can be found by using an analog multiplier with a low-pass filter: the device is then variously known as a phase, synchronous, phase-sensitive, or quadrature product detector or as a quadrature cross-correlation.

- Division, Squaring and Square Root Extraction: Figure 4 shows a block diagram for division using an analog multiplier. The analog multiplier is placed in the feedback loop of an operational amplifier. One input is applied to the multiplier: the other input is applied to the non-inverting terminal of the operational amplifier. Figure 5 shows the conceptual block diagram for squarerooting using an analog multiplier.

  The square-rooting operation is quite similar to that for division. The denomenator is tied to the output to providc its square.

- Voltage Controlled Filter: A voltage-controlled filter can be used for input signal conditioning, when a corner frequency is to be programmed or to be controlled by an incoming signal.

- Function Generation: The multiplier can be used to produce a triangular or a square wave, whose frequency is proportional to the applied voltage. Applications include use in voltage-controlled oscillators, sweep generators, square wave generators and voltage-to-frequency converters.

- Frequency Detection and Translation.

- Tapped Integrator-line Simulation of Linear Systems.

- Tapped Delay Line Simulation of Linear Systems.

- Programmable Signal Processors.

- Adaptive Processing Systems.

- Randomly Time-variant Channel Simulation.

- Adaptive Equalization of Randomly Time-variant Trans mission Characteristics.

- Adaptive Compensation in Feedback Control.

- Array Processing for Antenna Beam Steering, Antenna Null Steering, Spectral Analysis, Signal Sorting, Navigation Aid, etc.

This paper is primarily intended to provide the results of a survey and comparison of analog multiplication techniques with empahasis on analog multipliers using a new class of semiconductor devices-Carrier Domain Devices or CDD- developed by Barrie Gilbert[7],[8]. CDD is a highly versatile class of integrated circuits that can achieve more direct realization of certain signal-processing functions through the use of planar bipolar integrated devices having special lateral geometries but otherwise standard proessing. SLIM (Steerable Localized Injection Multiplier) a particular type of CDD multiplier, is the latest entry in the class of super integrated circuits to perform analog multiplication. and evolves in our discussion as the one with the greatest promise of high accuracy and speed.

Overview of Analog Multiplication Techniques

The central issues in multiplier implementation theory and synthesis are linearity, accuracy. self noise, speed, dynamic range of linear operation and spurious signal generation and effects. There is not a universal multiplier. A circuit that offers wide bandwidth may have excessive noise and vice versa. In general, a total error specification is the best measure of multiplier quality, but certain applications may place a premium on certain components of the total error. For example, if the two inputs to the multiplier always have large values, offset errors would not be significant but gain accuracy would be critical.

Although much work has been done to date, the subject of analog multiplication theory and techniques remains in a rather primitive state, and much remains to be done to expedite the evolution of multipliers that satisfy very stringent requirements on multiplication speed and accuracy over a wide dynamic range of the multiplicands and of the relative instantaneous ratios of multiplicands.

There are several methods used to perform analog multiplication[9][10], namely electromechanical, magnetic (magnetoresistance. Hall effect), triangle averaging, quarter square, pulse height/width, logarithmic sum, variable transconductance and those based on A/D and D/A conversion techniques. Analog multipliers were not being used much in the past because of their high cost. But lately, several manufacturers have been able to produce high-performance, easy-to-implement, low-cost IC units. We may expect to see analog mulipliers boom in much the same way operational amplifiers boomed after the 709 IC was introduced.

Hall effect multipliers are devices that rely on the principle that the voltage across a conductor is proportional to both the current through it and the strength of an external magnetic field across it. Hall devices use a semiconductor material, such as indium arsenide. The advantages of these devices is their simplicity, low cost and small size. Their disadvantages are the limited bandwidth they have, they’re temperature sensitive and not suited for four-quadrant operation because the devices are polarity sensitive.

Mathematically, the circuit for generating triangle averaging technique for analog multiplication is a variation of the quarter-square method which will be described in detail later. Instead of using square-law devices, the circuit generates the necessary quadratic functions by integration of clipped triangular waveform. The triangular wave is derived from a clock oscillator. Multiplication by triangle averaging is characterized by good linearity at low cost, butsuffers from limited bandwidth and slow frequency response.

A/D/A conversion is the most accurate method of analog multiplication. But it is much too expensive for simple analog circuitry.

At present, the two most common means of performing electronic analog multiplication are variable-transconductance and pulse height/width modulation. A third method, log-antilog or logarithmic sum, is gaining in popularity for low-speed high-accuracy calculations.

The highest accuracy is provided by the pulse-width multiplier[11]. Figure 6 shows a block diagram of the pulse-width/height modulation multiplier operation. The average value of a train of pulses is proportional to the product of the pulse amplitude and duration. One input sets the duration of the pulse, V_2, and the other input, V_1, sets the amplitude. The result goes through a low-pass filter which retains only the dc components of the pulse train. The output dc voltage is proportional to the product of the inputs.

The pulse width multiplier has good accuracy and linearity. Because some sections of the circuit can be ac coupled, temperature stability is extremely good. The relatively complex circuitry of the pulse-width multiplier limits its applicability to situations where highest accuracy is absolutely essential. Another drawback of this method is its slow frequency response which restricts it to static applications only.

Recent developments have made it possible for log-antilog multipliers to yield excellent accuracy, approaching that of pulse-width/height multipliers, but with much wider bandwidth, low noise, and reduced cost.

Figure 7 shows the basic operation of the log multiplier. The log-antilog technique utilizes the logarithmic voltage versus current relationship in a semiconductor junction. A product can be obtained by taking the log of both inputs and then the antilog of their sum. Due to the relatively high cost of stable log circuits, this technique is used only when high dynamic range is essential.

Among the techniques used to perform analog multiplication, the variable transconductance has been the only one which has been integrated in monolithic form. This technique takes advantage of the excellent exponential voltage-current characteristics of the junction diode for multiplier applications using pairs of transistors connected as a differential amplifier. This technique makes use of the inherent close matching of transistors fabricated on a single chip and the variable transconductance of the semiconductor junction[12]. It is much easier to design matched transistors and resistors with identical geometries and in close proximity on a single chip of silicon than to select matched pairs of discrete transistors. This ensures excellent tracking of parameters over time, temperature, and supply variations and, at the same time, yields low cost and reliability. The IC variable-transconductance multiplier has advantages over the previously mentioned techniques, namely, good transient response, smooth error curves (i.e..low error for small signals) and low noise. The variable transconductance technique has been

implemented using bipolar technology and has been the dominant one in the analog domain.

The first commercial analog multiplier in modular form utilized the quarter-square technique. This method has gained favor in the field of high-accuracy medium-speed multipliers. This technique is based on the algebraic identity:

$$\frac{1}{4}[(V_1 + V_2)^2 - (V_1 - V_2)^2] = V_1 V_2 \tag{1}$$

Figure 8 shows a block diagram of the quarter-square multiplier. The type of elements employed in this method are elements having bipolar square-law voltage-current characteristics, together with several operational amplifiers to perform the summing and squaring functions. The practical realization uses diode function generators, whose relatively high cost and objectionable breakpoints have made the quarter-square multiplier obsolete after the transconductance multiplier was introduced. Although this technique is used where better linearity is required, its disadvantages are circuit complexity, cost, and poor linearity at low signal levels. This is due to the resistor- diode networks normally used to generate a parabolic transfer characteristic for the squaring operation. An important reason why this technique has not been suitable for monolithic integrator is that large resistor values are required[13].

The principle of variable transconductance was first reported in the 1920's where it was used to perform the AGC function in vaccum-tube receivers. With the advancements in bipolar junction transistor (BJT), integrated circuit technology made possible the practical realization of the variable transconductance multipliers. The first multiplier was proposed in 1968 by Barrie Gilbert to be used as an analog phase comparator in monolithic phase-locked-loops[14],[15]. This multiplier found wide acceptance not only in analog computation, but also in a variety of modern communication and control systems[3]. Where reasonable static accuracy and large bandwidth are required. the transconductance multiplier was found to be the most useful technique. In this circuit, very high bandwidths as well as reasonable multiplacation accuracy can be achieved. One serious drawback with the transconductance multiplier is its poor noise performance.

Ever since the introduction of the first integrated circuit by Kilby in 1958 [16], IC design engineers have been trying to condense more elements of active circuits to achieve greater functional density. Carrier Domain Devices do not quite fulfill the promise of "super-integration" but yet could be considered as just another entry of a collection of very specialized architectures that realize the dream of super-integration.

The origin of the CDD principle lies in the development of analog character generators for oscilloscope displays[17]. The “x” and “y” signals for each stroke in a character were generated by a trio of area weighted transistors all with common base potential as shown in Figure 9. One collector current was used to drive the horizontal deflection, one to drive the vertical deflection and the third provided a scaling factor. The area ratios among the transistors of the trio determined the relative amount of collector current in each and thereby determined the coordinates of the oscilloscope trace. A sequence of strokes was created by connecting the base terminals of several trios to a special resistive ladder, which had a movable potential maximum. As the maximum was scanned from one end of the ladder to the other, the emitter current, I_E, would be steered successively from one trio to the next until the complete character had been drawn on the screen. Although the device was not really a single large transistor, these character generators embodied the essence of the CDD principle.

The first carrier domain device (CDD) was the circular geometry four-quadrant analog multiplier invented by Gilbert and refined by Smith[18]. The geometry of the device shown in Figure 10.

By applying differential currents $(1 - x)I_t$ to contact A and $(1 + x)I$ to contact B where x is a dimensionless input variable in the range -1 to +1, the maximum of potential occurs at an angle

$$\theta_m = \arccos x \qquad (2)$$

where θ_m is measured clockwise from contact A. Injection into the collector will be greatest at $\theta = \theta_m$ and will fall to zero at angles remote to θ_m. Contacts C_1 and C_2 are maintained at the same potential so that the collector acts as a current divider. The emitter strip is at a constant potential and is supplied by a current proportional to the other input variable y. The size of the domain depends on the voltage gradient in the base and is limited by emitter-base breakdown. As the differential base drive is varied, the domain swings around the circumference of the dee. Since the location of the domain follows an arccosine dependence and the current division is essentially a cosine operation, the differential output current is a linear function of the differential input signal. What favors CDD is its flexibility where a limitless variety of transfer functions can be realized by simple modification of geometry.

Gilbert also invented a thin rectangular form of CDD multiplier which he called the “Steerable Localized Injection Multiplier” or SLIM. The main feature of a SLIM is the special property of its parabolic base potential: The position of the peak of the parabola (and hence the domain) is a linear function of the differential voltage applied to the ends of the base. Gilbert devised several ways to generate this parabolic profile. But the most practical technique was the use of a long uniform resistor biased by a uniform current

sheet as in the SLIM. This was accomplished with a wide FET for which the NPN base was the drain, or a lateral PNP with the NPN base served as the collector.

SLIM

Consider an elongated NPN transistor shown in Figure 11. The base region has contacts at each end which are held at potentials of *V*. The emitter region has a contact along its length and is driven by a current I_t. The base region is also subjected to a uniformly distributed current.*I* along its length.

Consider, first, the consequence of feeding a uniformly distributed current into a uniformly-distributed resistor (since the base of an NPN transistor also acts as a resistor). On entering the base, I_{mj} flows to the base contacts at either end. Owing to the high sub-emitter resistance, negligible current flows underneath the emitter, and so, to a first approximation, current flow is one-dimensional in the region between the edge of the emitter and the edge of the base. By means of the one-dimensional form of Poisson's equation, one can show that the effect of the injection current is to produce a parabolic voltage distribution on the base: namely

$$V(x) = \frac{IR}{8L^2}x^2 - \frac{V_i}{L} + \frac{IR}{8} \tag{3}$$

which can be rewritten in the form:

$$V(x) = \Psi(x - x_m)^2 + K \tag{4}$$

where,

$$\Psi = \frac{IR}{8L^2} \tag{5}$$

$$x_m = \frac{4V_iL}{IR} \tag{6}$$

$$K = \frac{IR}{8} + \frac{2V_i^2}{IR} \tag{7}$$

which is a parabola with maximum at $x = x_m$ that is a linear function of the differential input voltage V_i, and inversely proportional to injected current *I*.
Equation 4 shows clearly that the potential profile is symmetrical around its maximum. Equation 6 indicates that an input voltage magnitude of $\frac{IR}{4}$ is required to move the peak all the way to one end of the base. The location, x_m of the maximum is therefore linearly related to the bias voltage V_i, and reaches $\pm L$ for $V_i = \pm\frac{IR}{4}$.

How does this voltage in the base region affect the injection of minority carriers from the emitter? Clearly, injection will he heaviest where the base is most positive This is referred to as emitter current crowding [18][19]. But there is a difference here. Emitter current crowding is caused by recombination current, which is to a large extent uncontrollable, and results in the unwanted restriction of current to the edges of the emitter, where the voltage drop is least. This localization of injection serves no useful purpose. In SLIMs, the whole operation depends on forcing injection to a particular locality on the emitter, by means of the parabolic base- voltage distribution, and of making use of this localization. which is now “read out” by the use of a long, resistive collector resistor, usually formed by a thin buried-layer diffusion[20].

Since the NPN emitter is current driven(see Figure 11), the emitter voltage will settle to approximately $0.7V$ below the maximum base potential, and emitter injection will occur around the position of x_m. This localized current flow within the transistor is called a current domain.

The emitter potential is uniform at a value that is only a fraction of a volt below the peak base voltage. By increasing RI, the base parabola will become steeper, the domain will become narrower, but the maximum reverse bias on the emitter (when the domain is driven to either end) will also increase. Since emitter-base breakdown limits the reverse bias to about 6 volts, the RI product is limited to about 12 volts. This puts a lower bound on s and defines a minimum size for the domain. If the size is considered to be the distance between points where the current density is half the maximum, the domain can be no smaller than about 10% of the device length.

The domain width Γ_0 is defined as the fractional length along the device between the half current amplitude points at constant temperature, the width of the domain is inversely proportional to the root of I_{inj} which will be refered to as V_{inj}.

SLIM as a Multiplier

The magnitude of the domain and its position can be altered independently of one another. It is this property that will enable this device to be used as an analog multiplier. Magnitude and position of the domain can be used to represent the variables X and Y in a multiplier whose output is a function of XY.

The position of the domain within the base is detected by allowing it to inject into an elongated buried collector region. The differential output current taken from each end of the collector is a function of the domain position.

The domain acts as if it is a point source of current injecting into the collector region at a position, x_c, coincident with its centroid. Thus when the domain is near the middle of the base, x_c is proportional to the applied differential base voltage. As the domain approaches the device ends, however, the domain becomes distorted and x_c is no longer proportional to the base voltage since x_c and x_m no longer coincide. Thus for linear operation, there is a maximum allowable domain excursion which depends on domain width and hence on V_{inj}.

There are two methods which can be used to derive the uniformly distributed current, I_{inj}. The first method is to make the base of the elongated NPN transistor also form the collector of a lateral PNP transistor which is current driven. However, this arrangement is not very satisfactory owing to poor linearity [21],[22]. These devices are given the name "enhanced CDD" since there is a spatial positive feedback between the base voltage profile and the (non-uniform) injected current profile. The effect of this is to sharpen or enhance the domain current profile.

A second method is to make the base region the drain of an FET (usually a JFET), and it is this arrangement which we shall consider. These devices have no feedback effects and the injected current is uniformly distributed. Figure 12 shows a plan view of a non-enhanced CDD using a p-channel JFET as the source of uniformly distributed current I_{inj}.

The cross section of the device is shown in Figure 12. where a p-type layer forms the source of the FET and the drain which is also the base of the pnp transistor. The gate and npn emitters are formed by two *n* diffusions. The base/drain region has contacts at either end to which the domain steering voltages can be applied. Differential output current is taken from each end of the buried layer collector region.

If the JFET is operated beyond pinch-off and its source is current driven, then it injects a uniformly distributed current into the drain/base region and this produces the required voltage profile necessary for domain formation. Also, since there is no current flow across the reverse-biased gate-source junction, I_{inj}, is numerically equal to the source driving current [23].

The SLIM layout is shown in Figure 13. The basic structure has already been described, but note that each npn transistor has two JFETs injecting current into the base. The purpose of this is to reduce the effects of lateral current crowding in the very high resistance sub-emitter region. FET current is flowing in laterally, in the positive and negative "y" direction, and NPN current is flowing vertically, in the "z" direction. FET is biased so that the current arrives at the drain in a uniform sheet. Assuming that the base current of the vertical NPN is negligible, the NPN base can be considered to be just a long resistor, contacted at the ends and biased by a distributed current source as shown in

Figure 14. The collector buried layers in the two CDDs are connected in parallel on the chip to give the two differential current outputs.

The complete multiplier has dimensions of 900μ x 300μ and is fabricated by standard planar diffusion processes.

Figure 15 shows voltage distributions along the x-axis for the different regions of the device. The gate voltage of the FET is fixed and the source floats at a slightly more negative voltage, such that V_{GS} is appropriate for the chosen source driving current.

Note that V . varies considerably along the length of the device and one must ensure that this voltage is always large enough to produce saturation of the JFET. The upper limit of V_{DS} is set by avalanche breakdown of the gate drain junction. This typically occurs at 7.6V for the SLIM, while a typical pinch-off voltage for the onset of saturation is 3V. Thus the base (drain) voltage cannot vary by more than 4.6V. In other words, the maximum allowable differential base voltage. V_B, is 2.3V.

The domain width is roughly 12.5% of the total device length and thus one would expect the x-input to reach values of $x = 0.75$ before non-linearity becomes severe. However, nonlinearity does appear before this value is reached owing to the fact that the FET output resistance in saturation is not infinite. This means that the injected current is not uniform along the device length and hence the base voltage profile deviates slightly from the required parabolic shape[24].

Conclusions

The greatest obstacle to the wide use of the SLIM is its linearity. SLIMs are very sensitive to end effects and therefore inherently less linear than the translinear multiplier. The intriguing feature of a SLIM is the special property of its parabolic base potential: The position of the peak of the domain is a linear function of the differential voltage applied to the ends of the base.

A primary feature that SLIM possesses is the emphasis on designing in terms of the medium rather than in terms of devices. The implication of this is that devices may be designed free from performance variations due to operating conditions or processing variations which influence the forward active characteristics of the inherent npn or pnp structure. This offers a method of device fabrication in which the single most important parameter is also the single most controllable processing parameter, i.e., the planar geometry of the device design. It is hoped that this work has added impetus to the seemingly small interest in distributed planar devices.

The non enhanced CDD multiplier (SLIM) could find wide acceptability in applications where low noise and wide bandwidth are essential. One such application is a low noise gain control system used in professional sound recording studios. Satellite and deep-space probe systems (data transmission and range-rate tracking systems) stand to gain very significantly in sensitivity and metric accuracy by the availability of a low-noise density microdevice.

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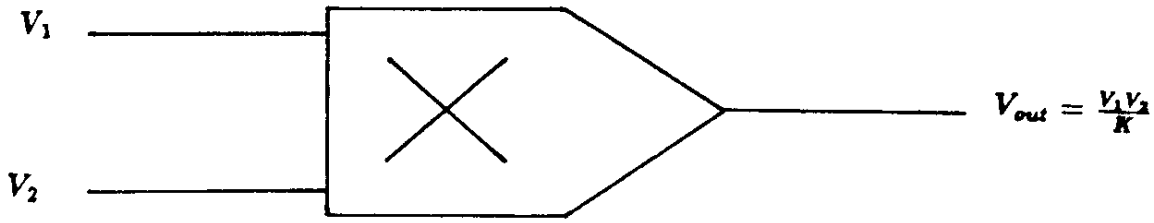


Figure 1: Functional Block diagram of analog multiplier

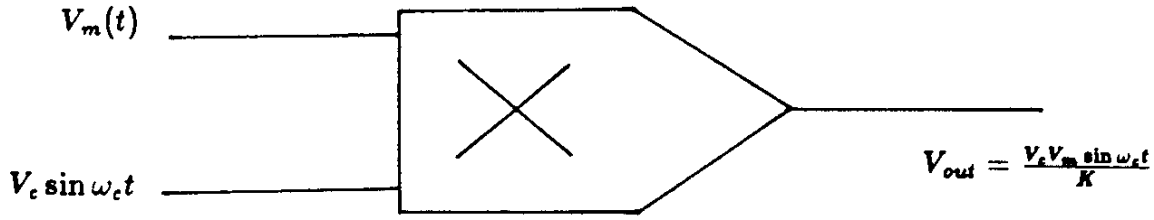


Figure 2: Multiplier as Balanced Modulator

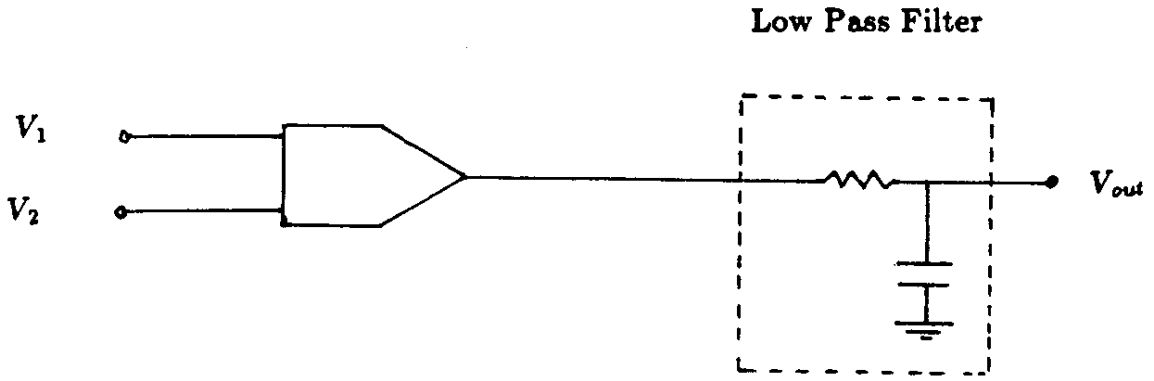


Figure 3: Block diagram for Phase Detection

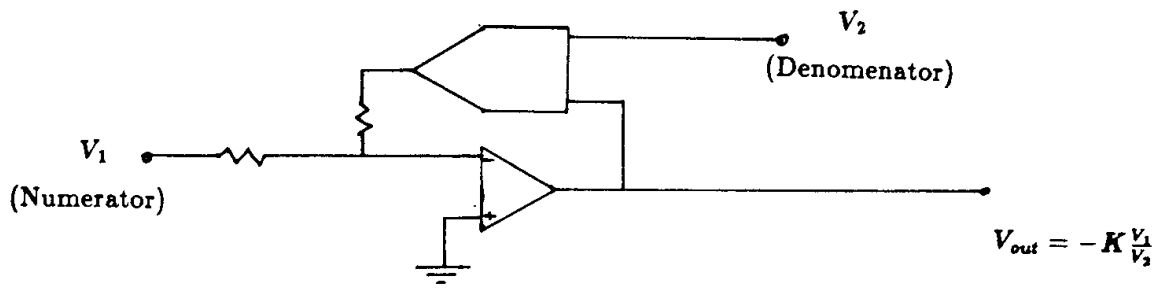


Figure 4: Block diagram for Division

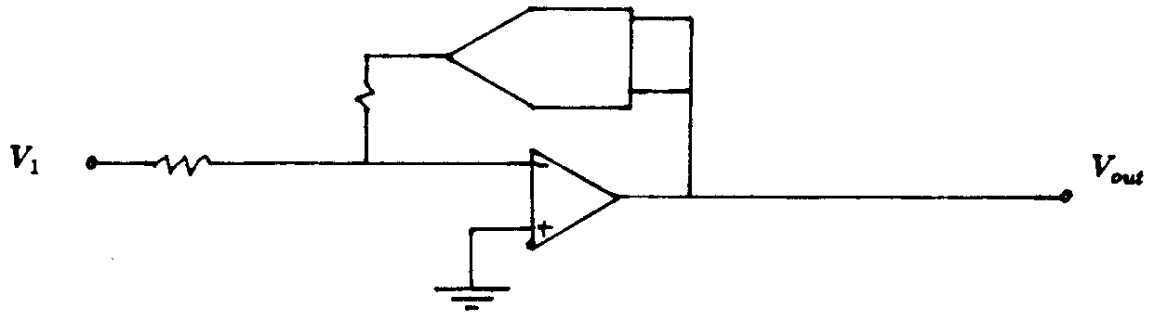
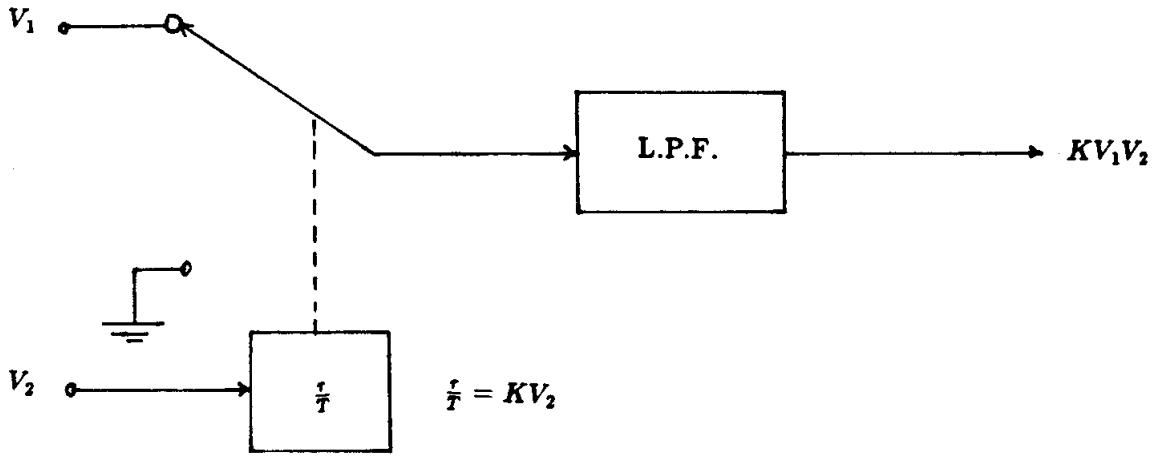


Figure 5: Block diagram for Square-Rooting



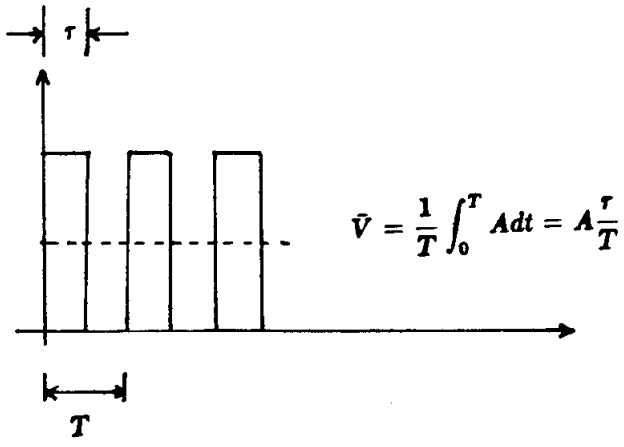


Figure 6: Pulse-width multiplier block diagram

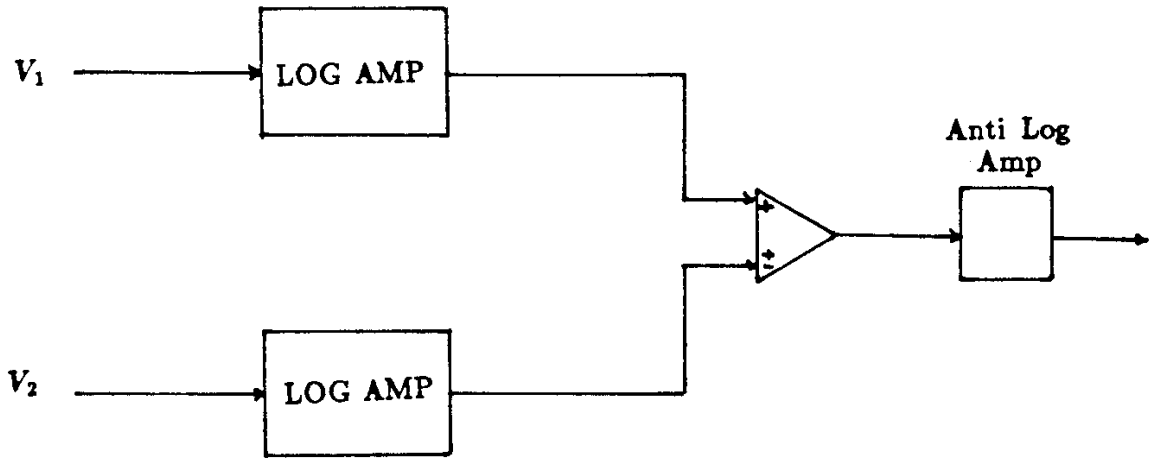


Figure 7: Log-antilog multiplier

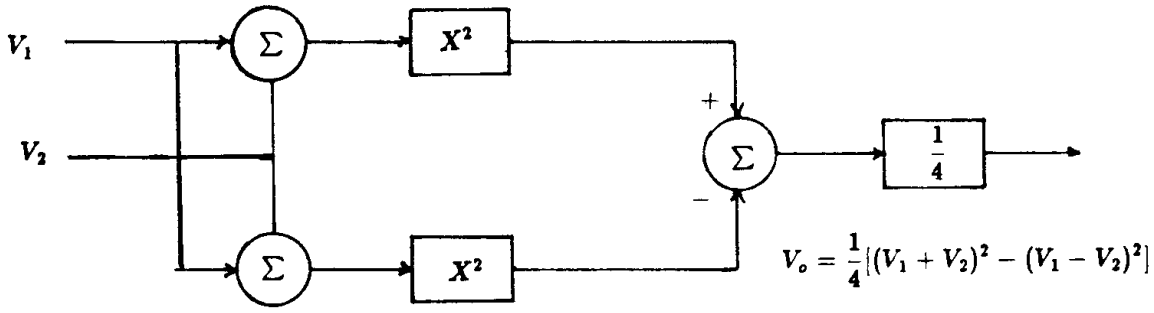


Figure 8: Block diagram of a quarter-square multiplier

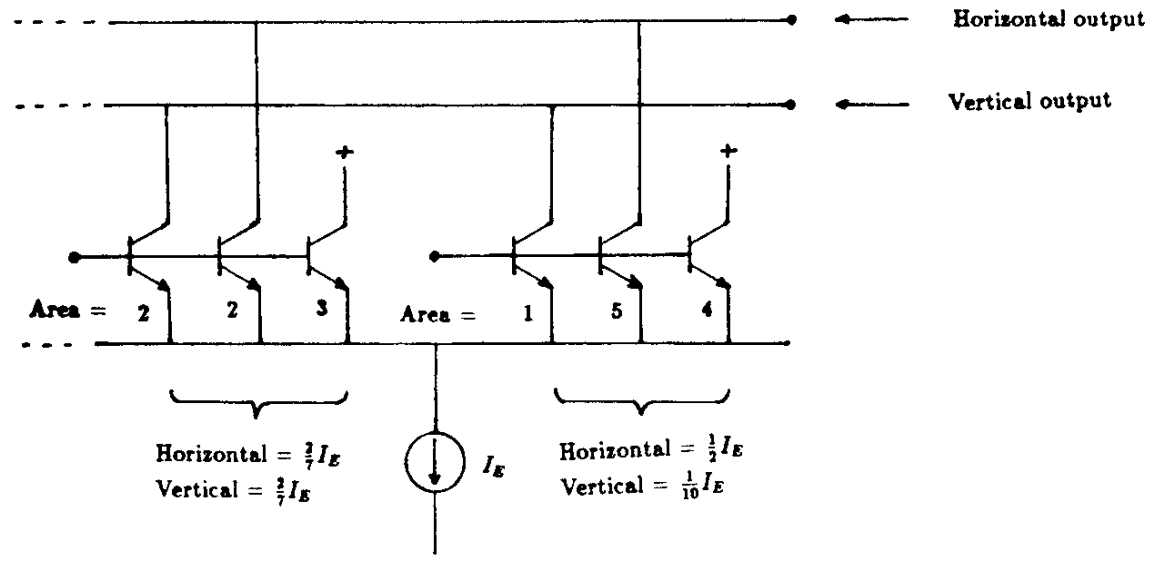


Figure 9: Character generators

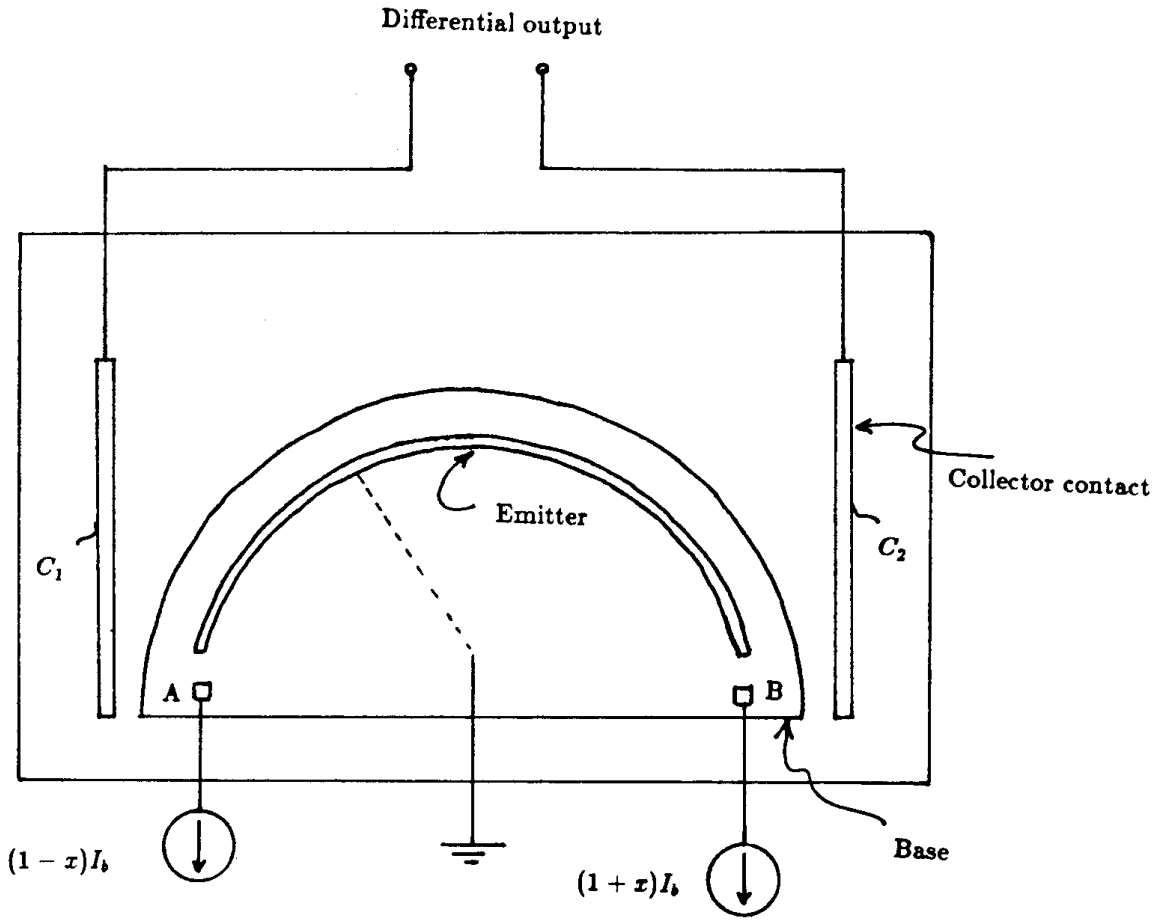


Figure 10: Layout of the basic CDD multiplier

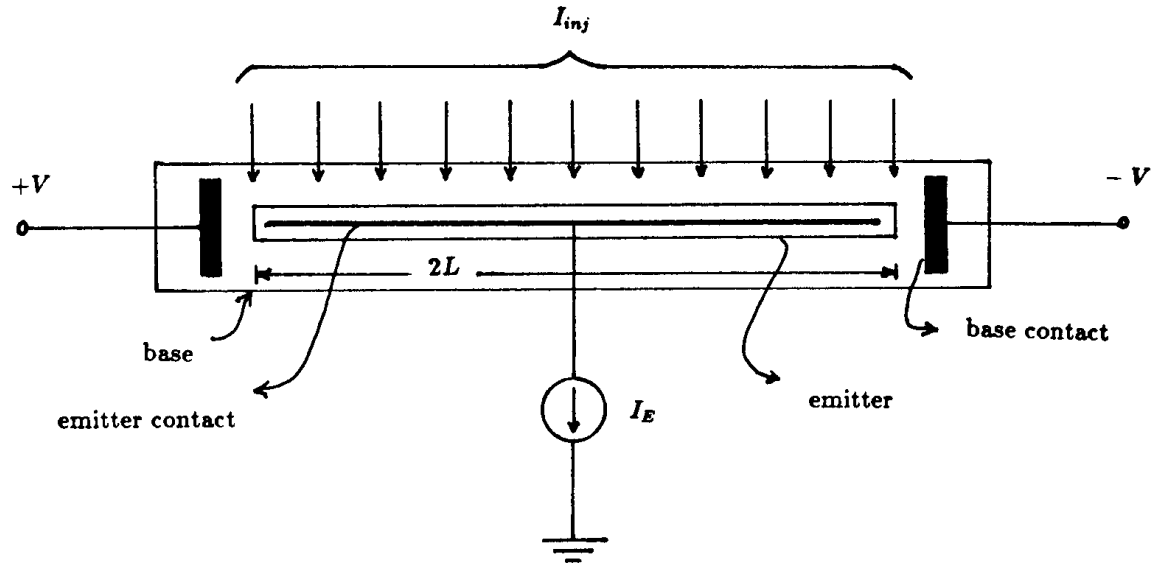


Figure 11: Base and emitter of SLIM

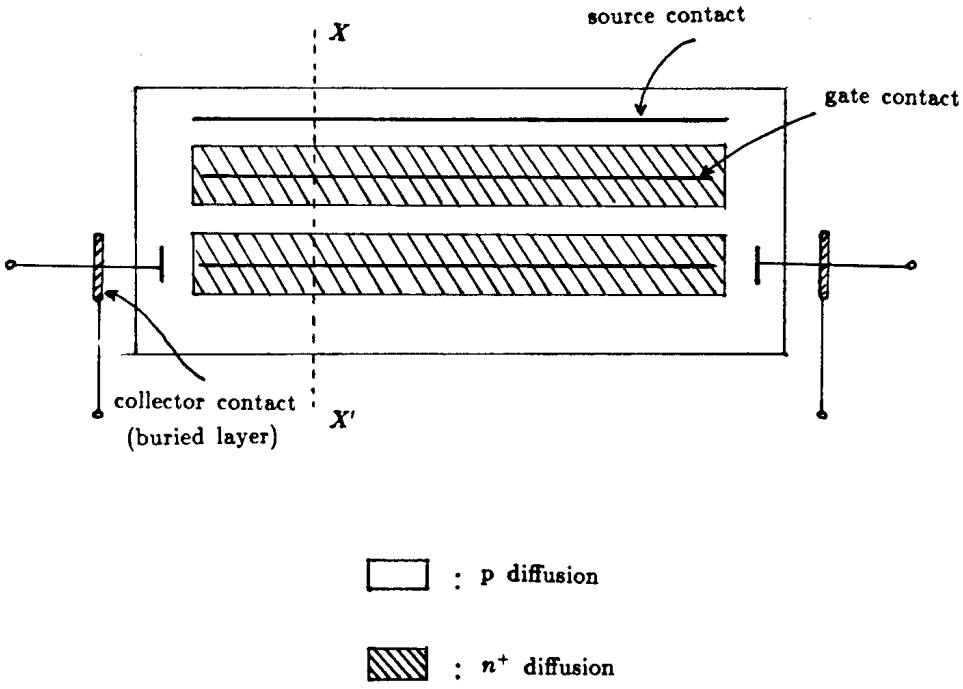


Figure 12: Structure of an non-enhanced CDD

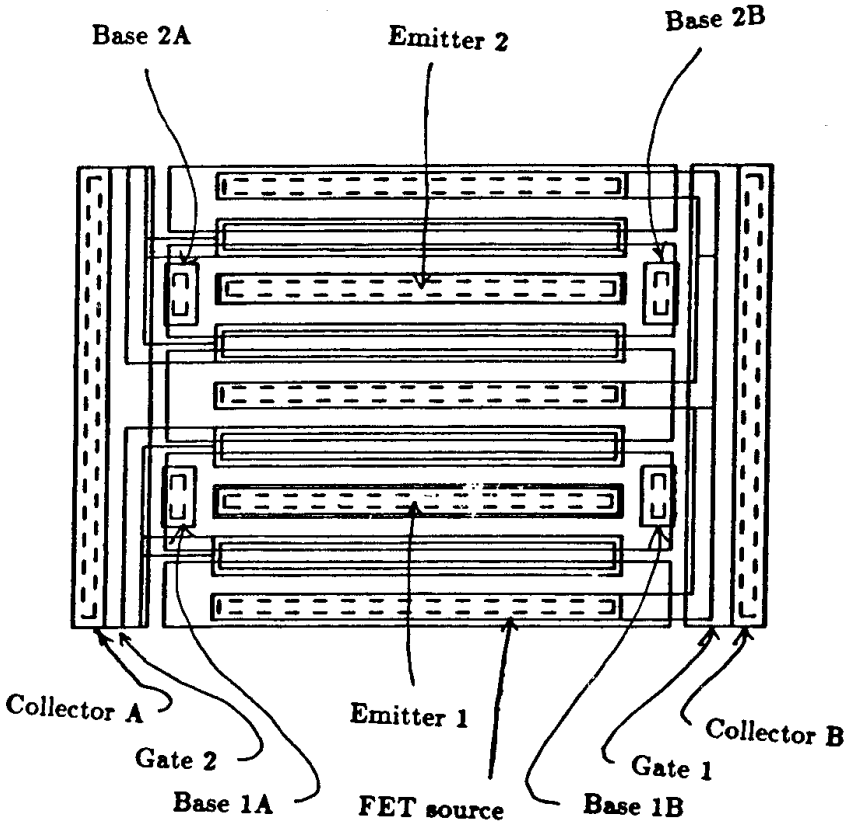


Figure 13: Typical SLIM layout

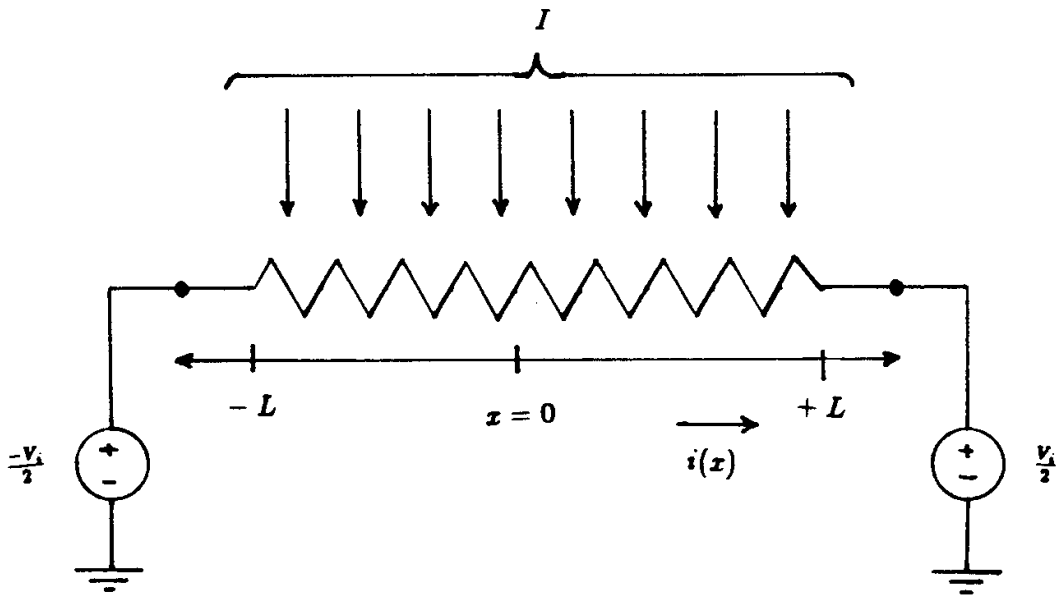


Figure 14: Distributed current source bias

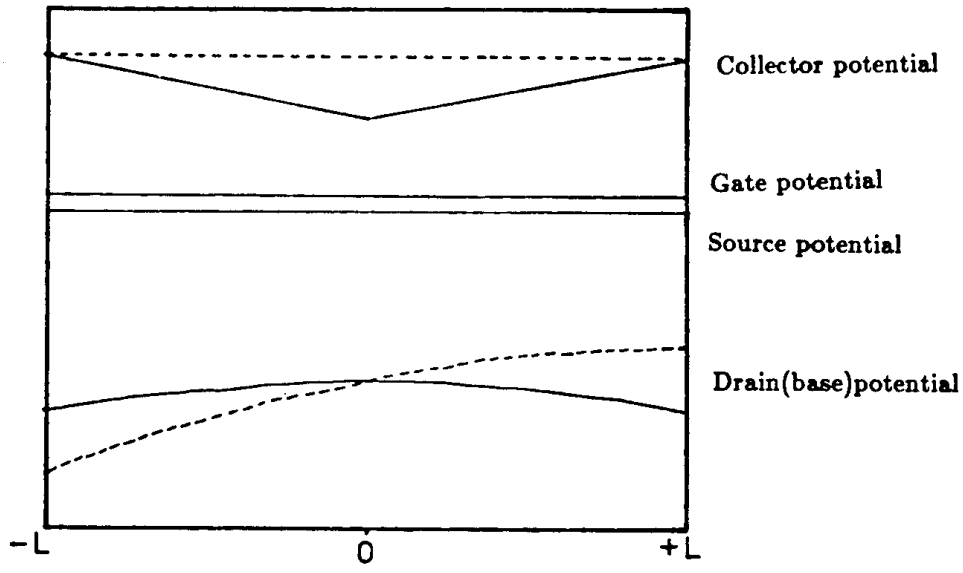


Figure 15: Typical voltage distribution along SLIM