A MISSILE INSTRUMENTATION ENCODER

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ABSTRACT

The modern Pulse Code Modulation (PCM) telemetry system faces many unique challenges in terms of data acquisition diversity and specifically satisfy the demanding missile requirements. The engineering considerations and hardware implementation are presented in this paper.

INTRODUCTION

The PCM-480 Pulse Code Modulation Encoder, developed by Loral Data Systems, under contract to General Dynamics, Convair Division, San Diego, addresses some of the prime concerns associated with encoders today.

Two of the most fundamental requirements in missile encoder design are physical size and power consumption. Packaging techniques were developed to insure minimum wasted space while maintaining the ruggedness required for reliable operation within a missile. By including some signal conditioning within the encoder, additional space within the missile was saved.

The PCM-480 Encoder is a high reliability unit with a Mean Time Between Failure of 48000 hours. Aside from the standard high accuracy analog inputs operating with a programmable gain amplifier, and the discrete bi-level inputs, the encoder has many other attributes. The encoder includes both Serial and Parallel Computer Interfaces, Master/Slave capability, a Frequency Counter, Block Data, two formats, two bit rates, Accelerometer signal conditioning, and High frequency inputs.

SYSTEM DESCRIPTION

Refer to Figure 1, System Block Diagram. The Power Supply used in the PCM-480 is a linear regulator, followed by a DC/DC converter. EMI filtering on the inputs and outputs of the supply maintains the conducted emissions and conducted susceptibility well within MIL-STD-461A limits. The Power Supply is synchronized to a multiple of the system word rate to insure that the switching occurs at a controlled interval. The system was designed primarily with 4000 series CMOS and HCMOS to minimize power consumption.

The Bit Rate Clock is derived from a crystal controlled oscillator in order to maintain a tolerance of 0.01%. An external programming pin selects one of two bit rates.

The Program Control stores the desired output formats and generates the commands necessary to control the channel sampling sequence. An external programming pin selects one of two output formats. The Program Control also supplies the Remote Interface, all of the necessary synchronizing signals required to control slave encoders.

The Analog Multiplexer section contains 64 single-ended inputs and 16 differential inputs. The conditioned outputs of the Analog Multiplexer are routed to a multiplexer on the Analog to Digital Converter. Other analog signals that are routed to this multiplexer are accelerometer inputs and the High Frequency channel inputs. From this multiplexer, these analog signals are fed to a sample and hold, and then to a 10 bit Analog to Digital Converter. The digitized analog signal is fed to an output multiplexer for incorporation into the serial data stream.

The Bi-Level Multiplexer is capable of handling 50 discrete inputs. These inputs are 0-35 volt inputs having a threshold of 1.5 to 2.0 volts. The output of the Bi-Level comparator is routed to the digital bus multiplexer. This multiplexer combines all the digital information prior to routing to the output multiplexer.

Another input to the digital bus multiplexer is the Parallel Computer Interface. Computer data is routed to the digital bus multiplexer when the PCM clock has been phase-locked to the computer clock.

The Serial Computer Interface loads the data into the system using the computer clock. This data is then fed to the digital bus multiplexer.

Digital Scene Mapping and Correlator (DSMAC) Data, is stored in a buffer register until ready to be formatted into the system output. The output of this register is another input to the digital bus multiplexer.

A Frequency Counter output and data from the remote encoders are the last of the inputs to the digital bus multiplexer.

The output of the digital bus multiplexer is routed to the output multiplexer. At this multiplexer, the analog, digital, synch words, and sub-frame ID, are interleaved into the output NRZ-L bit stream. This data stream is also fed to a Random NRZ-L generator, and a six-pole Bessel filter. The output of the filter is fed to a programmable gain output amplifier.

COMPUTER INTERFACES

PARALLEL COMPUTER INTERFACE

The Parallel Computer Interface was designed to operate with the Guidance Computer on the Tomahawk Missile. The Interface accepts data from 16 parallel input lines, and inserts the data into the output PCM bit stream.

A Phase-Lock Loop in the encoder, locks the PCM system to the computer clock. The computer sends a Time Pulse to the encoder every other minor frame (every 20 ms.). Fifteen milliseconds after the Time Pulse is received, the encoder sends out eight Data Request Pulses to the computer. Upon receipt of each data Request Pulse, the guidance computer responds with valid data on sixteen parallel input lines. If the PCM system loses the external computer clock, the appropriate data word is filled with alternating ones and zeroes.

Refer to the block diagram of the Parallel Computer Interface Figure 2. The system receives a Time Pulse via a differential line receiver. There is a fifteen millisecond delay between receipt of the pulse and generation of eight Data Request pulses to the computer via a line driver.

After each Data Request pulse, the encoder loads data from the 16 parallel input lines. This data is converted to serial form and sent to one of two 128 bit storage registers. While one of these registers is being written to, the other is available to be read. The Time Pulse is utilized to switch between storage registers. A clock select circuit routes the read/write clocks to the proper storage register. Loss of data during the receipt of the Time Pulse is precluded by the clock select circuit.

The storage register output is multiplexed with a flip-flop that generates an alternating one-zero pattern. 128 data bits are loaded into the registers every other minor frame. There are 70 bits per minor frame allocated for this data. The encoder inserts 64 bits of data into each minor frame, and alternating ones and zeroes in the remaining 6 bits per frame.

In the event a loss of computer clock is detected, the system inserts alternating ones and zeroes. This is accomplished by switching the output multiplexer from data to the one-zero pattern generator.

SERIAL COMPUTER INTERFACE

The Serial Guidance Computer Interface (see Figure 3), is capable of receiving 48 bits of serial data every minor frame. An Interrupt Pulse is issued by the encoder three times per minor frame. The computer responds to the Interrupt Pulse by issuing a 16 bit wide Data Enable Pulse simultaneously with a 16 bit data word. In the event no Data Enable signal is received by the encoder within 1500 microseconds after the Interrupt Pulse is issued alternating ones and zeroes are inserted in the output data stream. There are 70 bits allocated for computer data in the output format and 48 bits received each minor frame. The remaining 22 bits are filled with alternating ones and zeroes.

DSMAC COMPUTER INTERFACE

The Digital Scene Mapping and Correlation (DSMAC) computer output consists of a serial data stream arranged in a frame format consisting of 41 frames that each contain 23 words for a total of 15088 bits at a rate of 96 kbps. The major challenges involved in designing the DSMAC interface are described below and include the considerations

1. Satisfying the PCM encoder output rate of 10 kbps with an input of 9.6 kbps.
2. Synchronization of input clock with 0 acquisition time and maintaining synchronization throughout 1-3 frame sequences (max 4.72 seconds)

Satisfying the 10 kbps output rate was accomplished by utilizing a 64 word deep first in first out (FIFO) buffer (see Figure 4). At the beginning of each DSMAC frame a circuit initialization occurs during which all input/output counters and buffer counters are preset, and also, circuitry responsible for inputting data to the FIFO is initialized. Output circuitry is initialized when the FIFO buffer fills and data begins to be outputted from the buffer. Clock synchronization is maintained throughout the major frame by refreshing the clock divider circuits on each falling edge of the input data.

PHASE-LOCKED LOOP

To satisfy the requirements imposed by the various computer interfaces, the PCM encoder is required to operate phase-locked to a 640 kHz external clock, or in an internal free running mode with a bit rate stability of 0.01%. This stringent bit rate stability required the system clock to be crystal controlled (see Figure 5). Operation of a phase-locked loop was achieved by manufacturing the crystal with a large output capacitance to

input capacitance ratio (Co/Ci). This allows the crystal frequency to be pulled. A Co of approximately 0.009 pf. resulted in the ability to pull the crystal by approximately +/- 0.05% which satisfied the phase-locked loop tracking requirements of 0.01%. A crystal frequency of 13.824 MHz was required to produce all of the various encoder clocks.

The phase-locked loop was implemented with a monolithic phase detector that utilizes a transition activated phase/frequency comparator that produces up/down commands for a charge pump ultimately resulting in the generation of an error voltage. This error voltage is filtered and used to drive a voltage controlled multivibrator. The free running mode is accomplished by replacing the filtered error voltage with a temperature stable DC reference.

ANALOG INPUTS AND SIGNAL CONDITIONING

The Analog Multiplexer (see Fig.5), accepts 16 differential inputs and 64 single-ended inputs. The differential inputs are routed to the inputs of a differential programmable gain instrumentation amplifier (PGA) via Metal Oxide Semiconductor Field Effect Transistor (MOSFET) gates. This PGA has two gain settings. The current configuration has input ranges of +/- 10 volts, and 0-50 millivolts. The output of the PGA is directed to another multiplexer on the Analog to Digital Conversion board.

The Single-Ended channels are also sent through MOSFET gates. These channels are multiplexed a second time and then sent to a single-ended PGA. This PGA has three gain and two offset settings. The present configuration has input ranges of 0-10 volts, 0-5 volts, +/- 10 volts, and +/- 5 volts. The output of this PGA is also routed to the multiplexer on the Analog to Digital Conversion board.

These analog inputs are accurate to +/- 0.2% full scale over the temperature range of -54 C to +70 C.

There are three types of signal conditioning contained within the analog multiplexer.

Termination resistors - These resistors were required to allow signal inputs of up to 50 volts to be accepted by the encoder.
Half-Wave Rectifier - This was needed to monitor computer AC power.
Single and Differential Thermistor Inputs -These inputs are supplied by a stable, high accuracy, constant current source.

As shown in Figure 1, the encoder also contains a frequency counter. The counter will recognize signals from 0.1 volts peak-peak to 12.0 volts peak-peak. The frequency range

of the counter is 900 to 10230 Hz. The counter is implemented such that it measures the input frequency for 10 minor frames (0.1 seconds), then outputs this reading in the data stream. This measurement is latched and outputted in the data stream while the next measurement is being made.

Each of the three high frequency analog channels consist of either accelerometer data or high frequency analog data. The accelerometer input is compatible with an accelerometer having a frequency response of 5,500 Hz and a sensitivity of 11.5 coulombs/g. The high frequency analog channels receive signals that are +/-5 VP-P (max) with the HF analog channel. The two channels are then summed with the inactive channel input grounded. The output is filtered by a 6-pole Butterworth filter with a cutoff frequency of 2 kH

MECHANICAL DESCRIPTION

The PCM-480 assembly consists of a housing (see Figure 8), interconnect (mother) board, power supply, and six sub-assemblies (Digital Mux, Analog Mux, A/D Program Control, Guidance Board, Randomizer, and Input/Output Board). The dimensions are 6.00" X 4.50" X 2.25".

The housing section consists of a center section and front and rear covers. The entire housing is machined from 6061-T6 aluminum alloy with a 63 microinch machine finish.

Slots are cut into the center section as sub-assembly guides, to hold the sub-assemblies in position and to help dampen resonant frequencies. The six assemblies are assembled in board pairs by .25 inch standoffs. Each pair is attached to the center section by a stiffening bar at the top.

The power transformer, pass transistor, and drive transistor, are heat sunk to the power supply interface cover for better heat transfer. The complete assembly is contained within its own enclosure to attenuate any possible sources of noise in the power supply.

The external interface connectors used on the unit are the ITT Cannon MDM series. These connectors are designed to meet the severe environments encountered in missile/aerospace telemetry requirements.

CONCLUSIONS

The design of the Loral PCM-480 does solve a number of missile/aerospace telemetry problems. Power consumption was held to a minimum by the use of CMOS circuitry creative design techniques. Reliability was maintained by the use of high reliability parts and additional derating criteria. Maximum missile space was assured by including a large number of signal conditioning circuits in the encoder and packaging the unit in a manner that precluded wasted volume.

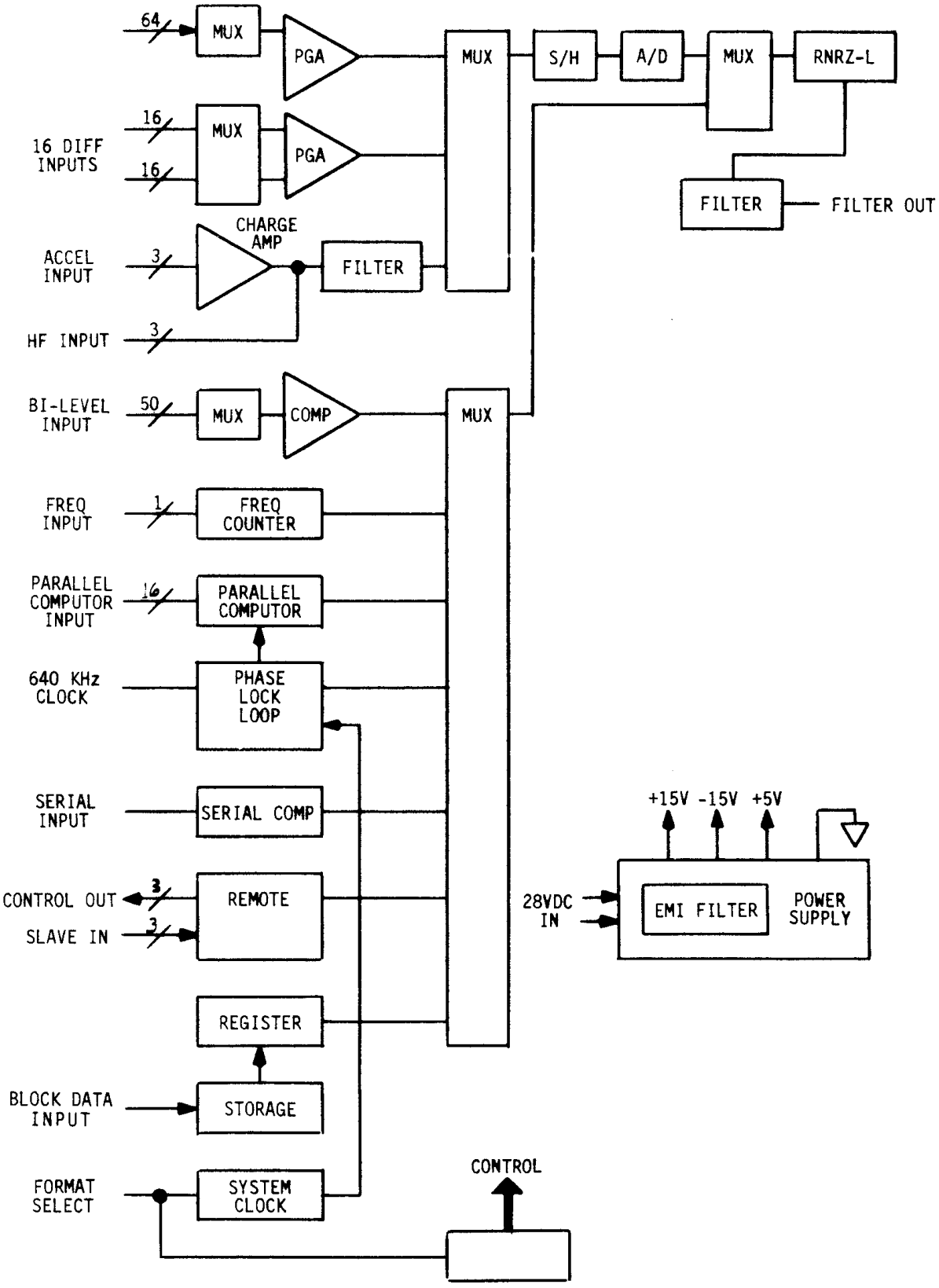

FIGURE 1
SYSTEM BLOCK DIAGRAM

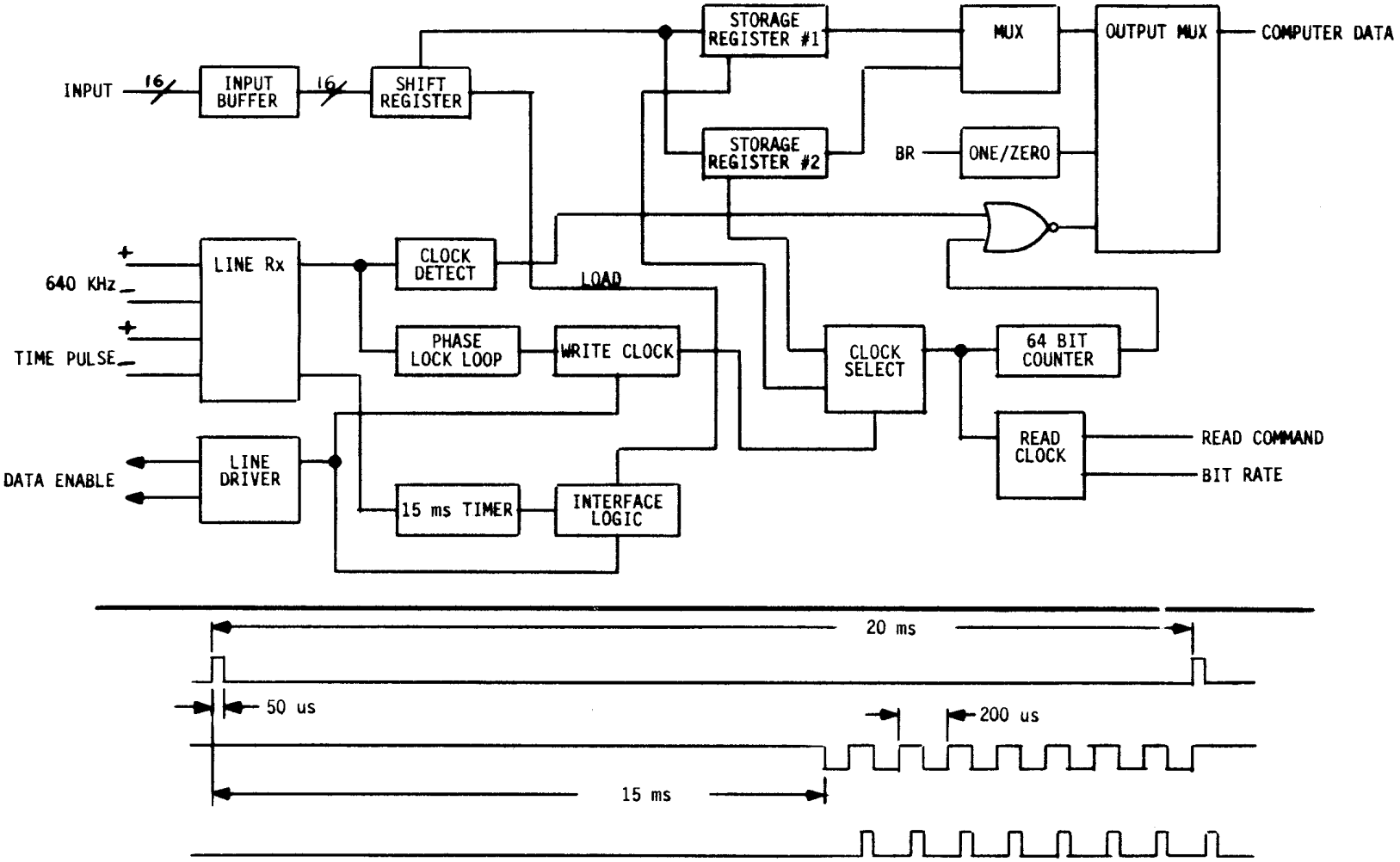

FIGURE 2
PARALLEL COMPUTER INTERFACE AND TIMING DIAGRAM

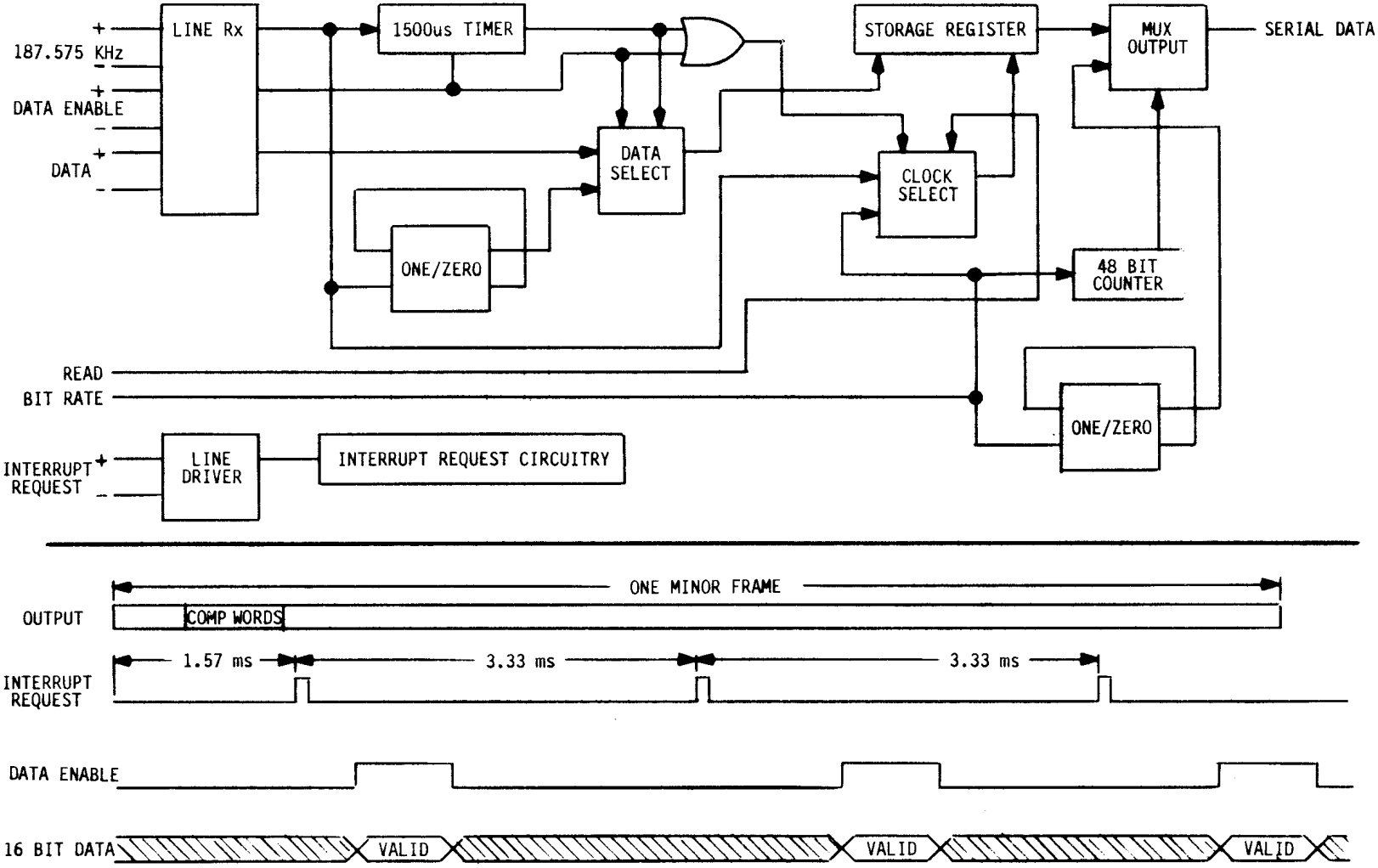

FIGURE 3
SERIAL COMPUTER INTERFACE AND TIMING DIAGRAM

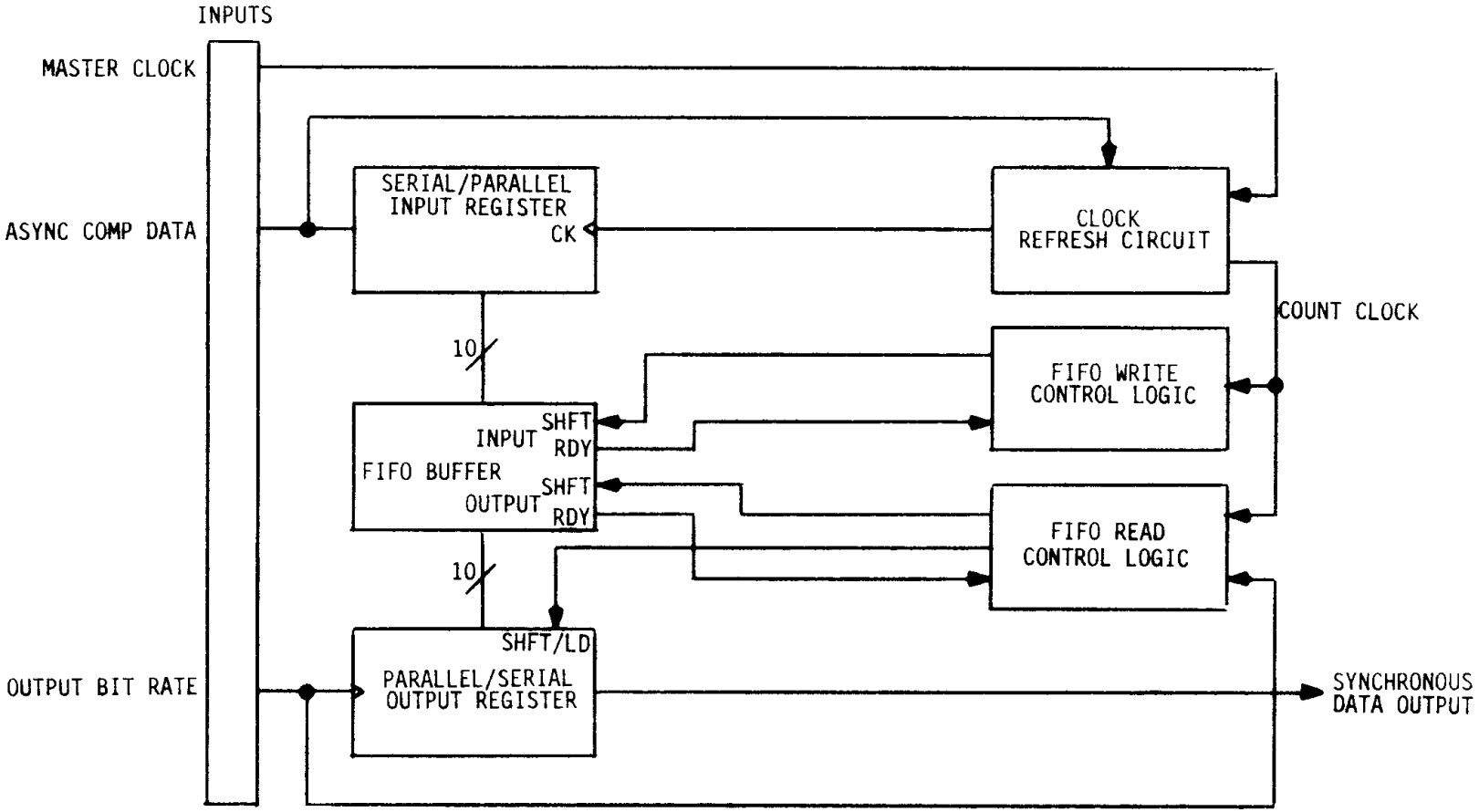

FIGURE 4
PCM 480 ASYNCHRONOUS DSMAC COMPUTER INTERFACE

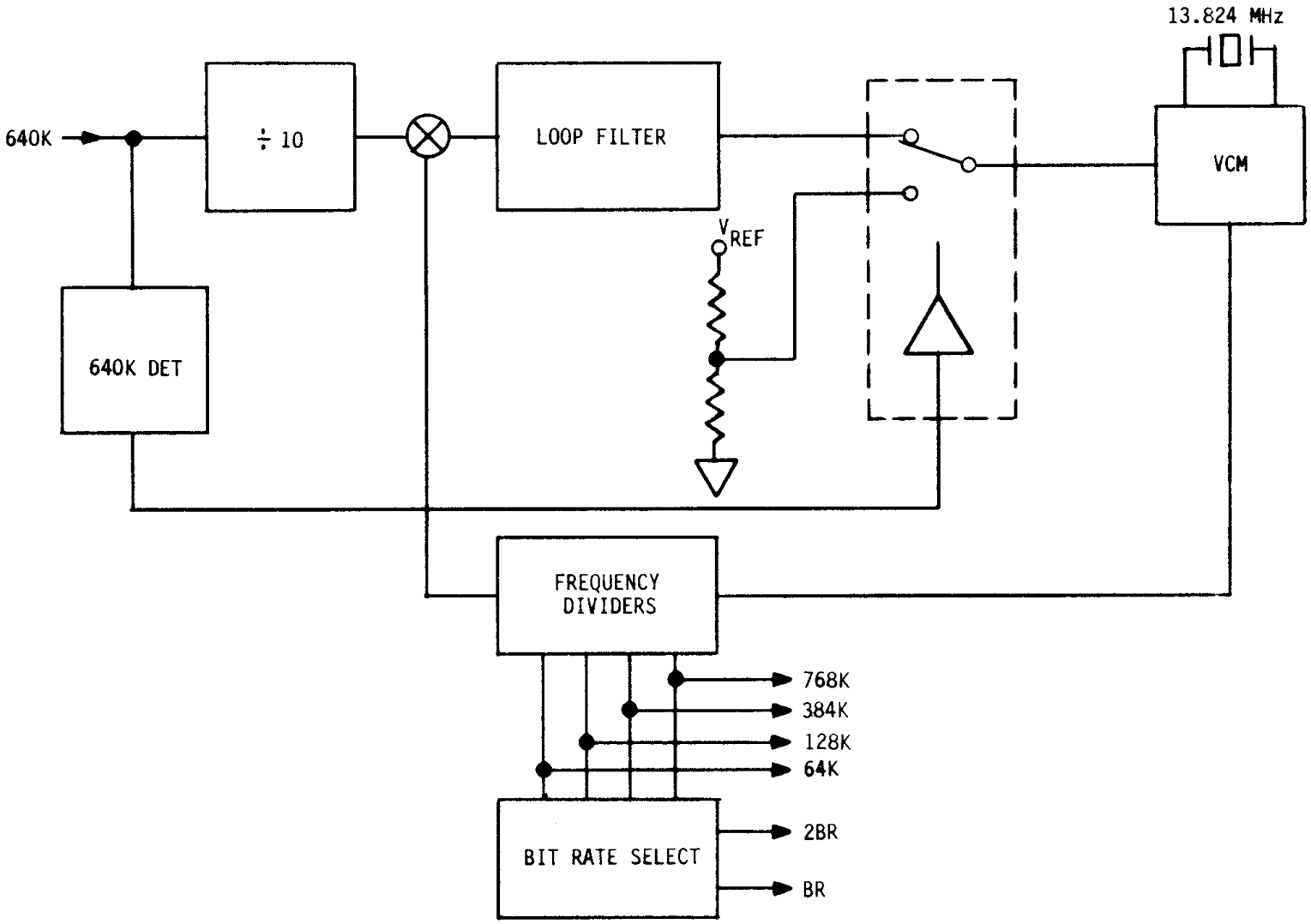

FIGURE 5
PHASE LOCKED LOOP & SYSTEM CLOCK GENERATION

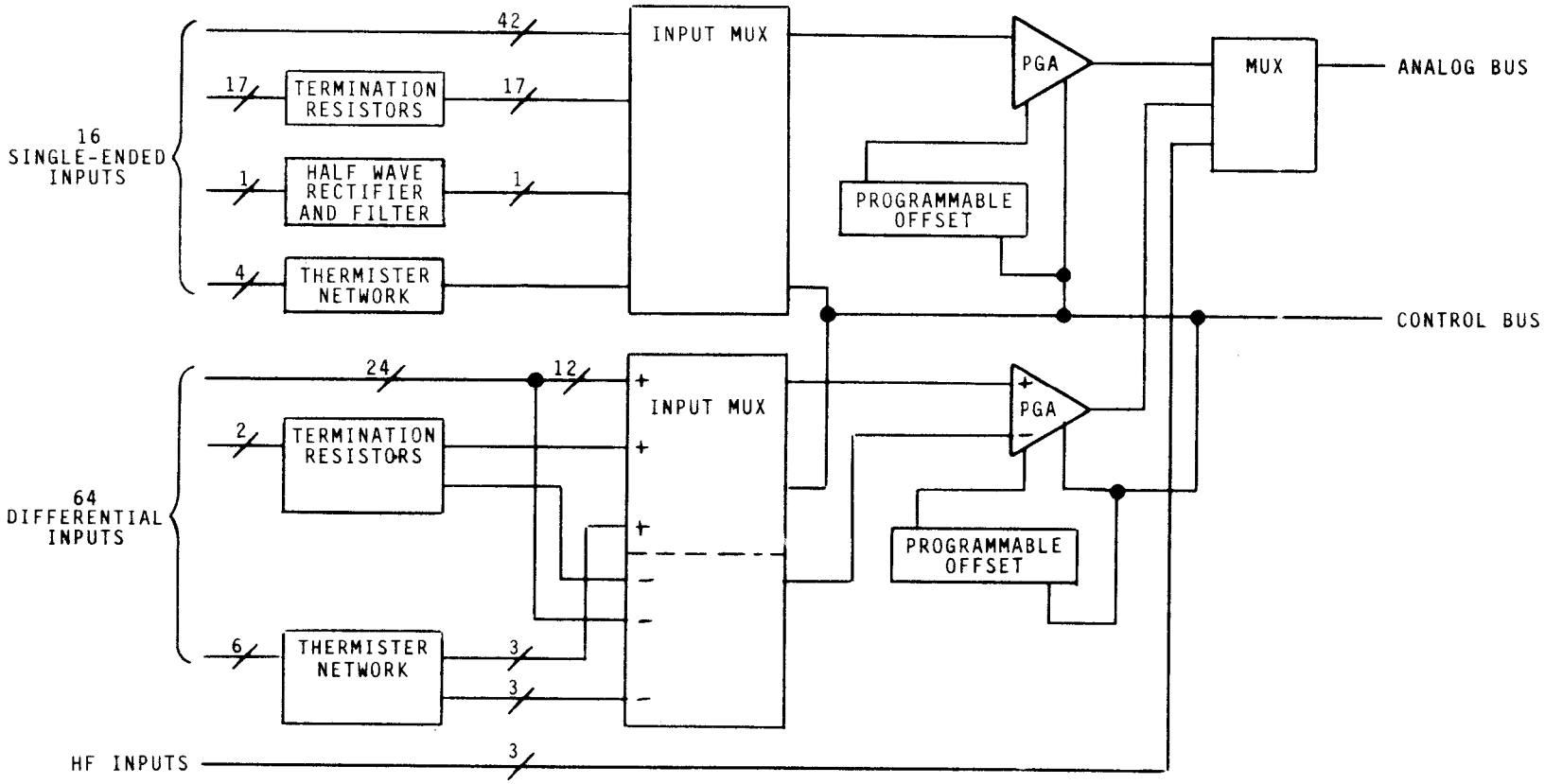

FIGURE 6
ANALOG MULTIPLEXER

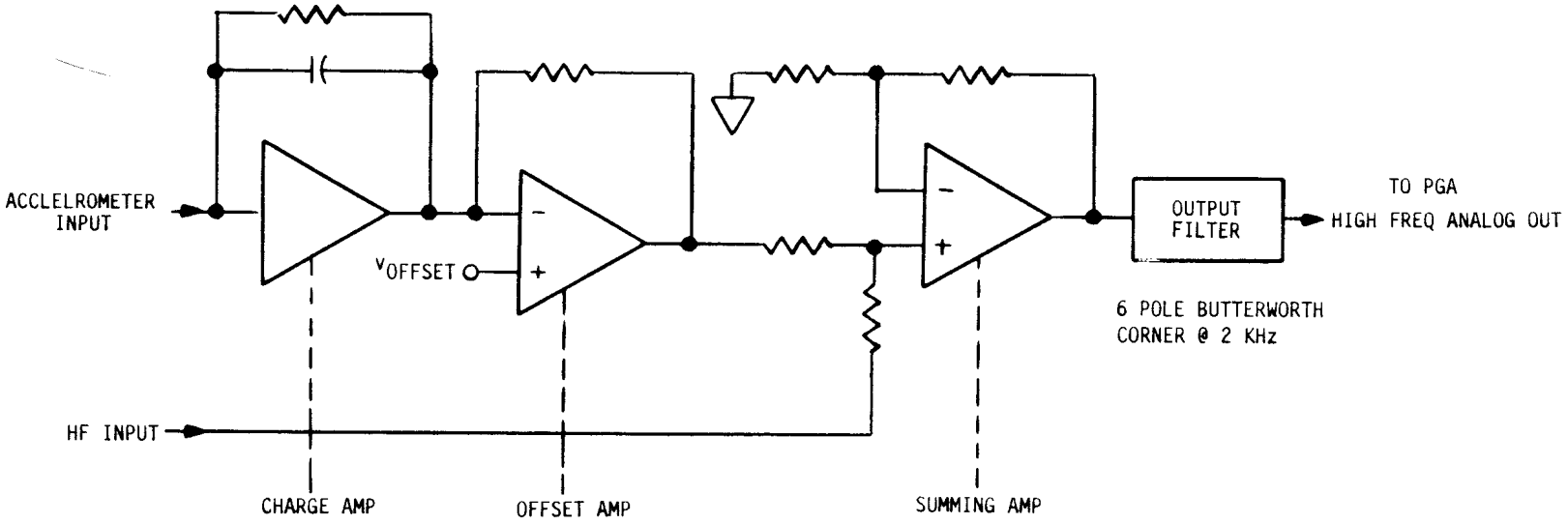

FIGURE 7
HIGH FREQUENCY ANALOG INPUTS

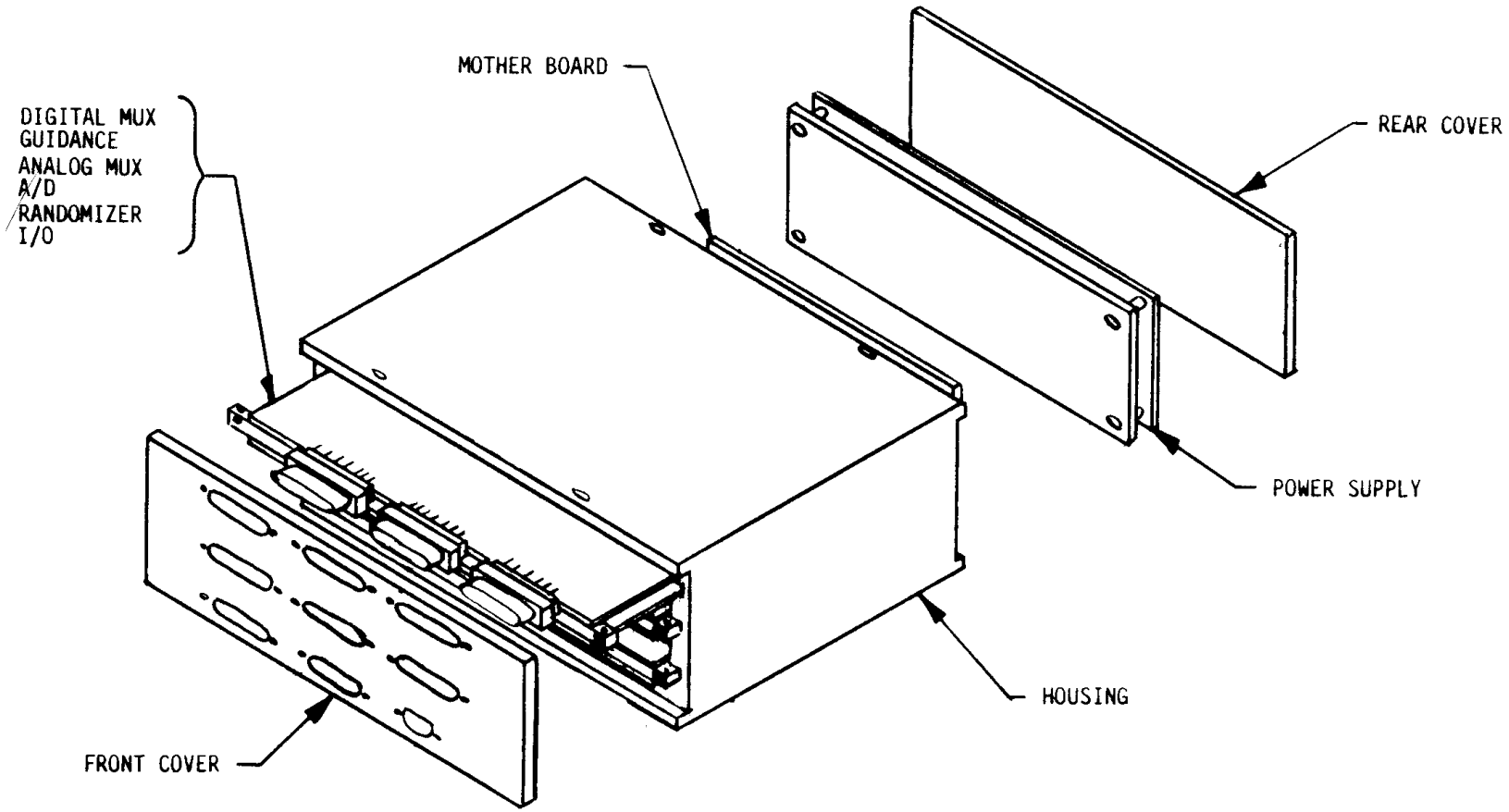

FIGURE 8
PCM ENCODER