DESIGN AND DEVELOPMENT OF AN ADVANCED MICROWAVE POWER LEVELING LOOP*

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ABSTRACT

An advanced microwave power leveling loop (MPLL) was conceived, designed, fabricated, tested, and used during spacecraft in-orbit testing. The primary function of the MPLL is to maintain constant RF power transmitted from an earth station antenna during spacecraft in-orbit transponder testing.

The MPLL utilizes nonlinear analog electronics with flexible signal path routing under microprocessor control. It achieves a power control dynamic range of greater than 50 dB with better than 0.1 dB of control resolution. Power level step changes of 20 dB can be accomplished in under 10 ms. The MPLL is IEEE-488 bus controllable and is designed for use in automated in-orbit test systems to facilitate the measurement process and produce more repeatable results than have previously been possible. Measurements performed with the aid of the MPLL include transponder frequency response, group delay, gain, and saturation level. The system can also be operated in a manual mode, and utilizes state-of-the-art human interfacing techniques such as a display/entry panel and a rotary encoder control knob.

This paper describes the MPLL design process, including computer simulation work and breadboard testing. Performance and temperature chamber test results are presented for breadboard and manufactured units.

1. INTRODUCTION

This paper discusses the design and development of an advanced microwave power leveling loop (MPLL) system from functional requirements definition to breadboard hardware test results. The hardware described is intended for use in communications

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satellite automated in-orbit test systems, but could be employed in many systems that require a precisely leveled microwave power output.

During in-orbit testing (IOT) of communications satellites, a test signal is transmitted from an earth station to the satellite. This signal must be of known frequency and power. Typically, the up-link signal of the IOT equipment is generated by a microwave frequency synthesizer. Between this frequency source and the earth station antenna, amplitude variations are introduced by many elements, including filters, attenuators, switches, power amplifiers, couplers, cables, waveguides, and rotary joints. These elements can produce variations of 4-5 dB over a nominal 500-mHz communications band.

The MPLL is an electronic subsystem that removes these variations in amplitude with time and frequency by continuously monitoring the RF power at the earth station antenna feed and adjusting the microwave source power via feedback control. The MPLL described here is a third-generation design incorporating refinements that were developed over the last 10 years of testing satellites in orbit.

2. FUNCTIONAL REQUIREMENTS AND SPECIFICATIONS

The MPLL should provide microwave power control in either a closed- or open-loop control mode. The closed-loop (or “leveled”) mode is a feedback control mode that automatically maintains microwave power at a constant, user-selectable level. The open-loop mode of operation allows the user to set a desired microwave power level, but does not automatically adjust or compensate for power level changes caused by system equipment fluctuations.

The functional and performance specifications for the MPLL are derived from two types of requirements. The first is based on an IOT hardware constraint, i.e., a measurement accuracy specification. The second is based on IOT experience and the need a for rapid IOT capability.

In response to the need for measurement accuracy, the MPLL must:

a. Sense microwave power with an RF detector diode located in the antenna feed area.
b. Control microwave power with a PIN diode modulator.
c. Level power to a 0.2-dB accuracy over a 500-MHz communications band.
d. Have a greater than 35-dB dynamic range of operation.
e. Supply a 1-kHz sinusoidal amplitude modulation of the microwave signal.
f. Provide an input for a 1-mHz amplitude modulation source.
g. Provide an output for 1-mHz amplitude modulation detected by the RF detector diode.

Based on IOT experience and the need to facilitate testing, the MPLL:

h. Allows for computer control via an IEEE-488 bus interface.
i. Requires a minimum of adjustments over its lifetime.
j. Functions to specifications in the noisy RF earth station environment.
k. Provides better than 0.1-dB power adjustment resolution over the entire operating range.
l. Allows fast (<10 ms) power step response.
m. Uses a rotary control for power level adjustment.
n. Transitions from closed to open (and open to closed) loop control without introducing a step change in power level.
o. Provides a set of storage registers for quick storage/recall of power levels.

Specification (h) responds to the need for automated measurement capability, and requires that all MPLL functions be commendable from the IEEE-488 interface. These functions include power level control, open/closed loop mode selection, modulation on/off control. and storage register control. Also, local (or manual) control should be locked out during IEEE-488 commanding. Specification (j) is based on the knowledge that earth stations experience high levels of RF interference (from microwave frequencies down to power line frequencies) which has caused difficulties in previous MPLL designs.

Overall, this generation of MPLL is designed as an integral part of an automated IOT system. A new and important use of the MPLL is in performing automatic spacecraft transponder saturation level measurements. Such automated measurements can significantly reduce the time required for IOT, and can provide improved measurement repeatability with fewer errors.

3. DESIGN APPROACH AND DESCRIPTION

As shown in Figure 1, the MPLL elements (shaded blocks) were added to an unleveled system to produce a leveled system. The MPLL consists of the following five major elements:

- RF Detector Diode
- Preamp Unit
- MPLL Main Unit
- Manual Display/Entry Unit
- PIN Diode Modulator

The preamp unit is mounted near the RF detector diode in the antenna feed area. The MPLL main unit is a rack-mount unit that is located in an IOT equipment rack. The

display/entry unit is located near the IOT equipment racks in an area convenient to the operator. In operation, the IOT operator either controls the MPLL manually using the display/entry unit, or allows the control computer to send commands to the MPLL via the IEEE-488 bus.

The subsections that follow describe the basis for selection and the functional characteristics of the MPLL elements. Each subsection highlights design problems or critical areas as they relate to the MPLL system. Subsection 3.4 summarizes the design solutions for these problems.

3.1 Sensing and Control Elements

The selection of an RF crystal detector diode sensor and a PIN diode modulator control element was based on the need for continuous domain control. These elements provide fast (high-bandwidth) response and were used in previous designs. This allows the new generation of leveling loop to provide a plug-in-compatible upgrade for existing systems.

These elements also have drawbacks. As shown by the transfer characteristics of Figure 2, the devices are highly nonlinear (that is, an N times change in input does not produce an N times change in output). There is a definite exponential type of response, but even this is not entirely correct. While the curves of Figure 2 are typical, significant variation exists on a unit-to-unit and over temperature basis. This may explain why it is difficult to obtain accurate data for a particular device.

The device characteristics reveal that power level cannot be directly and accurately measured or controlled by these elements. Also, in terms of control theory, loop gain (and therefore time response) cannot be held constant over the operating range of the closed-loop system without using nonlinear compensation.

3.2 Preamp Unit

A remotely located preamp design was chosen based on the low signal output level of the RF detector diode. Because the diode used provides outputs in the millivolt range, earth station noise is easily disruptive even if a short length of cable is used to connect the diode to the MPLL. The preamp will amplify detector local output to increase the signal-to-noise ratio so that noise in the long detector-to-MPLL main unit connecting link will not corrupt the signal. Refer to the block diagram of the preamp unit shown in Figure 3.

Since the signal produced by the detector will span a 50-dB dynamic range in actual operation, linear amplification alone is not sufficient. Even with amplification, signals from the detector may get lost in noise during transmission to the main unit. Because of this,

signal compression was added in the form of a logarithmic amplifier. The logarithmic amplifier essentially compresses a 50-dB dynamic range input signal into an output signal with a 20-dB dynamic range, thereby adding up to 30 dB to the preamp-to-main unit link signal-to-noise ratio.

As further insurance against noise corruption, a continuous digital transmission mode was selected. This approach was implemented with a linear voltage-to-frequency (V/F) converter, which converts continuous-domain amplitude information into continuous-domain frequency information that can be transmitted with digital (two amplitude state) pulses. Continuous digital transmission prevents the loss of detector output amplitude information due to quantization error, and provides immunity to amplitude modulation noise.

The design difficulties associated with a preamp, as described above, arise from the fact that it must function over a large temperature range typical of the earth station antenna feed area. Unfortunately, the electronics required to implement the logarithmic amplifier and linear V/F converter can be very temperature sensitive.

3.3 Main Unit and Display/Entry Unit

The MPLL main unit utilizes a microprocessor to control all functions for the MPLL system, and provides an interface to the two types of user controls. It connects to the display/entry unit for manual control, and to an IEEE-488 instrument control bus for computer automated control. The MPLL main unit also houses the analog control electronics that receive the power level sensor information generated by the preamp and provide drive signals to the PIN modulator. The MPLL main unit has a rotary control mounted on its front panel that can be used by the operator to adjust power level in the manual mode. Figure 4 is a block diagram of the overall system, and Figure 5 shows details of the analog control electronics and the microprocessor-controlled switching functions.

A microprocessor-based design was selected so that a minimum amount of hardware could provide maximum functional flexibility. The microprocessor is almost a necessity given that IEEE-488 bus control is required of the MPLL. Beyond this, the microprocessor provides for the use of a combined-function touch panel display/entry unit, which makes the MPLL more user friendly by providing descriptive interactive displays to the operator.

An MPLL calibration process is also performed under microprocessor control, using the control computer and power meter shown in Figure 1. Calibration provides the MPLL with RF crystal detector diode power-to-voltage transfer characteristic data. With this

information, the MPLL can rapidly measure and set system RF power with ±0.1 dB accuracy.

Closed-loop control could have been implemented through the microprocessor using digital filter techniques; however, the processor algorithms needed to control such a system would require a large amount of processing time, resulting in a low sample rate and correspondingly low control bandwidth. Therefore, an analog approach was selected. The analog electronics used contain a nonlinear loop compensation network (Figure 5) based on the nonlinear nature of the sense and control elements described in Subsection 3.1. A block diagram of the analog electronics is shown in Figure 5, which also shows the various microprocessor-controlled switches and analog interfaces used for system control.

3.4 Summary of Solutions to MPLL Design Problems

Based on the design requirements listed in section 2 and the design approach presented in this section, several areas of design criticality or difficulties arose. Most of these problems were overcome by using the microprocessor and flexible microprocessor-controlled nonlinear analog electronics. Through careful computer-aided design of the nonlinear loop compensation network, the loop was linearized to a degree (as will be shown by the system transfer characteristic curves and time response plots in Section 5). The use of a liberal number of microprocessor-controlled analog switches and analog monitoring points in the electronics paths allowed the processor to configure the system as required to transition from open to closed and closed to open loops without inducing a power level change. This flexibility also enables the processor to perform a calibration process and display accurate power levels derived from a nonlinear sensor (RF detector diode). Finally, this approach allows a large degree of IEEE-488 bus command capability and provides for informative user displays and convenient user control interfaces.

Two problem areas were not resolved by the above-mentioned hardware/software flexibility. One area involved the implementation of a temperature-stable preamp unit containing the complex analog processing electronics described in Subsection 3.2. This critical design factor was overcome through an iterative test and circuit analysis process which identified the circuits of highest temperature sensitivity and designed circuits of low temperature dependence in these areas. A discrete V/F converter design was ultimately used to achieve minimum temperature dependence.

The second problem area was concerned with achieving an open-loop control voltage vs output characteristic that was nearly linear, like that of the closed-loop system. This dilemma was resolved by placing a voltage squaring circuit in the control voltage path after the digital-to-analog (D/A) converter during open-loop operation. This, along with some

software routines, produced a “dB-linear feel” in the open-loop mode similar to that achieved in the closed-loop mode by the feedback path logarithmic amplifier.

4. DESIGN DETAILS

This section presents a detailed description of the constituent parts of the MPLL design: the microcomputer architecture and functions, the nonlinear analog electronics, and the temperature-stable preamp circuit.

4.1 Microcomputer/User Interface Design

A standard bus (STD BUS) microcomputer architecture was chosen for use in the MPLL for several reasons. First, STD BUS computer systems can be packaged in a reasonably compact fashion. This was important in order to meet a 3-1/2-in.-high rack-mounted package design goal. Second, a large selection of STD BUS components was available with off-the-shelf delivery, which allowed the CPU, memory, digital/analog I/O, mathematical processor, and IEEE-488 bus interface cards for the MPLL design to be plug-in compatible and low cost. Overall, the use of a STD BUS component microprocessor system eliminated the need to design costly custom processor cards and provided all the functionality of a custom design.

The MPLL uses seven STD BUS cards, as shown in Figure 4. The CPU is a 4-MHz Z80A microcomputer supported by a 9511-based mathematical processor board. Use of the mathematical processor board reduced the amount of MPLL software required and provided fast mathematical calculation capability, all with plug-in ease. Three cards provided multichannel 12-bit analog and 64-bit TTL I/O capability.

Interrupt sources were connected to the Z80A interrupt line through a custom TTL digital board. This interface allowed for the stacking of interrupts to avoid missing any. The interface circuit for the optical rotary encoder is also contained on this board, as is the interface for the display/entry unit touch switches. The IEEE-488 bus interface card used is based on an Intel 8291A chip. The board performs many functions, including hardware-488 bus handshaking, serial poll response, and status buffering. Because of this high level of on-card functionality, the MPLL CPU need only perform in software applications routines; therefore, MPLL response to IEEE-488 bus commands is very fast. The memory board for the Z80A contains 8K bytes of PROM and 2K bytes of RAM.

Operationally, the microcomputer continuously monitors the MPLL input devices for a user command. Rotary encoder, local reset, and IEEE-488 bus (GPIB) inputs are handled on an interrupt basis, while touch panel inputs are managed on a polled basis. Figure 6 shows the overall MPLL software flow. Most of the MPLL software routines are

interruptable and re-entrant. However some routines are noninterruptable in order to prevent undesirable operational conditions from occurring due to the asynchronous nature of interrupts. When an interrupt occurs, it is processed as is shown in Figure 7. Interrupt priority is assigned through software, as shown.

Every function of the MPLL has an associated microcomputer software routine. While the description of each of these routines is beyond the scope of this paper, Table I summarizes the MPLL functions. The table is actually a list of MPLL IEEE-488 commands which encompass the full set of MPLL functions performed by the microcomputer as a result of any user input except rotary encoder inputs.

Table II summarizes the IEEE-488 bus commands supported by the MPLL. User inputs, processed by table-driven software, produce outputs in the form of hardware signals to the switches and D/A converters shown in Figure 5. The rotary encoder produces one interrupt to the CPU for approximately every 1/3 of a degree of rotation. Each encoder interrupt is counted by the interrupt service routine. When the count reaches N, the input value to the D/A converter that Controls system microwave power level is incremented or decremented, depending on encoder rotational direction.

The MPLL functions under either a local or a remote mode. In the local mode, operator inputs are accepted from the touch/display unit and from the rotary encoder. However, when an IEEE-488 command is received, the display/entry unit and rotary encoder are locked out. The remote mode of operation is then entered, and only IEEE-488 commands are accepted until the MPLL is commanded to the local mode again.

Under both modes of operation, the display/entry unit continuously displays current MPLL status. Figure 8 shows the display format used. The asterisks indicate the location of operational touch switches. When a touch switch is acted upon or an IEEE-488 command is processed, the displayed text is updated to reflect any new MPLL conditions. The display/entry unit consists of a plasma panel display with an infrared beam optical switch grid placed just in front of it. The plasma panel accepts parallel ASCII data at rates of greater than 1 million characters per second, and easily accepts characters as fast as the Z80A CPU can produce them. The optical switch grid provides an output that corresponds to the location of the particular switch that is active, and can be used to vector to processing routines.

Table I. Leveling Loop IBEE-488 Command Summary

Command	Function Description
MD1	Modulation on.
MDO	Modulation off.
LAC	Selects coarse resolution for rotary level adjust control.
LAF	Selects fine resolution for rotary level adjust control.
CAL	Invokes calibration process.
CST	Terminates calibration process.
SPW	Selects power output mode.
SDA	Selects D/A converter output mode.
CLO	Selects closed-loop operation.
OPN	Selects open-loop operation.
PUP	Increments power control D/A converter with the value selected by the STP command.
PDN	Decrements power control D/A converter with the value set by the STP command.
STOXXE	Stores current system power level in register XX, where XX equals 1 to 10.
RCLXXE	Recalls power stored in register XX and sets system to this level. XX equals 1 to 10.
STPXXXE	Loads power control D/A converter step size register with value XXX, where $0 \leq XXX \leq 255$.
SCRXXXE	Loads relative resolution for coarse level adjustment. $0 \leq XXX \leq 255$, where 0 is coarse and 255 is fine.
SFRXXXE	Same as SCRXXXE except loads fine level adjustment resolution.
PWR+-XX.XE	Sets system power to ±XX.X dBm. Value field may or may not be signed and may contain a leading zero or space, but most use one decimal place only.
CLP+-XX.XXE	Controller reads power value and sends to leveling loop on an SRQ generated during calibration. Value field is in dBm and may or may not be signed. It may contain a leading space or zero, but most use two decimal places.

Table II. Leveling Loop IEEE-488 Bus Commands

Command	Function Description
REMOTE	MPLL enters the REMOTE mode when selectively addressed to listen.
LOCAL (GTL)	MPLL enters the LOCAL mode when requested to by a GOTO LOCAL message.
LOCAL (REN FALSE)	MPLL enters the LOCAL state when the HPIB hardware REMOTE enable line goes false.
ABORT (IFC)	MPLL stops all talk and listen functions and continues normal operation.
DEVICE CLEAR (SDC)	MPLL assumes a state defined by CLOSED LOOP, MODULATION OFF, COARSE LEVEL ADJUST,and minimum power output. MPLL does not lose calibration information or storage contents, and stays in the LOCAL/REMOTE mode it was in at the time of SDC request.
SERIAL POLL	MPLL returns the status byte to the controller defined in Table III.

Table III. Leveling Loop Status Byte Summary

Serial Poll Status Byte Bit Number	Description
0	0 = D/A Output mode selected 1 = Power output mode selected
1	0 = Fine resolution level adjust selected 1 = Coarse resolution level adjust selected
2	0 = 1-kHz modulation on 1 = 1-kHz modulation off
3	0 = Closed-loop (leveled) mode 1 = Open-loop (unleveled) mode
4	0 = LOCAL control mode 1 = REMOTE (HPIB) control mode
5	0 = Calibration not in process 1 = Calibration in process
6	RSV (1 = SRQ)
7	0 = Complete calibration not performed 1 = Complete calibration performed

All MPLL software was written in assembly language. The assembled code occupies nearly 8K bytes of PROM and includes system diagnostic software that can be run at any time during MPLL local mode operation. This software performs a PROM checksum test, a bit-by-bit RAM write/read test, a mathematical processor test, and digital/analog I/O internal hardware loopback tests. During a diagnostic run, MPLL operation is suspended so that no user input is acted upon.

4.2 Analog Electronics Design

Since the MPLL was designed for 50 dB of dynamic range, and the sensing and control elements are highly nonlinear, considerable attention was given to designing the analog electronics that perform the power leveling function. Other MPLL requirements that governed the analog electronics design included the need for fast power step response (less than 100 ms over the entire 50-dB operating range) and the desire that the manual power control knob have a dB-linear feel.

A computer simulation program was created to identify suitable transfer functions for use in the analog electronics design. Figure 9 is a block diagram of this program. Models were created for the RF crystal detector diode, the PIN diode attenuator, and the TWT amplifier (see Figure 10 transfer curve) based on data collected and experience with the components. Polynomial curve fitting was performed on the data to form the final models. The simulation program allowed various functions to be tested in the forward and feedback control paths. By varying the input control voltage, both power output vs control input and power step response could be investigated. A TEK PLOT 10 graphics software package was used to generate time and transfer response plots.

Many transfer functions could have been used in the simulation program, but only those functions that could be synthesized with analog electronics of a reasonable complexity were seriously considered. The transfer functions shown in Figure 5 fell in place almost naturally. The best location for a nonlinear log function was found to be the feedback path. Since the preamp unit was located in the feedback path and a compression circuit was needed in the preamp, the logarithmic amplifier was ideally suited for the task. Placement of the logarithmic amplifier in the feedback path caused the power out vs control voltage input function to be nearly dB-linear, as desired. The forward transfer function was then developed around an integrator such that control “position error” would be zero. Double integration schemes were tested, but did not provide as fast a transient response as the single integrator design. Eventually, with the correct gain selections and limiter placement, a 20-dB step power change could be accomplished in under 5 ms.

The logarithmic amplifier in the feedback path allows the 12-bit D/A converter used as the MPLL control voltage source to provide a nearly constant control resolution of better than

0.05 dB over the entire operating range. This makes the control feel smooth to the operator. However, the dB-linearizing effect of the logarithmic amplifier was lost when the open-loop control mode was used. To maintain good control resolution in the open-loop mode, a squaring function was placed in series with the D/A output. This had the effect of expanding the D/A output range and somewhat substituted for the feedback loop compression provided by the logarithmic amplifier in the closed-loop mode.

4.3 Temperature-Stable Analog Circuit Design

In order for the conceptual analog electronics to be implemented in circuit form, the critical circuitry of the preamp unit had to be temperature-stable because the preamp would be located in an uncontrolled environment. Both the logarithmic amplifier and the V/F converter circuits were potentially very temperature sensitive. The sensitive areas of the logarithmic amplifier were more easily identified than were those of the V/F converter, but both circuits provided a challenge in design.

The logarithmic amplifier was designed around the exponential collector current vs base-emitter voltage characteristic of a bipolar transistor. Equations reveal that if two transistors are used (one with a reference collector current and the other with an input current), the differential base-emitter voltage is a logarithmic function of the input current. The differential voltage is also directly proportional to temperature, and is affected by the relative matching of the two transistors used. The temperature effect was compensated for with a thermistor-controlled gain amplifier. A monolithic supermatched pair of transistors was used to avoid matching problems.

With these obvious problem areas corrected, one area of concern remained. Since the logarithmic amplifier was required to perform over a wide dynamic range, a reference current on the order of 100 nA was used. Because of this, bi-FET op amps were used where temperature-dependent amplifier input bias currents would be a problem. Also, precision, ultra-low-noise, low-drift bipolar op amps were used in gain stages.

The final preamp V/F converter circuit design was the result of an iterative design and thermal chamber test process. A monolithic IC-based circuit initially tested proved to be too temperature-sensitive. Based on this experience, a more discrete V/F converter circuit was built to allow the various blocks of the circuit to be examined and tested. Ultimately, it was found that monolithic analog switch ICs were highly temperature sensitive with respect to turn-on and turn-off vs command signals. This caused imprecise on/off time switching of a current source in the circuit. Since the V/F transfer function was directly proportional to the length of the current pulse, this switching function had to be stabilized with respect to temperature. The solution was found in the use of a discrete dual-gate MOSFET switch with a high-speed driver. Along with a precision monolithic voltage

reference, the discrete V/F converter provided an order of magnitude improvement in temperature sensitivity over the commercial monolithic IC-based circuit.

5. HARDWARE TEST RESULTS

A breadboard MPLL was fabricated and tested using a setup similar to that shown in Figure 1. The high-power amplifier (HPA) shown was simulated in the laboratory by using a 2-W traveling wave tube amplifier. The IEEE-488 bus control design of the MPLL allowed repetitive and incremental step tests to be performed with ease.

Figures 11 through 14 present simulated vs measured MPLL closed-loop characteristics. Figure 11 shows the computer-simulated MPLL response to a 20-dB power level step change. The step occurs at the 50 ms mark. Actual measured RF crystal detector diode output voltage response due to a 20-dB step power change is displayed in Figure 12. The top oscilloscope trace of Figure 12 ,shows the MPLL control voltage step, while the bottom trace shows the crystal detector voltage. The horizontal axis is set at 2 ms per division. A fast (under 10 ms) response time has been attained. Additionally, the response is smooth and free from overshoot that could cause momentary undesired bursts of RF power.

Figure 13 displays the computer-simulated MPLL control voltage vs output RF power transfer characteristic. The measured function is shown in Figure 14. Note that a dB-linear characteristic has been achieved over a range of approximately 35 dB.

Other tests performed included -20 to +50°C temperature testing of the preamp unit. These tests showed that from -20 to +40°C, the system RF output level drifted at a rate less than 0.05 dB/°C. At temperatures below 25°C, drift was less than 0.02 dB/°C.

6. SUMMARY AND CONCLUSIONS

An advanced microwave power leveling loop system was designed, fabricated, and tested. Because this new-generation MPLL was designed for use in automated test systems, control time response and transfer characteristics were substantially improved over earlier designs to meet rapid measurement needs. A computer dynamics simulation was used to linearize and optimize the control characteristics of an otherwise nonlinear system.

Breadboard test results show that the MPLL design goals were achieved and that the microprocessor/nonlinear analog control electronics design approach was effective. Additionally, the operational characteristics of the MPLL were improved so as to be consistent with state-of-the-art instrument design. Finally, the microprocessor-based design

allows the MPLL to be customized, through software revision, to meet the needs of individual system applications.

7. ACKNOWLEDGMENTS

The original idea for the advanced MPLL was conceived by A. Lopatin, who also provided technical guidance relative to microcomputer design from the outset of the project. Thanks are also given to E. Hare for his technical support in the hardware and software areas. V. Riginos was instrumental in securing project support and, along with K. Fullett, furnished expertise in the microwave and processor interfacing areas. Finally, special appreciation goes out to H.-D. Zago of INTELSAT for providing financial authorization for the project.

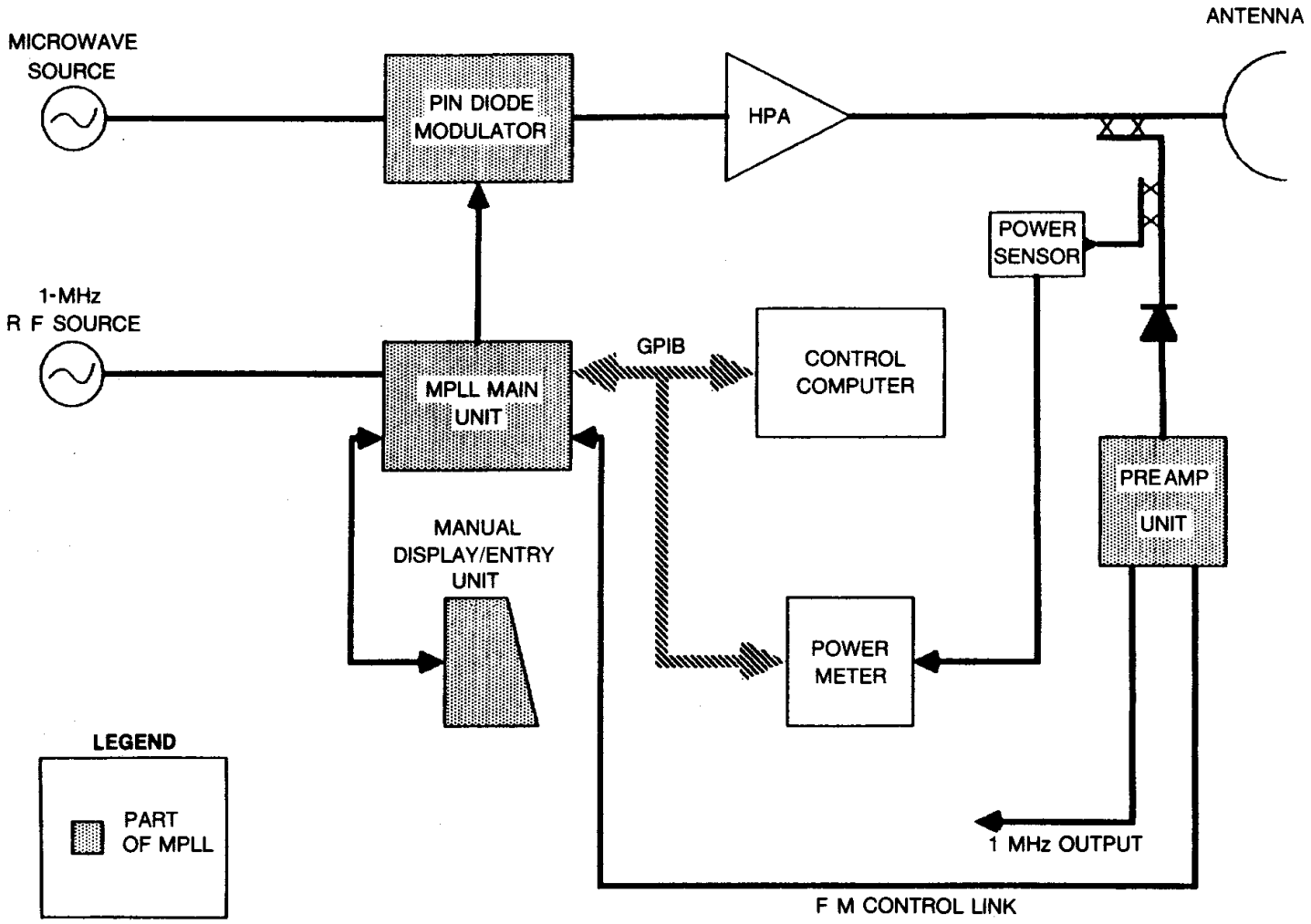

Figure 1. MPLL System Block Diagram

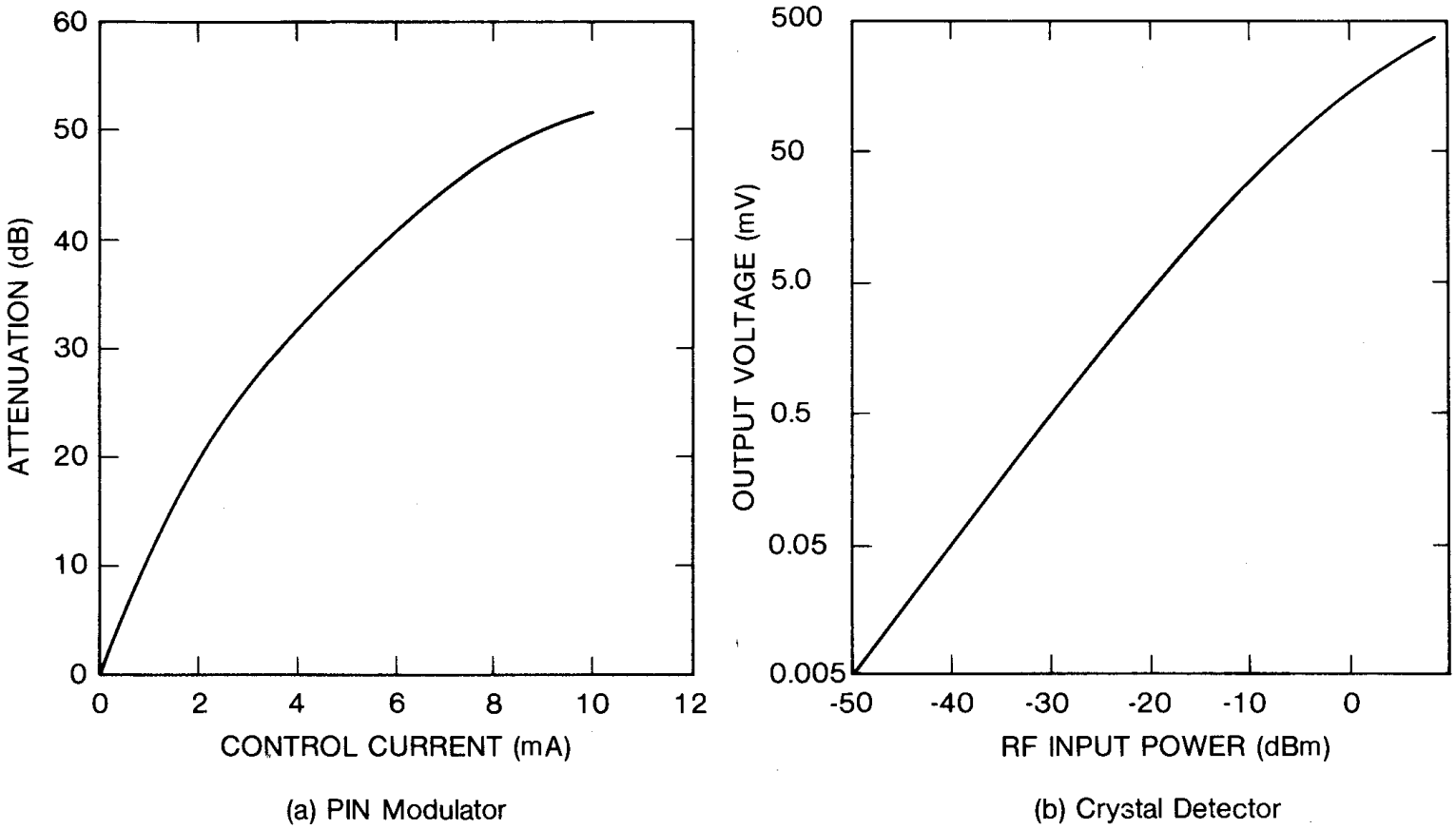

Figure 2. Typical PIN Modulator and Crystal Detector Transfer Characteristics

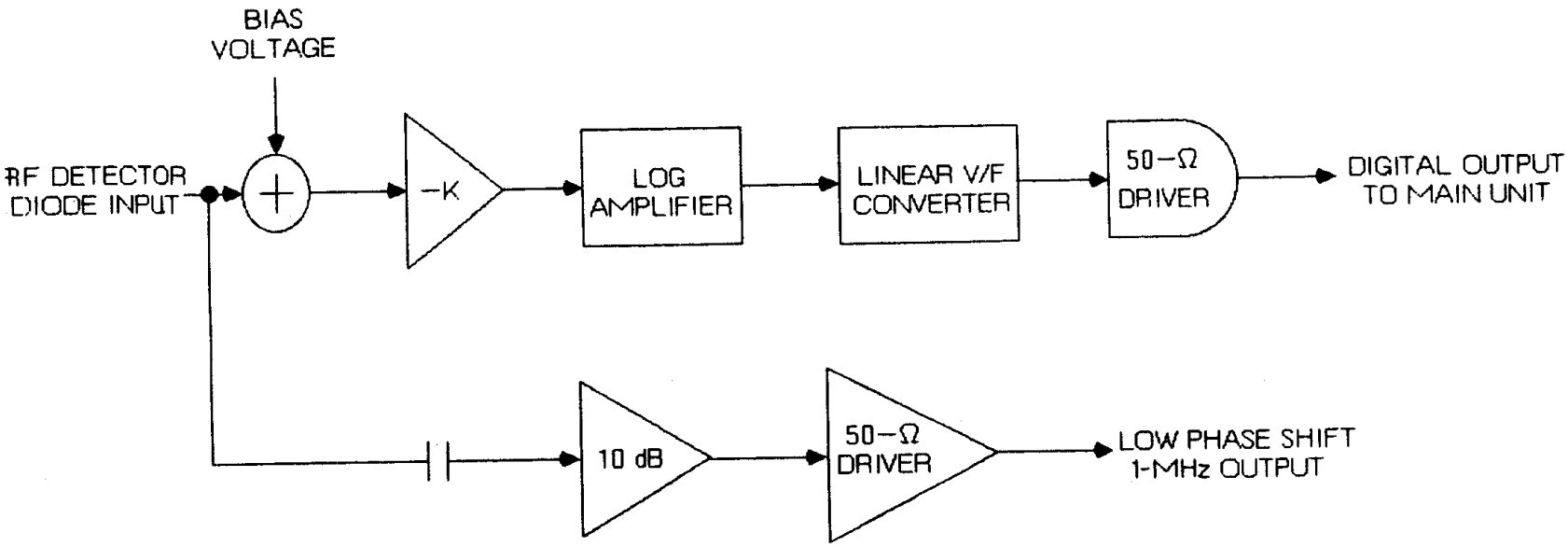

Figure 3. Preamp Block Diagram

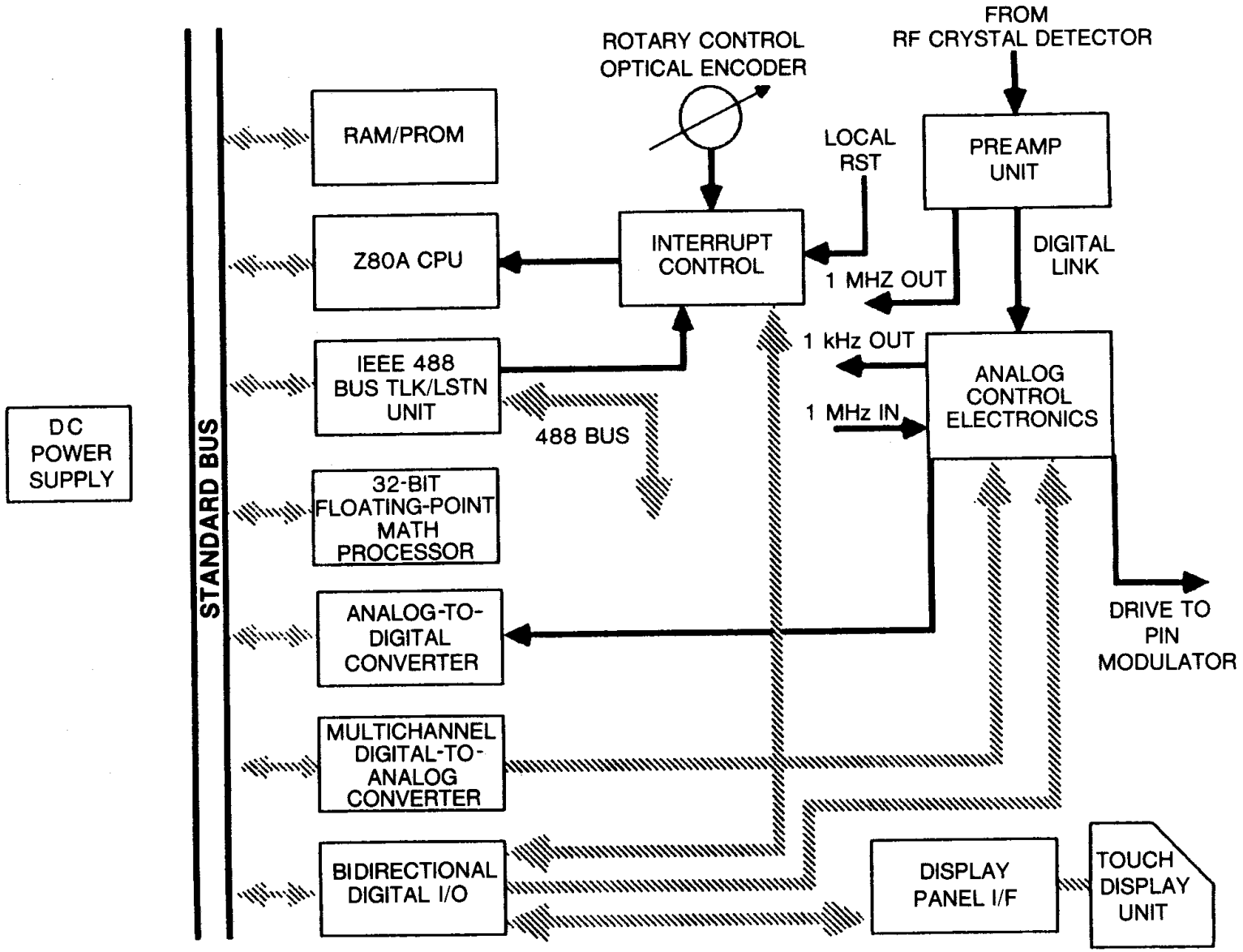

Figure 4. MPLL Block Diagram

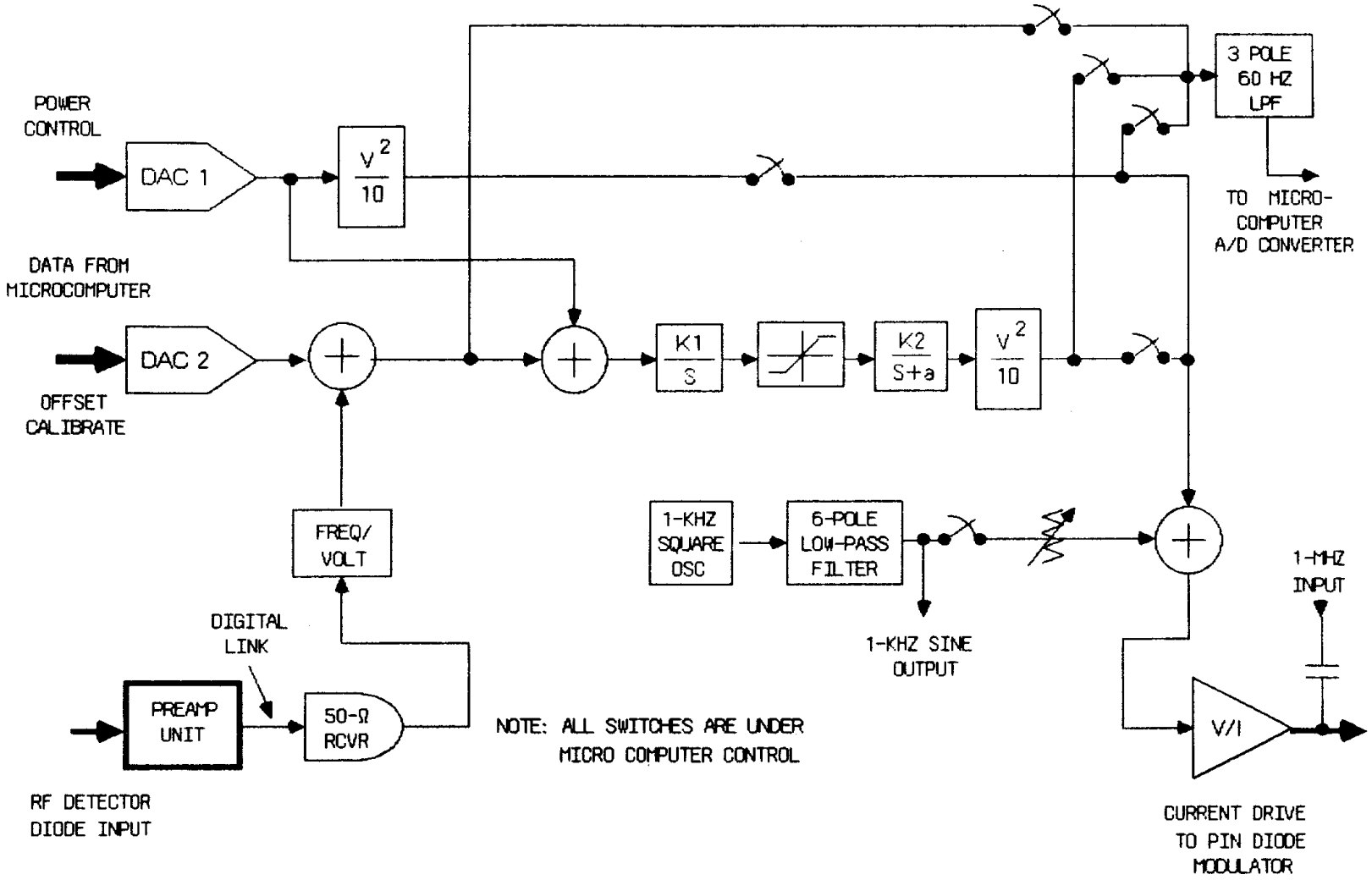

Figure 5. Analog Electronics Block Diagram

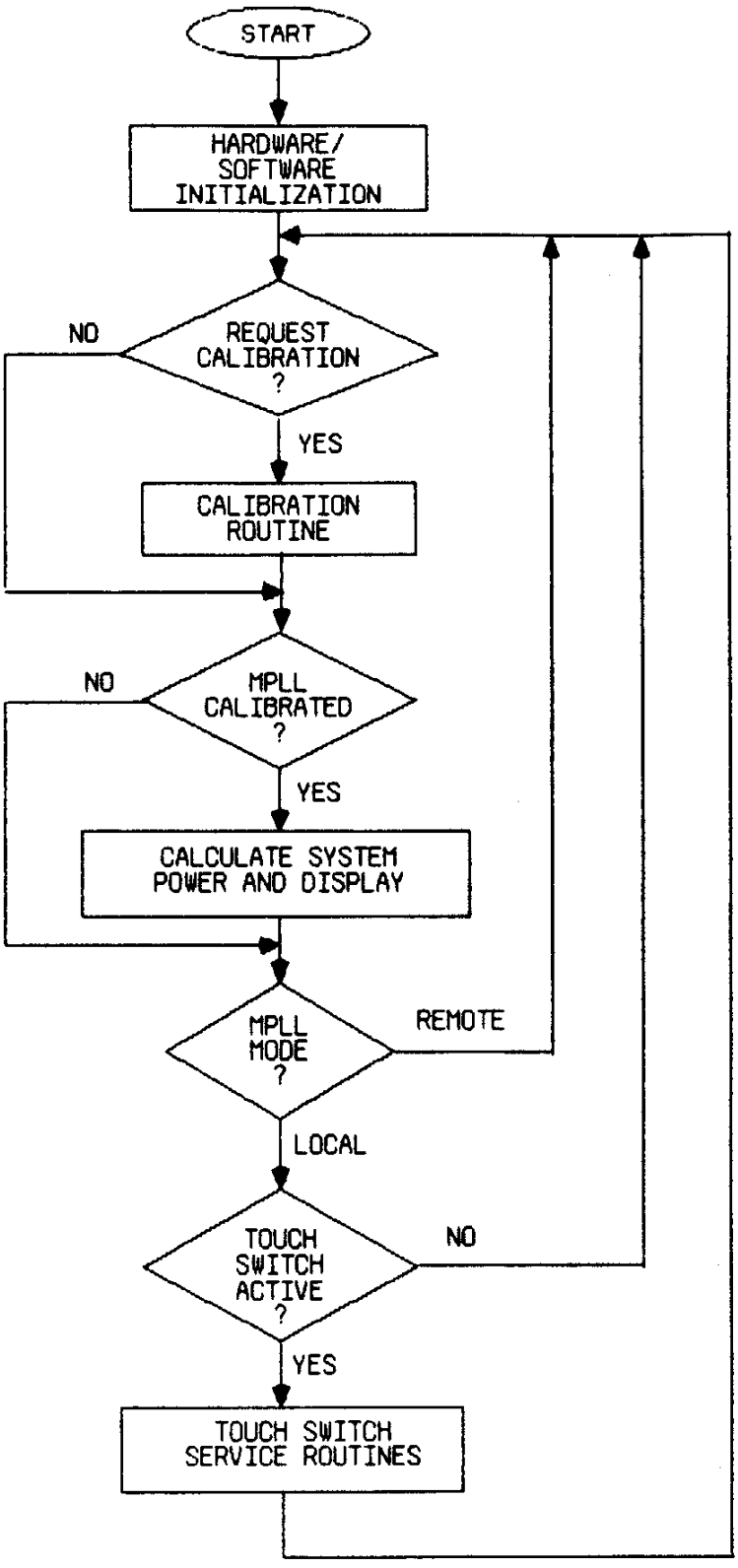

Figure 6. MPLL Software Flow

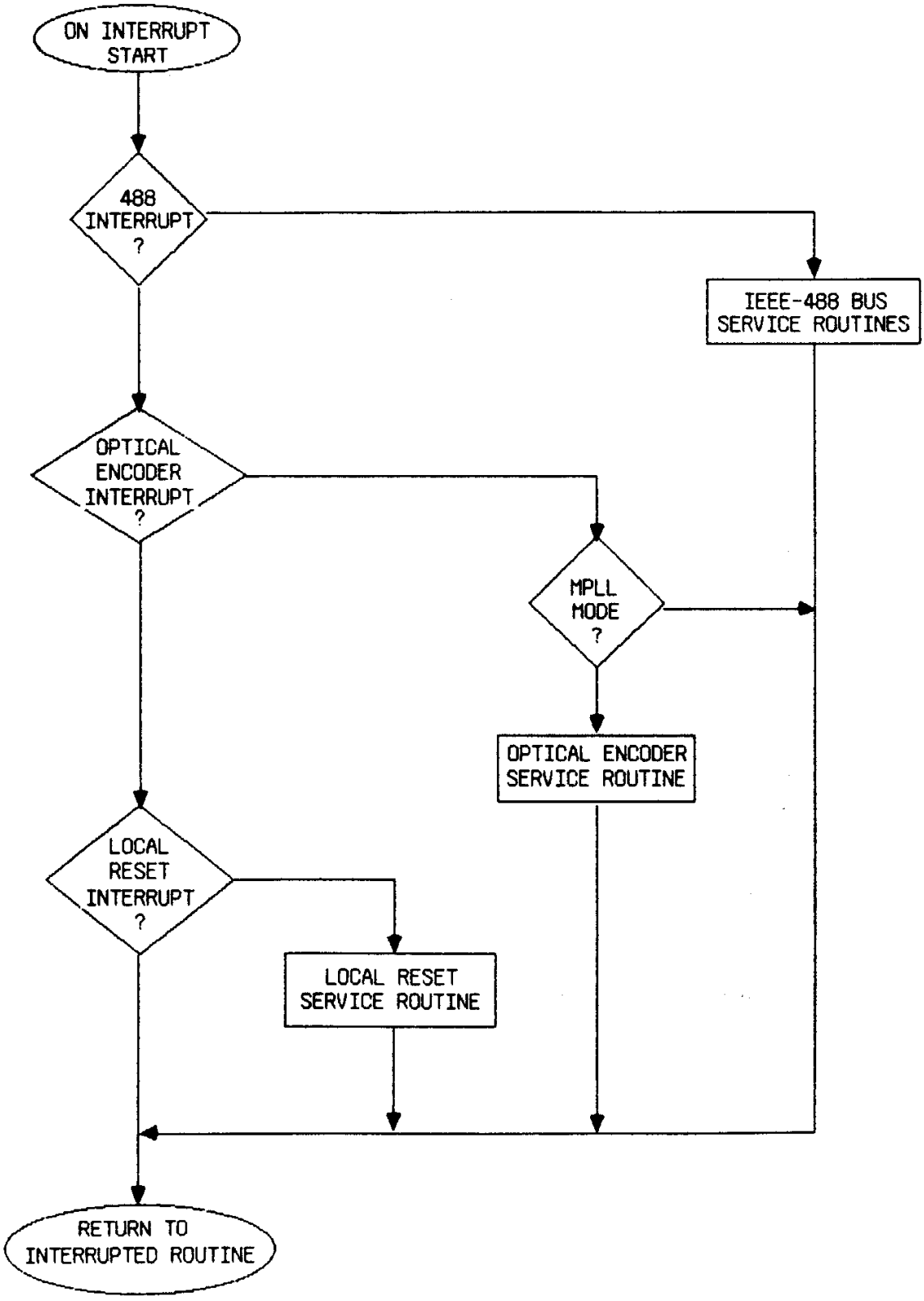

Figure 7. MPLL Interrupt Processing Flow

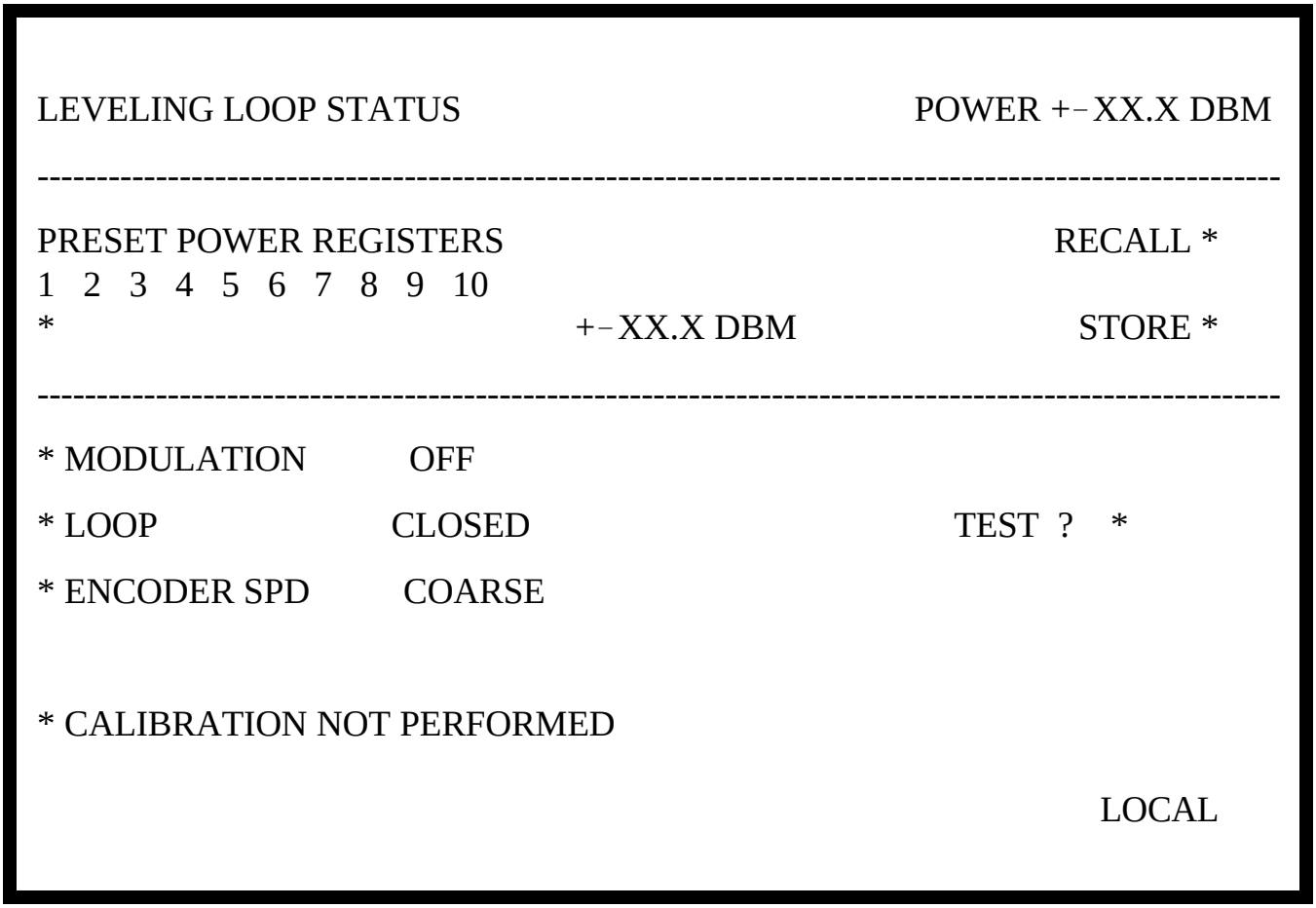

Figure 8. MPLL Touch/Display Unit
Operational Display Format

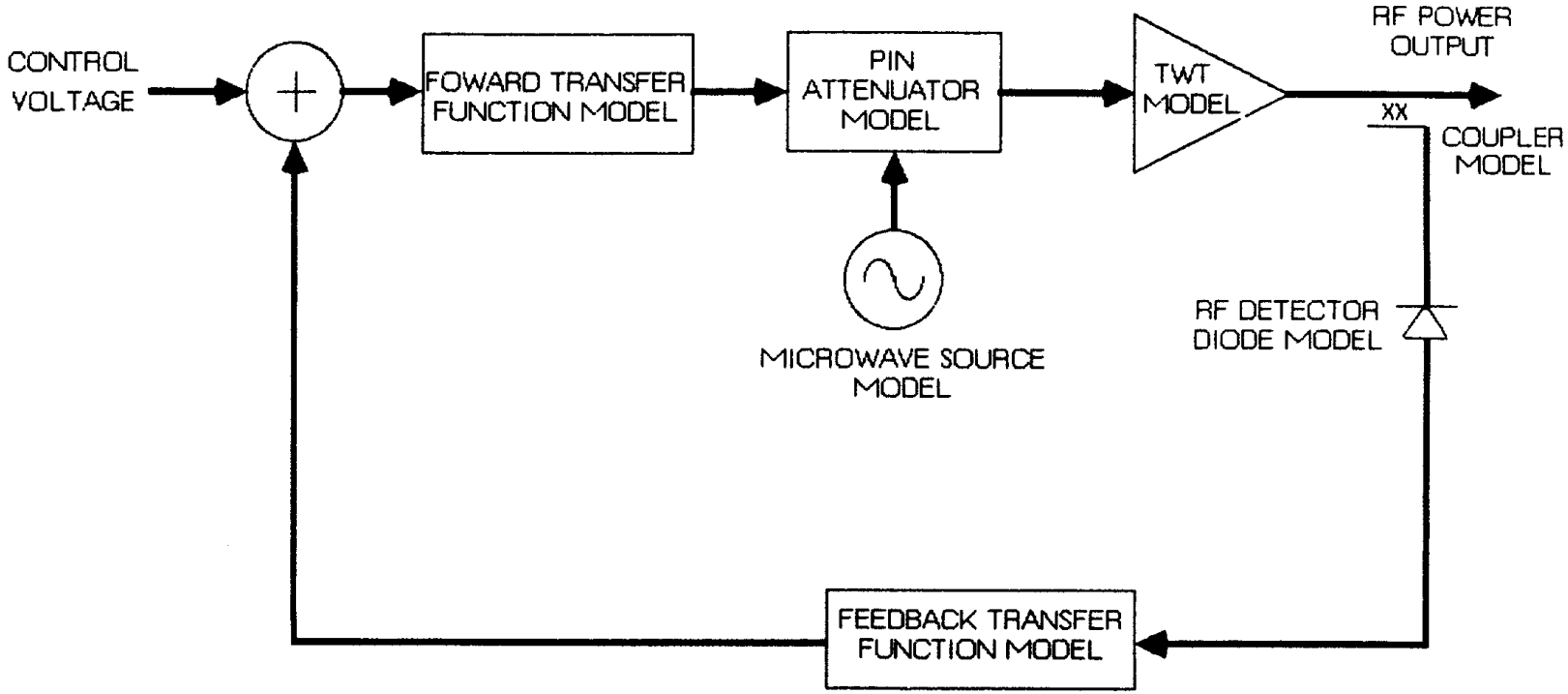

Figure 9. MPLL Closed-Loop Dynamics Simulation Block Diagram

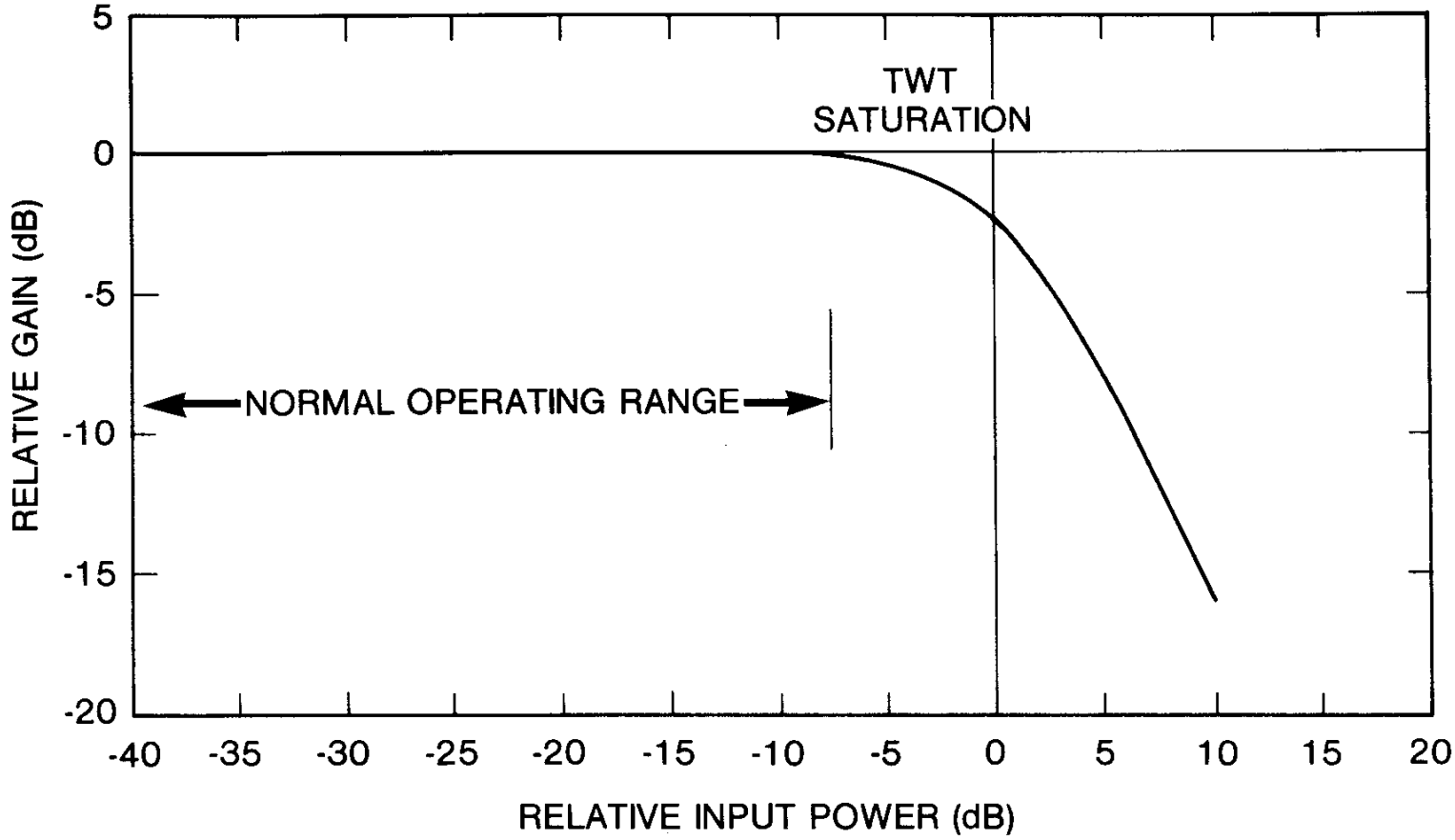

Figure 10. Relative TWT Power Gain vs Input Level

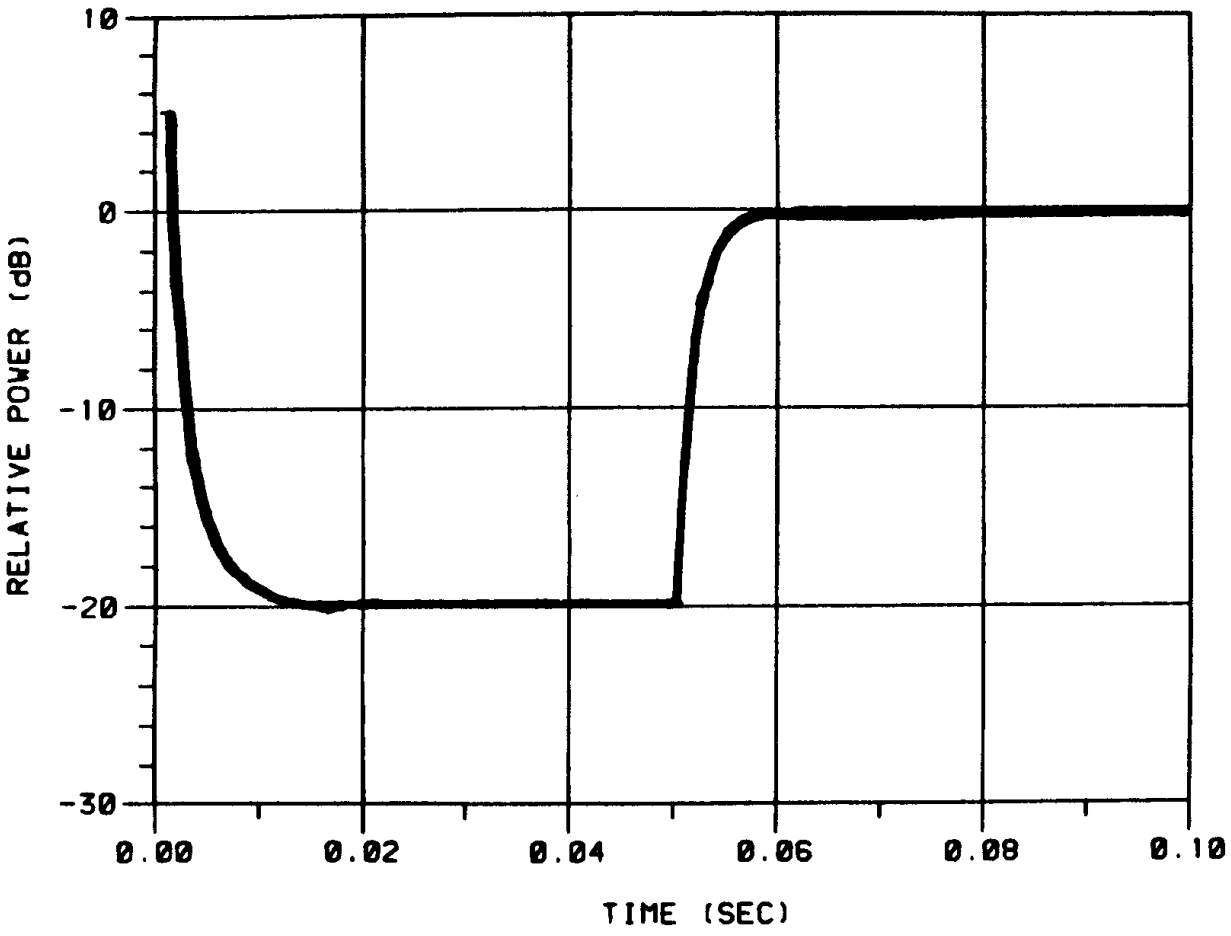

Figure 11. MPLL Step Response Simulation

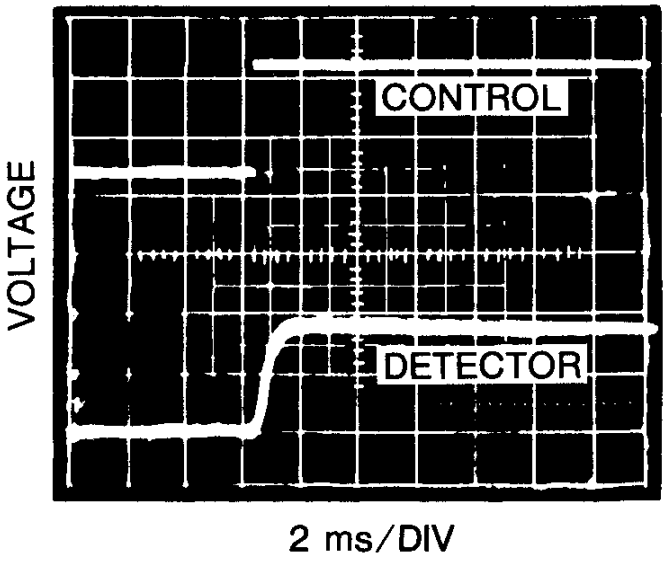

Figure 12. Measured MPLL

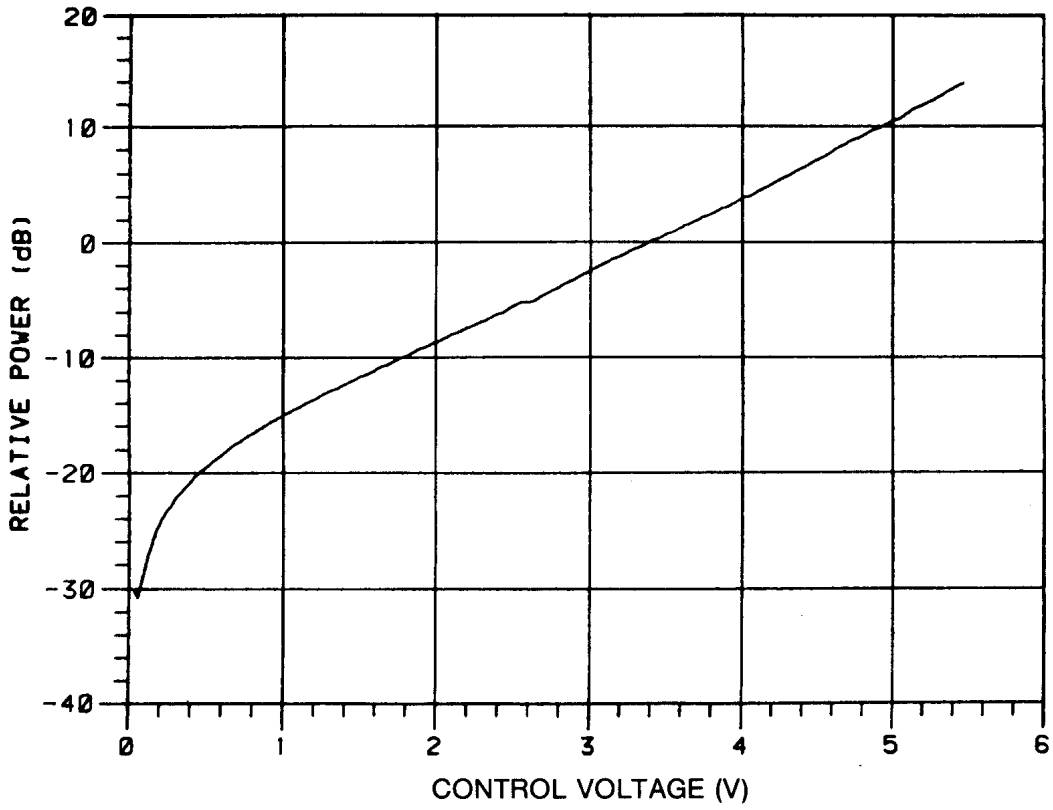

Figure 13. MPLL Transfer Function Simulation

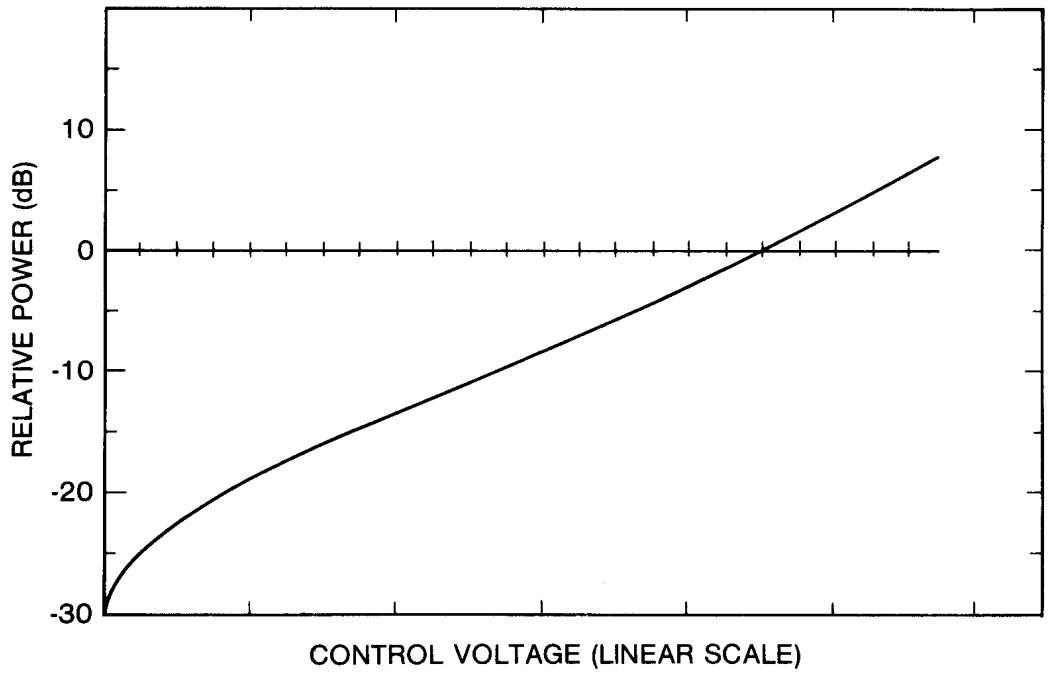

Figure 14. Measured MPLL Transfer Function