# IF DBPSK Modems Design for Command Link and Telemetry Systems

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## ABSTRACT

In this paper, the 70 MHz IF differential binary phase shift keying (DBPSK) modem is designed and implemented. At the transmitter, the data are first differentially encoded, and then sent to the binary phase modulator, which is followed by a delicatedly designed band pass filter to suppress the undesired sideband spectrum. At the receiver, the DBPSK signal is coherently demodulated by a Costas loop which is carefully analyzed and designed in this paper. In order to maintain the overall loop gain within a desired range for keeping a better loop performance, an IF preconditioning AGC (Automatic Gain Control) circuit is added in the demodulator to keep the IF amplifier output level almost constant even at low signal to noise ratio. In order to improve the false lock due to the data sideband, especially for low rate modems, and to enhance acquisition, a modified Costas loop and an automatic sweep search acquisition circuit are included in the demodulator.

Besides the carrier recovery, the bit rate clock must be recovered from the received DBPSK signal. Instead of serial processing, i.e., clock recovery comes after carrier recovery, a parallel processing of the received DBPSK signal is employed, i.e., clock recovery is parallel to carrier recovery. In other words, the carrier and clock recovery circuits independently process the same received DBPSK signal at the same time. The advantages obtained from the parallel processing are faster overall system acquisition and reduction of information loss. The recovered clock is derived from a bandlimited DBPSK signal by an envelope detector followed by a phase-locked loop (PLL). The key features of this suboptimum clock recovery circuits are simplicity and low cost for practical hardware implementation.

An example for modem design will be given and the modem will be implemented and then tested. Parameters selection and hardware implementation of important building blocks in the modem circuit are all given careful consideration. Furthermore, the block of the IF AGC, modified Costas loop scheme and sweep search circuits will also be described

with emphasis on their key functions. Finally, the bit error rate performance of the experimently implemented modem will be tested and presented.

## I. INTRODUCTION

Since digital modulation method has become more and more popular in transmitting the data in command link and telemetry systems. The DBPSK is the most often employed technique in digital modulation due to the fact that it can not only offer a lower probability of bit error rate for a given signal to noise ratio, but also avoid the phase ambiguity in the demodulator. For coherent detection, a locally generated reference carrier whose phase must closely track the phase of the carrier signal at the transmitter must be generated at the receiver. Because the DBPSK signal is a signal with carrier suppressed, the conventional PLL is not applicable to carrier recovery. A nonlinear process must be employed for DBPSK signal to generate the reference carrier. Costas loop is a common method for carrier recovery. In addition to carrier recovery, bit rate clock must be derived to differentially decode and/or descramble the received data. The bit rate clock is derived by a suboptimal method for simplicity.

## II. SYSTEM DESCRIPTION

Fig. 1(a) shows the modulator configuration of the IF modem employed in this paper. The optional scrambler is used not for security, but for increasing the transition density of the NRZ data stream, and thus enhancing the stability of the bit synchronizer. In order to resolve the phase ambiguity involved in the Costas loop, a diffenertial encoder is added in the modulator. Binary phase modulator is a balance mixer in which the phase of IF carrier is changed between $0^\circ$ and $180^\circ$ depending on bit “0” or bit “1” is sent from the output of differential encoder. Then, DBPSK signal output from modulator is amplified and filtered by IF amplifier and filter.

Fig. 1(b) shows the block diagram of the demodulator. The received DBPSK signal is passed through IF bandpass filter, and then it is amplified by a three-stage IF amplifier whose output level is controlled by a preconditioning AGC circuit. The block diagram enclosed by dashed-line is the part which is mainly interested and will be described in detail in the subsequent sections.

## III. CIRCUIT DESCRIPTION OF COSTAS LOOP

The equivalent circuit of the Costas loop is identical to the squaring loop [1] which is a PLL preceded by a squaring device. Thus conventional PLL design principles can be applied to the design of Costas loop. Fig. 2 shows a little bit detailed block diagram

which includes main Costas loop and its associated acquisition aid circuits (i.e., acquisition aid sweeper, false lock detector and control circuits).

It shows a very common implementation used in uncoded system for Eb/No (bit energy to noise density ratio) ≥ 10 dB, called the hard-limited or polarity loop. Ritter [2] has shown that the optimal phase estimator requires a tanh (kEb/No) nonlinearity following the in-phase data arm filter. For large values of Eb/No, tanh(x) equals the polarity or sign of x(±l), and can be implemented with a hard limiter. Simon [3] has shown that the inclusion of a limiter introduces a signal suppression factor into the analysis which could improve or degrade performance. Results from [3] indicate that for high Eb/No there is an actual improvement in the loop's squaring loss, on the order of 0.5 dB for Eb/No ≥ 10 dB and NRZ data. Also inclusion of the limiter in the in-phase arm allows substitution of a switching chopper multiplier for the typical analog four-quadrant multiplier, with its inherent DC drift stability improvement.

Cahn [4] suggested a modified Costas loop by removing the quadrature arm filter of an analog Costas loop in order to improve frequency acquisition and aid in removing false lock. Cahn has shown that the loop acts like a composite AFC/Costas loop combination. In practical implementation, quadrature arm filter is usually very wideband because it is designed only to remove the double IF frequency term. Loop filter is an important portion in the Costas loop design. To maintain a better loop stability and keep analysis simple, we choose the active lead-lag filter with transfer function

$$F(s) = A\,(1 + \tau_2 S) / (1 + \tau_1 S)$$

A: DC voltage gain

$\tau_1, \tau_2$: pole, zero time constants

Instead of using a VCO (Voltage Controlled Oscillator), a VCXO (Voltage Controlled Crystal Oscillator) is employed to reduce the phase jitter.

Fig. 3 shows the flowchart of operation algorithm of the Costas loop. In the beginning, the acquisition mode is activated, the modified Costas loop is employed. The quadrature arm filter is removed to achieve significant improvement in false lock performance. Furthermore, an all zero pattern is periodically inserted into the transmitting data stream at modulator as a pure carrier preamble for Costas loop acquisition and requisition [5]. Thus false lock is not a serious problem, carrier sweeping (if added) is an efficient acquisition aid to reduce the acquisition time. False lock detector [6] is included in the false/true lock detector to determine whether the loop is in false lock or not. This false lock detector only detects the false lock due to the sideband frequency half bit rate offset from the carrier frequency. The loop is broken for a moment then connected again when false lock, which is not likely to occur in our design, is detected. If true lock is detected then the loop

enters into the tracking mode and the sweeper is turned off. The bandwidth of quadrature arm filter is switched to a value close to the optimum one in order to reduce tracking jitter.

## IV. DESIGN PROCEDURE AND CONSIDERATIONS OF COSTAS LOOP

There is a compromise between carrier phase jitter $\sigma_\phi$ (relevent to probability of error Pe) and acquisition time Tacq. All of the carrier recovery techniques always exhibit phase jitter, which degrades the overall system's probability of error. Holmes [7] has plotted figures showing the approximate performance degradation due to imperfect carrier recovery. Those figures show the Pe as a function of Eb/No for various values of static phase error $\theta_v$ with total rms phase jitter $\sigma_\phi$ as a parameter.

Fig. 4 shows a design procedure for Costas loop. First of all, the Pe requirement is considered for the given Eb/No, Rs (data rate), $\Delta w$ (frequency uncertainty) and $\Delta \dot{w}$ (frequency sweeping rate). We choose proper $\theta_v, \tau_\phi$, given Eb/No to meet the required Pe from Holmes' plotts. Then kv and BL (loop bandwidth) can be calculated.

A high probability of lock will be obtained for a loop signal to noise ratio of +6 dB or better. Another important consideration is that the calculated BL be at least an order of magnitude less than the data rate, otherwise the Costas loop would track each data bit transition, thus never achieves demodulation of the data stream [8].

As a practical matter, for uncoded systems where Eb/No > 10 dB there is little to gained by implementing arm filters more complex than Butterworth 2 poles, which result in a squaring loss (SL) a couple of dB. In this paper, 2 poles Butterworth arm filters with bandwidth from 1.4 to 2.0 data rate are always chosen. $\xi$ is properly selected from the desired loop's transient characteristics. To maintain real values of resistors and capacitors, some constraints to $\xi$ which are shown on Fig. 4 must be met for the lead-lag loop filter design.

If $\Delta w_3 < Wn^2$ and wL (lockin range)$>\Delta w$ then Tacq is calculated by $Tacq = \Delta w^2/(2\xi wn^3)$. If the calculated Tacq is smaller than the required Tacq, then the loop can track the frequency sweeping rate. The frequency acquisition sweeper is not needed in this kind of application. If the loop can not track the frequency sweeping rate, then sweeper must be added. The sweeper's sweeping rate is designated as R90 on Fig. 4.

## V. BIT SYNCHRONIZER

### 1. CIRCUIT DESCRIPTION

Fig. 5 shows block diagrams of the bit synchronizer used in this paper. The envelope of the received DBPSK signal will drop to zero at phase reversal points when it is passed through a bandlimited prefilter. The envelope of the filtered DBPSK signal preserving the data rate information can be used to generate bit rate clock. A signal with data rate equal to transmitted data rate (Rs) is detected from the envelope detector. This signal is sent into transition detector to produce RZ (Return to Zero) signal which doubles the data transition density of transmitted NRZ data. Finally, the RZ signal is sent to the high Q filter which is realized by a PLL. Then the bit rate clock is derived from the output of the PLL.

### 2. DESIGN PROCEDURE AND CONSIDERATIONS

Since the bit synchronizer is realized by a PLL, the design principles are similar to those of Costas loop, the design procedure is not listed here. For NRZ data with very long "0" or long "1" sequence, an optional scrambler can be added at modulator to increase the data transition density for enhancing the stability of the bit synchronizer.

## VI. DESIGN EXAMPLE

Requirement: Design a 70 MHz modem with $Pe \leq 10^{-4}$, $Tacq \leq 1.0$ sec, given frequency uncertainty ($\Delta f$), including Doppler and oscillator instabilities ±20 KHz, maximum Doppler rate ($\Delta f$) ±0.1 KHz/sec, $Eb/No \leq 13$ dB, data rate (Rs) 9.6 Kbit/sec.

Solution; Choose $\sigma_\phi^2 = 2.7 * 10^{-3}$ rad $\quad \theta_v = 0.157$ rad

then $kv = 8 * 10^5$ $\quad$ BL = 526 Hz

Choose $\xi = 0.707$

then wn = 991.88 rad/sec $\quad$ wL = 1.4 krad/sec

It does not meet the requirement if the loop acquires by itself Tacq=11.43sec

If sweeper is added with sweeping rate R90 = 150 KHz/sec then the Tacq is calculated as $Tacq = \Delta f / (R90 - |\Delta f|) = 0.27$ sec which meets the requirement.

Choose kd = 0.4 V/rad, $\quad$ kv = 4 KHz/V, F(0) = 80

then $\tau 1 = 0.8$ sec $\quad$ $\tau 2 = 1.75$ msec

Fig. 6 shows the results of probability of bit error Pe versus Eb/No. It indicates that the Pe meets the requirement, but with degradation of 3-4 dB in Eb/No compared to the ideal Pe.

## VII. CONCLUSION

Design procedure and consideration of 70 MHz IF DBPSK modems with Costas loop are presented in this paper. A design example is given and then the designed modem is implemented and its bit error rate performance is also tested.

False lock of Costas loops caused by arm filters distortion of the data is a serious problem during loop acquisition if offset frequency between input DBPSK carrier frequency and VCXO frequency larger than half of data rate. Field test had proved that Cahn's proposal [4] offered a method for false lock improvement. Though many other false lock avoidance methods have been suggested, Cahn's method is employed by us for its hardware simplicity, i.e., no additional circuitry is required.

This design guides for Costas loop is applicable to many other applications.

## VIII. REFERENCES


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7) Jack K. Holmes, “Coherent Spread Spectrum Systems” Wiley-Interscience, 1982, Chapter 6.

8) Robert Hennick, “Demodulate DPSK Signals Coherently Using a Costas Phase-Lock Loop” EDN, July 1, 1972, pp. 44-47

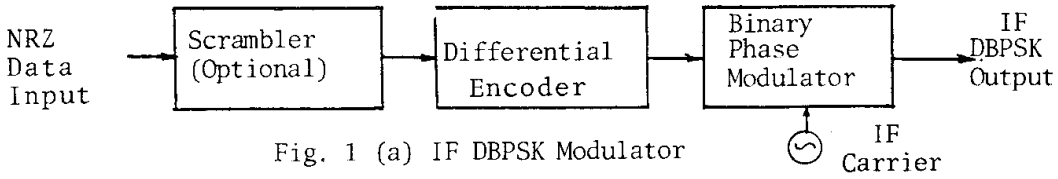



Fig. 1 (a) IF DBPSK Modulator

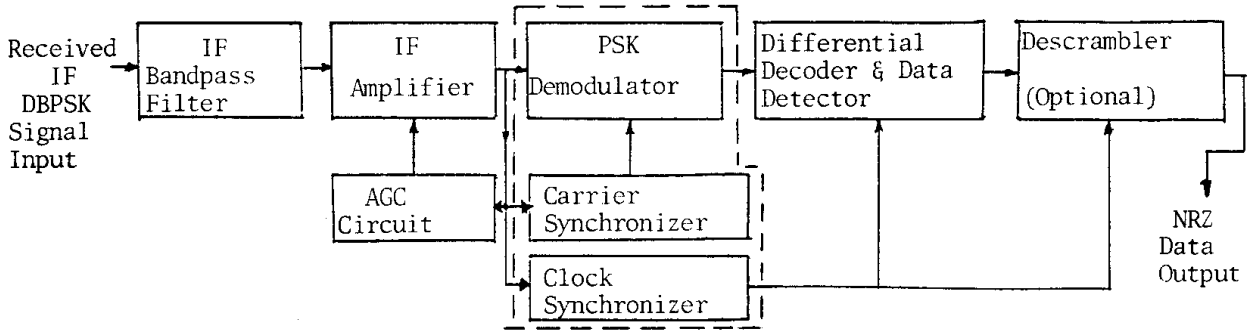



**Fig. 1 (b) IF DBPSK Demodulator**

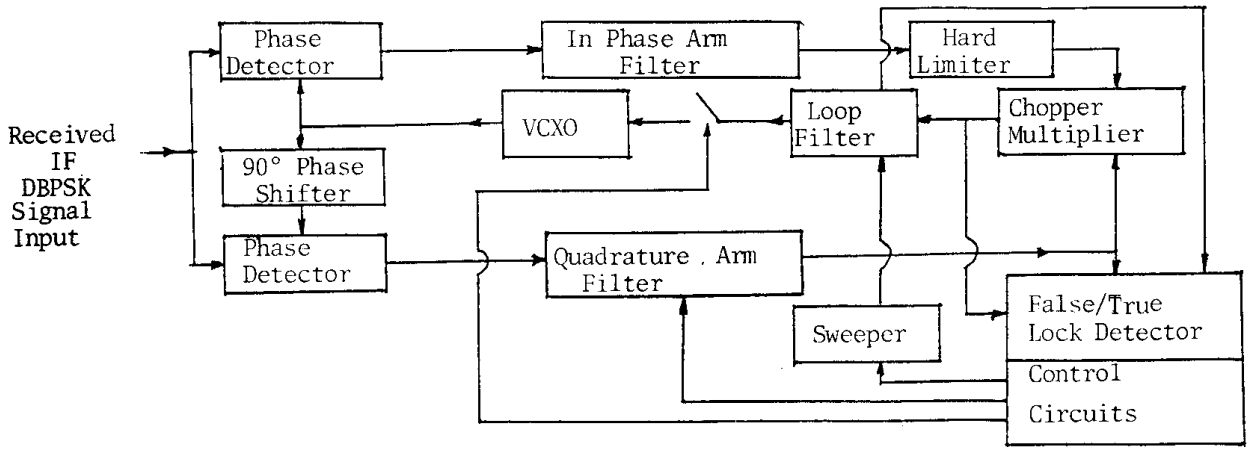



**Fig. 2 Costas Loop & Acquistition Aid Circuits**

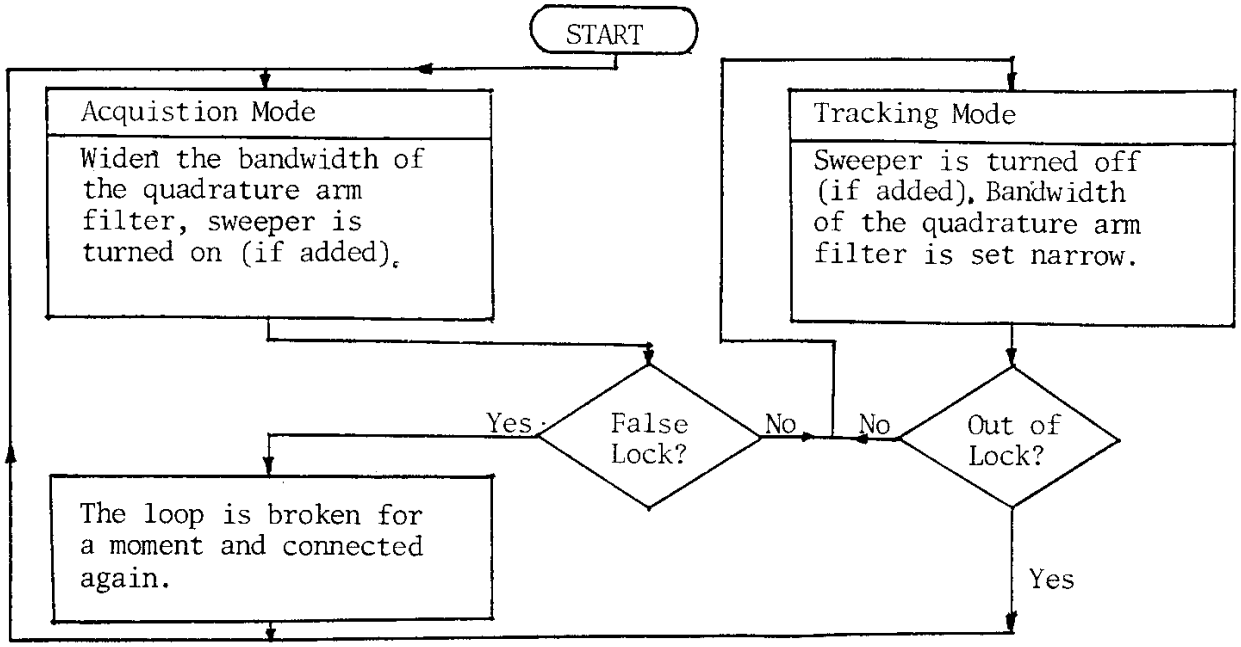
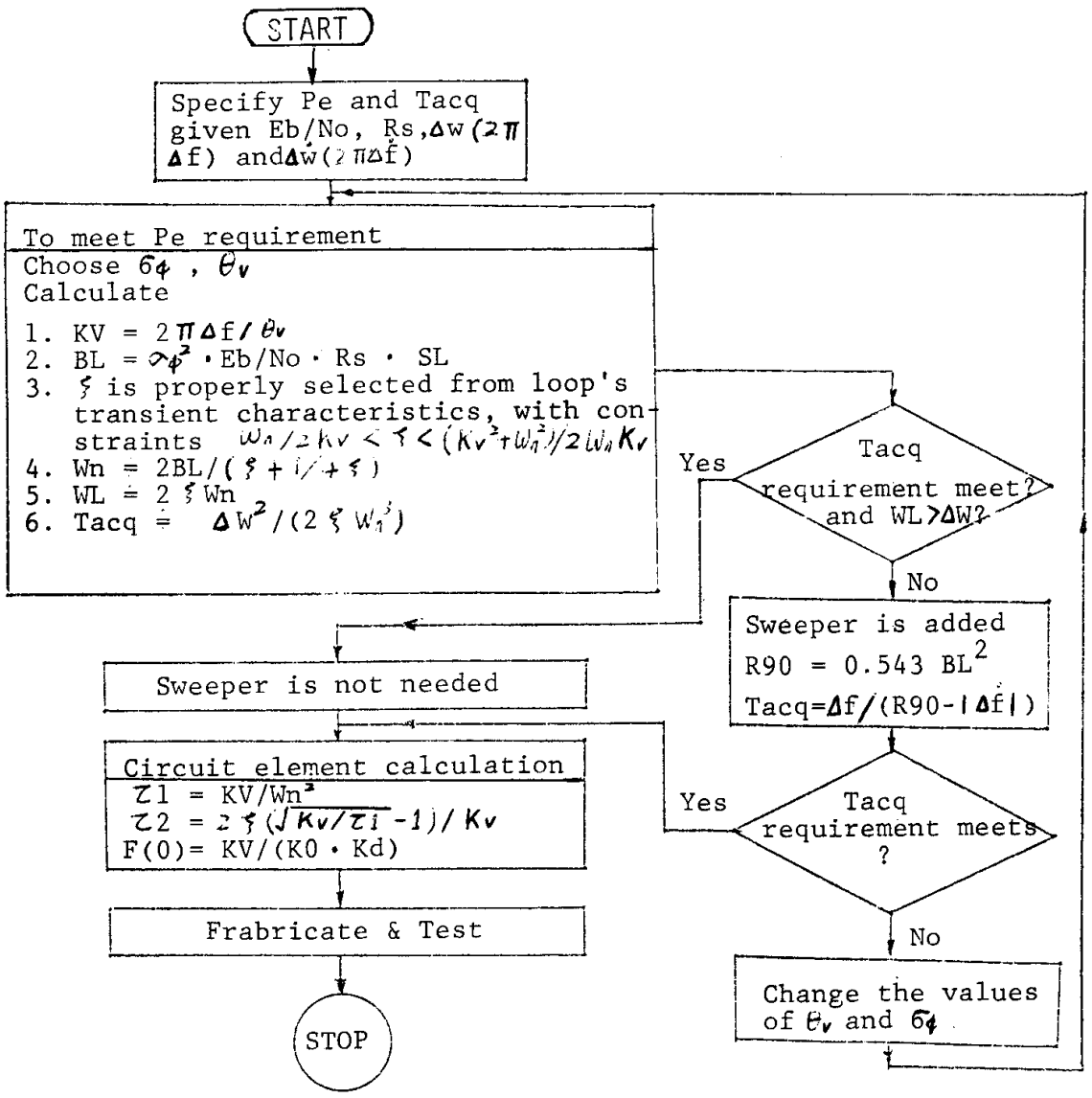



**Fig. 3 Flowchart of Loop's Operation Algorithm**




Pe: probability of bit error
Tacq: acquisition time (sec)
Eb/No: bit energy to noise density ratio (dB)
Rs: data rate (bit/sec)
$\Delta W$: frequency uncertainty (rad/sec)
$\Delta \dot{W}$: frequency sweeping rate ($rad/sec^2$)
WL: lockin range (rad/sec)
KV: DC loop gain
$\theta_v$: static phase error (rad)
BL: one-sided loop bandwidth (Hz)
$\sigma_\phi^2$: mean squared phase jitter ($rad^2$)
SL: squaring loss (dB)
$\zeta$ : damping factor
Wn: natural frequency (rad/sec)
R90: sweeper's sweeping rate with 90% probability of acquisition(Hz/sec)
$\tau 1, \tau 2$: time constants of loop filter (sec)
Kd: phase detector gain (V/rad)
K0: VCXO gain (rad/sec/V)
F(0): DC gain of loop filter

**Fig. 4 Design Flowchart of Costas Loop**

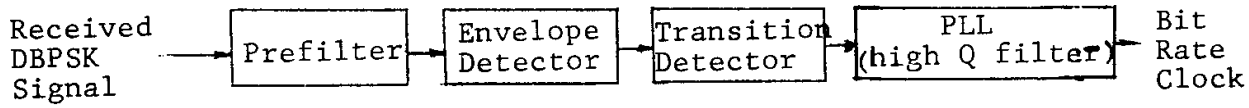



**Fig. 5 Block Diagram of Bit Synchronizer**

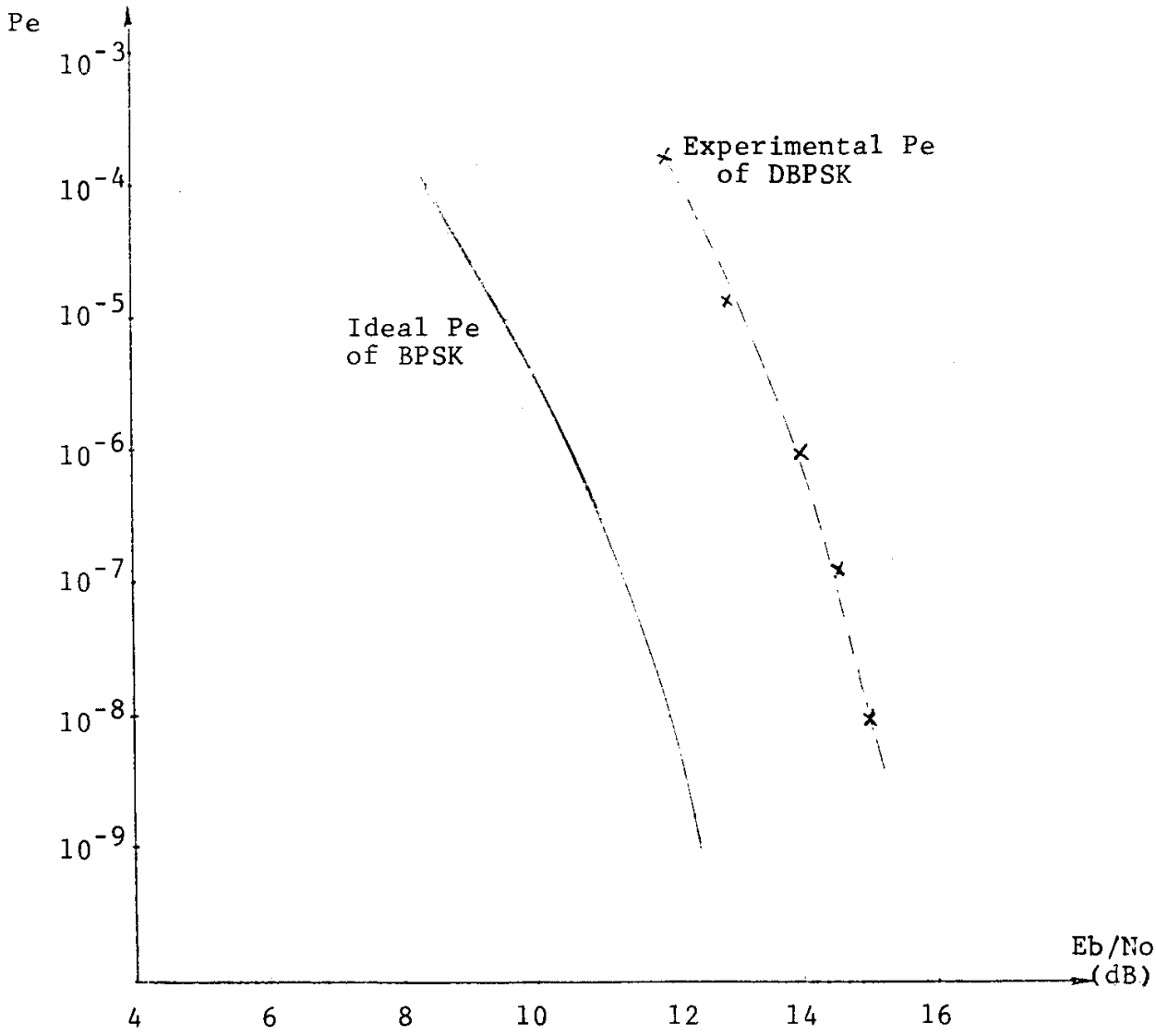



**Fig. 6 Probability of bit error Pe for experimental DBPSK modem**