AN APPROACH TO TELEMETRY SYSTEM ARCHITECTURE

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Abstract: Availability of low cost microcomputers, LSI devices have made it necessary to recast the architecture of aerospace telemetry system to realize all the attendant benefits. System constraints and the resultant hardware design are described in this paper.

Introduction: Motivation behind the evolution of any avionics hardware is to achieve reduction in operational support and life cycle costs. From an architectural standpoint, these requirements translate to the use of low-power/off-the-shelf LSI, reduced device diversity and built-in-test capability. A detailed description of the architecture of an onboard telemetry system with supporting ground based hardware based on the above principles is the subject of this paper.

Part I develops the architecture of the onboard system based on system requirements. It shows that a distributed system meets all the operational constraints of a multistage launch vehicle. In addition to standard components such as multiplexers and encoders use is made of a microcomputer at each data acquisition node for relaxed sampling, data buffering, packetization and to provide adequate self test capabilities.

Part II describes the ground based decommutator. It is seen that the function of a decommutator can be split into five independent sub-functions. Each of these is built around a microcomputer nucleus which performs the functions of initialization and realtime computing. Some of the functions performed in LSI are clock synchronization, pattern correlation and data packet identification.

Part III describes the low cost tools realized for supporting the development.

Part I. ONBOARD SYSTEM

Present day launch vehicles are configured as multistage rockets to maximise the payload boost capability of the launcher. It becomes logical to configure the onboard telemetry system as a distributed data acquisiton system. A data acquisition node will be located in each stage and the encoded information is sent to the upper stage as a serial digital bit stream for final multiplexing and tagging with identification data.

The most important problem to be overcome is related timing accuracy. Hardwired telemetry system provide precisely timed sequences for collecting telemetry data. Particular measurements are sampled at specific times in the commutation cycle, and the timing cannot change. Commutation cyclces in processor based systems are software controlled and as such, are subject to timing variations caused by such things as servicing interrupts, updating program parameters, and execution of subroutines.

Onboard telemetry information can be put into two classes - analog and digital. Analog signals are quantized and buffered before multiplexing whereas digital signals are directly buffered. Aliasing considerations require that analog data be sampled 3-4 times the signal bandwidth and digital data be sampled at least 2 times the buffer fill rate to prevent overflow.

Each data acquisition node consists of an analog multiplexer-encoder and FIFO to buffer analog and digital data respectively in addition to a microcomputer with 2 M bps SDLC capability. (Such as Intel 8744). The master microcomputer system located in the upper most stage sends an address packet to each slave station on a cyclic basis. A slave station responds by emptying its buffer over the common serial line as a SDLC data packet. Simultaeously the slave station is initialised to sample and buffer the analog and digital data. Then every frame period the entire process is repeated. It should be noted however that super-commutated signals undergo some distortion due to uneven sampling. (This is true of most present day telemetry systems).

The primary station receives and buffers serial data, strips the header and adds format words such as sync. code, ID number and ensures a constant rate of transmission on the downlink.

The major difference between the existing and the new data acquisition can be described as follows: In the existing system primary station sends a channel address on the serial bus which is decoded uniquely by a slave station and the quantized signal is sent back serially as the reply. The major disadvantage of this method is the small time available in completing this procedure resulting in the need for relatively high speed analog circuits. In the proposed system, quantization of the local group of signal proceeds independently of the serial bus actively and needs to be completed only within the buffer fill period which is almost equal to the frame period. This results in per channel quantization time being decreased 5-10 times. Super and subcommutations are implemented under software control at each slave microcomputer. This requires the current frame number being available at each secondary site. This information is communicated to each secondary station as part of data transfer initiation procedure. Primary/Secondary communication will take place over an optical fibre link.

Part II. DECOMMUTATOR

Telemetry information after passing through the space link gets received and demodulated. It will be a noisy and distorted version of the onboard signal. It is taken through regenerating and synchronising decommutator subsystems before acceptance by data processor. A telemetry ground station incorporating the above elements has to be versatile in order to give mission support over its intended lifetime. Availability of LSI has had a significant impact on the physical design and functionality of decommutators. Pre LSI implementation had a device count of 8000 and had used 200 different types of devices. Decommutator consists of bit synchroniser, frame synchronizer, digital to analog converter and demultiplexer/data processor interface.

Bit synchronizer (BS) consists of an integrate and dump circuit (matched filter) PLL Bit rate generator, signal conditioning circuits and sync. monitors. All functions have been implemented as digital functions. The major difficulty faced was in the implementation of the integrate and dump filter. Bit periods can be as low as 500 nS. System analysis indicates a requirement of 4 bit quantization and 16 point sampling of the signal during a bit period. This translates to encoding speed of 32 Megsamples/Sec. at 4 bit accuracy and subsequent accumulation at this rate. To keep the front end simple the antialiasing filter has not been made tunable. This results in a variable length accumulator since the number of samples accumulated is inversely proportional to the bit rate. Thus a scaling network is needed so that only normalized result is passed on from the accumulator for further processing.

A unique alogirthm has been developed for the bit sync. acuqisition process. Acquisition is possible at any offset of gain, level, frequency (less than 10%) and phase between the incoming signal and the local estimation. A novel successive approximation technique has been developed for robustness in estimation procedure. The procedure has been simulated and verified for robust performance under expected conditions. With this algorithm BS acuqisition is completed within 100 bits in the worst case.

Frame synchronisation consists of a correlator, counters and status monitoring circuits. The local microcomputer does parameter set up and participates in subframe sync. acquisition and tracking. A special buffer memory is provided which can store a complete frame and which can be readout in a burst mode under polled conditions. This feature is useful for combining different telemetry bit streams into a single data stream. A typical ISRO launcher has 2-3 telemetry data streams. During checkout as well as for in-flight recording purposes a combined telemetry data stream is very convenient for data handling.

Digital to analog converter is useful in providing a hard copy output of a selected for quick look purposes. DAC consists of a content addressable memory (CAM) and individual analog converters. CAM is realised using available RAMs and the channel selection information is written into the RAM by the local micromputer. During initialization a token is put at the memory location corresponding to the location in the frame of the selected word. During demultiplexing the RAM address counters are driven by the rate pulses and generate word/frame addresses in real time. The memory output is directly used for latching data prior to analog conversion.

The Microcomputer chosen for decommutator has been Z8 made by Zilog. In order to reduce cost and improve reliability the production model would have a ROM version of Z8. To customize each Z8 for its application, Z8 reads a pattern of 1's and 0's stored at the input of a local shift register during power-on initialization.

Trouble shooting will be done by replacing resident microcomputer with an emulator and running a diagnostic program. These programs have been written as part of the development process. Development of sub-system starts with a minimal microcomputer configuration and incrementally adding hardware and the corresponding software drivers.

It has not been possible to include detailed hardware/software description for each subsystem. However the design approach toward simulator implementation is given as an example. PCM Simulator consists of a pattern generator and format rate pulse generators. These functions are realized roughly in microcomputer and LSI resident programmable counters respectively.

Pattern generator is a 16 bit feedback shift register which can be loaded by Z8 under external timer control. Normally the shift register will be outputting pseudo random data sequence. When unique words such as frame sync. pattern, Identification word, special word are loaded into the shift register automatic serialization takes place. The location of these words is determined by the overflow of the counters which are fed to a PROM base address table and which in turn interrupts Z8 with an address. Z8 in turn loads the data pointed by the interrupt into its I/O pins. 16 bits later this pattern is loaded into the shift register. This technique avoids the variable delay in the data generation normally associated with microprocessor based system.

Part III. DEVELOPMENT TOOLS

At the start of the development program only Z8 was commercially available and work was concentrated on decommutation elements where interprocessor communication requirements are not demanding. Z8 has a plug in socket for loading PROM. During initial stages it was expected that PROM would have to be removed and reprogramme several

times. An elegant alternative was developed using a static RAM configured as a dual port RAM which could be written through an interface form a terminal and which would be read by Z8 in normal operation. Since the terminal to RAM interface can support only Hex and a few control characters all programming had to be done in HEX. This did not prove to be an efficiency bottleneck in practice mainly because programs are short in length (typically 500 bytes).

PRESENT STATUS AND CONCLUSIONS

Breadboard models of frame sync., DAC, Simulator have been realised. Computer verification of BS performance has also been completed. Onboard system realization will be taken up after Intel 8744 becomes available (end of 1986). Proto models of ground based decommutator are scheduled for completion this year.

A cost effective way of realizing 1 Mbps PCM telemetry system has been described. It is seen that although data rates are high, it is possible to realize a workable system by a combination of microcomputer, special purpose LSI, and programmable array logic. Device count and diversity have been reduced by a factor of 50 compared to earlier realizations. The proto model of decommutator is proposed to be realized as a plug-in card for standard PCs thereby realizing low cost desk top decommutator/telemetry checkout systems. Onboard system will reach flight usage status after highrel version of 8744 becomes available.