DATA ACQUISITION TECHNIQUES USED FOR MIL-STD-1553 DATA

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ABSTRACT:

This paper will address various applications and methods used for the acquisition, recording, and telemetering of data from the MIL-STD-1553 avionic multiplexer data bus installations in aircraft, missiles, and other vehicles. Discussions of the problems encountered and hardware utilized in current applications are reviewed. The innovative techniques used to optimize system performance, and future trends for program requirements are also discussed.

INTRODUCTION:

In recent years it has become increasingly apparent that the telemetry data acquisition industry is being required to interface with existing Avionic data busses. These bus types extend from the commercial standard ARINC 429 bus to the military 1553 multiplex bus. This requirement has caused some concern for the Test Range Stations due to the expense of modifying existing equipment, therefore it has become the responsibility of the supplier to design and produce data acquisition equipment that is compatible with IRIG-106 standards.

The data bus monitor will soon be required to be capable of performing such functions as system error detection and correction functions, system reconfiguration for degraded modes of operation, and may also be required to have the capability to perform secondary bus controller functions. The bus monitor is the ideal bus terminal selection to incorporate these types of features to perform these types of functions.
VARYING APPLICATION REQUIREMENTS:

Input requirements;
The requirement to interface data acquisition monitors to avionic systems has extended beyond MIL-STD-1553A and MIL-STD-1553B busses. Prior to the development of the Aircraft Internal Time Division Command/Response Multiplex Data Bus specification (MIL-STD-1553), the military aircraft industry had designed, developed, and implemented numerous different multiplex data bus system schemes. Fortunately the majority of these bussing schemes have exhibited similarities in their performance characteristics and electrical parameters. Some of these bus types include but are by no means limited to the following:

a. MIL-STD-1553A
b. MIL-STD-1553B
c. MIL-STD-1553B / USAF Notice 1
d. DEF-STAN 00-18
e. 81-1057 GRMK.5
f. MACAIR 3818
g. F-18 Armament bus
h. H009

Some of the data busses that have required data acquisition interfacing in the past and must continue to be supported include:

a. ARINC 429
b. RS-422
c. RS-232C

Data processing requirements;
Since the telemetry industry acceptance of MIL-STD-1553, the system applications have become more demanding and the design approaches have been required to stay abreast of the fast moving technological advancements. The methods of processing the received input data has as many, if not more, application dependent requirements as there are input and output types. Hence, the design approaches that can be utilized to accomplish the task requirements is directly proportional to the number of design engineers in the data acquisition field. Recent system specifications have required data processing approaches to satisfy some of the following applications:

a. all data to be retrieved from the input data bus
b. selected data messages to be retrieved from the input data bus
c. selected data words to be retrieved from the input data bus
d. interfacing with up to as many as six (6) input busses  

e. interfacing with different types of input/output data busses simultaneously  

f. increased data storage capacity and faster access times  

g. electrically eraseable programable memory features  

h. on board data reduction, manipulation, and/or calculations  

i. increased data through-put and operating speeds  

j. lower operating power requirements and heat dissipation  

k. slaved and/or standalone bus monitor systems  

Output requirements;  
Just as the input requirements are application dependent but remain similar, in performance, so have the output requirements become application dependent, but similar, in performance. This similarity is due in most part to the acceptance of the Inter-Range Instrumentation Group Standard (IRIG-106). Although the majority of the applications for data acquisition bus monitors require IRIG-106 compatibility, the broad scope and flexibility of the standard allows the end user to specify a wide range of output requirements. Some of the more recent output requirements include:  

a. up to four (4) output ports of selected data for split track recording  

b. a single output port of all data for in-flight recording  

c. premodulated output data for transmission  

d. single or multiple output ports for interfacing with instrumentation data acquisition systems  

e. parallel data output ports  

In addition to the application variations listed above all of the serial data streams can also be specified in a variety of standard formats such as:  

a. NRZ-L data  

b. premodulated NRZ-L data  

c. DM-M coded data  

d. premodulated DM-M data  

e. Randomized NRZ- L data  

f. premodulated randomized NRZ-L data  

g. computer backplane interface, etc.  

Environmental requirements;  
Typically, the flight test industry has not been required to meet the full military operating environment, however, this relaxation is rapidly being updated to reflect the standards presently in use by the avionic industry. This is not to imply that existing flight-test equipment cannot meet or exceed these environmental requirements, but the level of
confidence to successfully demonstrate compliance to these types of avionic environments is extremely low in some equipments. Consequently, to insure continued equipment usage and failure free operation many of these environmental requirements are being invoked in new procurement specifications. The environmental requirements being invoked are still application dependent, but are dictated by the vehicle platform and mission profile. The existing vehicle platforms and respective environments are well documented and merely listed here to illustrate the broad range of application dependent test levels that are available.

a. airborne inhibited environment
b. airborne uninhabited environment
c. manned space environment
d. unmanned space environment
e. rocket/missle mounted
f. etc.

**Equipment packaging requirements:**
The variations that effect packaging are, once again, directly influenced by the system application and in particular the vehicle platform. The telemetry test group has, in most cases, been tasked with instrumenting the test vehicle with a minimal amount of available “real estate”. This restriction has dictated the use of innovative mechanical packaging approaches to reduce the overall size and weight of the system. The successfully proven techniques used in the past have included such ideas as the following:

a. stackable printed circuit boards
b. hybridization of discrete circuits
c. stackable hybrids
d. leadless chip carriers
e. multi-layer printed circuit boards
f. flexible-circuit boards

**FLEXIBLE APPLICATION SOLUTIONS:**
The nonrecurring expenses incurred during the development of a product can be minimized by insuring sufficient flexibility in the circuit designs.

**Input requirements:**
In the case of the input requirements the circuits which lend themselves to flexible designs can best be visualized by first creating a matrix of the data bus requirements to identify any similarities. Once a matrix has been completed the designer can then begin to group the data busses by electrical parameter similarity, and identify those input characteristics
that will require little or no circuit modifications to meet. These modifications may be as simple as a capacitor, resistor, or IC part number change.

Example 1:

<table>
<thead>
<tr>
<th>Xfmr input level</th>
<th>T/R response voltage range</th>
<th>application</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.86-14.0V, p-p, 1-1</td>
<td>0.0-0.2V, p-p, 1-1</td>
<td>1553B, notice 1</td>
</tr>
<tr>
<td>0.0-20.0V, p-p, 1-1</td>
<td>0.0-0.7V, p-p, 1-1</td>
<td>1553A, F-18</td>
</tr>
</tbody>
</table>

**direct coupled input**

<table>
<thead>
<tr>
<th>Xfmr input level</th>
<th>T/R response voltage range</th>
<th>application</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0-20.0V, p-p, 1-1</td>
<td>0.0-0.7V, p-p, 1-1</td>
<td>F-18, 1553A</td>
</tr>
<tr>
<td>1.2-20.0V, p-p, 1-1</td>
<td>0.0-0.28V, p-p, 1-1</td>
<td>1553B</td>
</tr>
<tr>
<td>not allowed</td>
<td></td>
<td>notice 1</td>
</tr>
</tbody>
</table>

**output levels**

<table>
<thead>
<tr>
<th>Xfmr input level</th>
<th>RL</th>
<th>application</th>
</tr>
</thead>
<tbody>
<tr>
<td>18.0-27.0V, p-p, 1-1</td>
<td>70 ohms</td>
<td>1553B, notice 1</td>
</tr>
<tr>
<td>6.0-20.0V, p-p, 1-1</td>
<td>unspecified</td>
<td>1553A</td>
</tr>
<tr>
<td>28.0-36.0V, p-p, 1-1</td>
<td>140 ohms</td>
<td>F-18</td>
</tr>
</tbody>
</table>

**Results;**
The bus monitor terminal does not normally require transmit functions therefore, for this example it will be ignored.

To design a flexible circuit that would require little modification to meet the above parameters and eliminate design costs now becomes a simple matter. Instead of using vendor supplied transceivers the input receiver can be designed to offer P.C. board jumper options at the input transformer coupler to comply with either transformer or direct coupling bus requirements. The secondary of the transformer is input to an LM-106 device or equivalent with its threshold resistors accessible, so that response and no response levels can be adjusted/modified with a simple resistor change.

**Data processing requirements**

This same technique can be used for determining similarities in the processing requirements of the various specifications. First, generate a systems requirements matrix, highlight similarities, and identify compatibilities.
Example 2:

Interface Requirements

<table>
<thead>
<tr>
<th>input type</th>
<th># of busses</th>
<th>output type</th>
<th>comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. MIL-STD-1553 A/B</td>
<td>1 dual redundant</td>
<td>NRZ-L to PCM unit</td>
<td>slaved unit</td>
</tr>
<tr>
<td>2. MIL-STD-1553 A/B</td>
<td>single channel</td>
<td>premodulated PCM</td>
<td>standalone</td>
</tr>
<tr>
<td>DEF-STAN 00-18</td>
<td>no redundancy</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3. MIL-STD-1553 A/B</td>
<td>2 dual redundant</td>
<td>VMEbus</td>
<td>computer hosted</td>
</tr>
<tr>
<td>GRMK.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4. MIL-STD-1553 A/B</td>
<td>2 dual redundant</td>
<td>single track</td>
<td>standalone</td>
</tr>
<tr>
<td>flight recorder</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5. MIL-STD-1553 A/B</td>
<td>2 dual redundant</td>
<td>NRZ-L to PCM unit</td>
<td>slaved unit</td>
</tr>
<tr>
<td>6. MIL-STD-1553 A/B</td>
<td>1 dual redundant</td>
<td>4 tracks flight recorder</td>
<td>standalone</td>
</tr>
<tr>
<td>7. MIL-STD-1553 A/B</td>
<td>1 dual redundant</td>
<td>single track</td>
<td>standalone</td>
</tr>
<tr>
<td>video recorder</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8. MIL-STD-1553 A/B</td>
<td>4 dual redundant</td>
<td>premodulated PCM</td>
<td>standalone</td>
</tr>
<tr>
<td>9. MIL-STD-1553 A/B</td>
<td>2 dual redundant</td>
<td>4 tracks flight recorder</td>
<td>standalone</td>
</tr>
<tr>
<td>H009</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results;

With the aid of example 1 it is becomes easy to visualize that there is only one input circuit that will be required to be designed to satisfy all of the applications listed in example 2. However, it is just as apparent that the output requirements vary significantly enough to warrant the design of 3 possibly 4 different output sections. These sections can be listed as;

1. data track spilting for up to 4 recorder tracks
2. NRZ-L data
   a. with premudulator
   b. without premudulator
3. computer interface (VMEbus)
In addition to this, the matrix also illustrated that the input decoding and output encoding requirements will differ for the applications but may have some common circuits. The only input Manchester decoding variation will be for the H009 application will require the design of a different circuit, therefore, the next step is to generate a matrix of these functional/control requirements. (NOTE: ARINC-429, RS-422 would also require unique input designs; the RS-422 and the RS-232 requirements could be grouped together.)

Example 3:

<table>
<thead>
<tr>
<th>Encoding/Decoding Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory capacity</td>
</tr>
<tr>
<td>1. 8 K x 20 bits RAM</td>
</tr>
<tr>
<td>2. 16 x 20 bits FIFO</td>
</tr>
<tr>
<td>3. 32K x 16 bits RAM</td>
</tr>
<tr>
<td>4. 2, 1K x 20 bit RAM</td>
</tr>
<tr>
<td>5. 2, 1K x 8 bits RAM per bus</td>
</tr>
<tr>
<td>6. 1024 x 23 bits FIFO per track</td>
</tr>
<tr>
<td>7. 16 x 20 bits FIFO</td>
</tr>
<tr>
<td>8. 4, 16 x 20 bits FIFO per bus</td>
</tr>
<tr>
<td>9. 8K x 20 bits RAM</td>
</tr>
</tbody>
</table>
Results;
This matrix clearly illustrates the compatibility and differences of the various applications. Memory requirements can be grouped into two major sections RAM and FIFO; other than this the main difference, is of course the size of data buffering for the particular requirement. The time tag requirements can be accomplished with a single circuit design. The output format/control sections illustrate that a variety of “core” circuit designs can be utilized, with minor modifications to satisfy the requirements listed above. The key to the output formatters is to design the format memory with sufficient flexibility to allow repeated use for varying applications. This can be accomplished in two ways, the first is to design the memory large enough to hold numerous formats, the second method is to design the format memory with EEPROM’s.

Environmental flexibility;
To insure compliance to specifications requiring operation in full military environments obviously begins with the proper parts selection, unfortunately some designers will stop at this step. To properly design equipment for a full military environment only begins with the selection of parts.

A proper design will include that the components within the circuits be derated in accordance to their circuit use, this is in addition to the derating that is placed on the components by the manufacturing and testing specifications.

In addition to the proper parts selection and derating criteria, a complete timing and circuit analysis should be performed to insure adequate error margins have been designed into the design. A complete circuit/worst case analysis will increase the users confidence that the equipment will operate without degradation over the full temperature range and will not fail due to component aging.

A thermal analysis is always a good practice, the results of this analysis is helpful not only to the reliability engineers but also to the mechanical engineers in the packaging of the equipment. This analysis will identify any thermal concerns at the beginning of a program before it becomes a severe and expensive problem.

Another analysis report that is extremely helpful to mechanical and design engineers is the EMI/EMC analysis. This analysis should be performed early in the design phase.

After these types of (minimal) analyses is completed the parts can be selected for the application and a single design will be testable to any environmental specifications and will exhibit a high MTBF calculation and long life. It should also be noted that these types of analyses should be updated throughout the design/development/production program to reflect all incorporated changes.
Packaging flexibility
As illustrated in the matrixes above the circuits which exhibit similarity in function can also be partitioned by similarity. In this way as new applications evolve the new designs of PC boards remains minimal, this not only reduces delivery lead time but also reduces the NRE cost for development.

With proper partitioning of the circuits a backplane bussing scheme can be used that eliminates the need for wire-wrapping of most signals. By maximizing the use of “core” designs and a bussed backplane scheme, the system can be configured for most any application by simply adding or removing the required PC boards. The majority of the time spent and expense incurred for a new development now becomes primarily a mechanical repackaging NRE.

In some applications the dimensional specifications will require that the circuitry and/or the unit must be hybridized. Once again a proper circuit design lends itself to this type of packaging, and the expense remains primarily a mechanical one.

FUTURE TRENDS FOR MONITORS
As the 1553 system applications mature the bus terminals are being required to perform/transfer system bus control functions, this is defined as a non-stationary master. These types of requirements have also introduced new areas of concern that the monitor is being required to flag and correct. The types of concerns that must be monitored are:

1. Bus Control Handover Failures;
   This type of failure can leave the system with no active controller, or with multiple active controllers. This type of failure will cause the system to halt.
2. Failure to Pass Bus Control;
   This type of causes the system to revert to a stationary master. The problem with this is that the active bus controller only has limited bus control information so the system is forced to operate in a degraded mode.
3. Failure to Control;
   This failure occurs when a terminal does not request or accept bus control when it should. The discrepancy with this type of failure is that the subsystems under its control can not pass or acquire data and appear to have failed.
4. Incorrect Selection of Next BUS Controller;
   This means the selection of the bus controller allocation has been violated, the result is that time-critical data is not serviced.

Each of these types of errors must be detected and identified, the perfect choice to perform these error detection and correction functions is the bus monitor.
Handover failures occur when the bus controller completes its assigned priority message and fails to transfer control. This failure can be detected by a lack of bus traffic. The distinctive feature of the non-stationary master is the almost constant bus activity. Even when no data is being transferred the controller is polling potential controllers to determine if a bus request has been posted. If a long period of bus inactivity (15.625 to 50msec.) exists on the bus, there may have been a handover failure and the bus lacks a controller. The monitor could be designed to pursue recovery procedures by transmitting an asynchronous message to the bus controller causing it to relinquish control. If the monitor is successful the control would be offered back to the same terminal for a second time, if control is accepted then recovery is complete, otherwise, the monitor would reconfigure the system. If after a predetermined amount of time the same terminal again gains control of the bus and fails to transmit or transfer control, the monitor would reconfigure the terminal out of the system.

Bus control failures resulting in a bus controller retaining control of the bus indefinitely is another area of concern. The monitor, once again, is capable of detecting this error because it is monitoring the system. Once a bus request is posted, bus failure during this period indicates either an ineffective or dominant bus controller. When the monitor detects this condition, it can wait for the next polling sequence and set its priority level to gain control. If the monitor requests control and this fails, the monitor must obtain direct control (i.e. using a discrete or alternate bus and re-configuring). If the monitor succeeds, control is offered to the highest priority bus controller. If an ineffective controller gains control of the bus and fails to relinquish it, the monitor reconfigures the terminal out of the system.

Subsystem or terminal failures can be detected without the use of the terminal or subsystem flags, for example; repeated message completion failures, bad data or non-varying data from a subsystem may be interpreted as a subsystem failure. System software, as opposed to bus control software, should be used to detect these and other failures.

The monitor must be capable of gaining control of the bus. To achieve this goal, each bus controller should gain bus control at least once each major frame for synchronous transmissions. For those applications where a bus controller has no synchronous requirements, the monitor must examine the health of the system via mode control commands to determine if system operation is satisfactory.