TELEMETERING OF A MISSILE BUS 1553 B

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1. INTRODUCTION

It is difficult to transmit directly the data circulating on a 1553-B bus by microwave link during a missile test, given that it is not a synchronous message.

For the ANS missile the AEROSPATIALE tactical missile division has decided to include the 1553 message in a PCM message to IRIG standards.

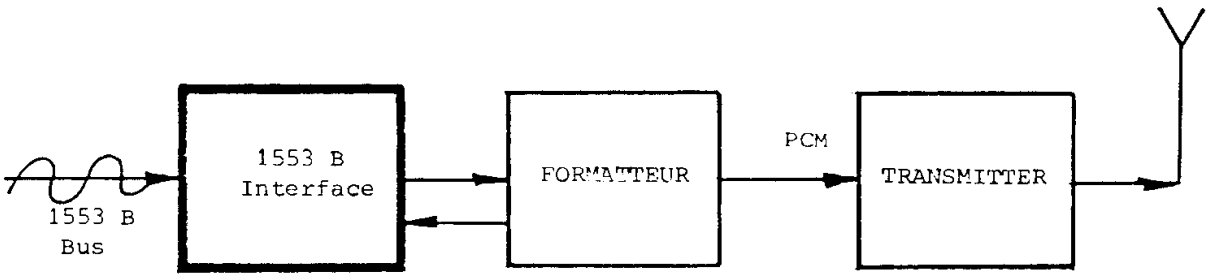
In view of the asynchronism between the traditional telemetering data and the bus message it has been necessary to develop a specific controller providing the interface between the bus and the IRIG PCM. This controller performs the functions of synchronization, encoding, structural analysis of message, adaptatin of the input speed to the PCM rate and also dating of the data.

Moreover, during tests on the missile, it is necessary to process the bus data on the ground. A conventional decommutator, although suitable for the usual analog channels, cannot be used in real time. It is therefore been necessary to develop equipment providing on the ground the reconstitution of a 1553 bus that can be processed by ordinary standard equipment.

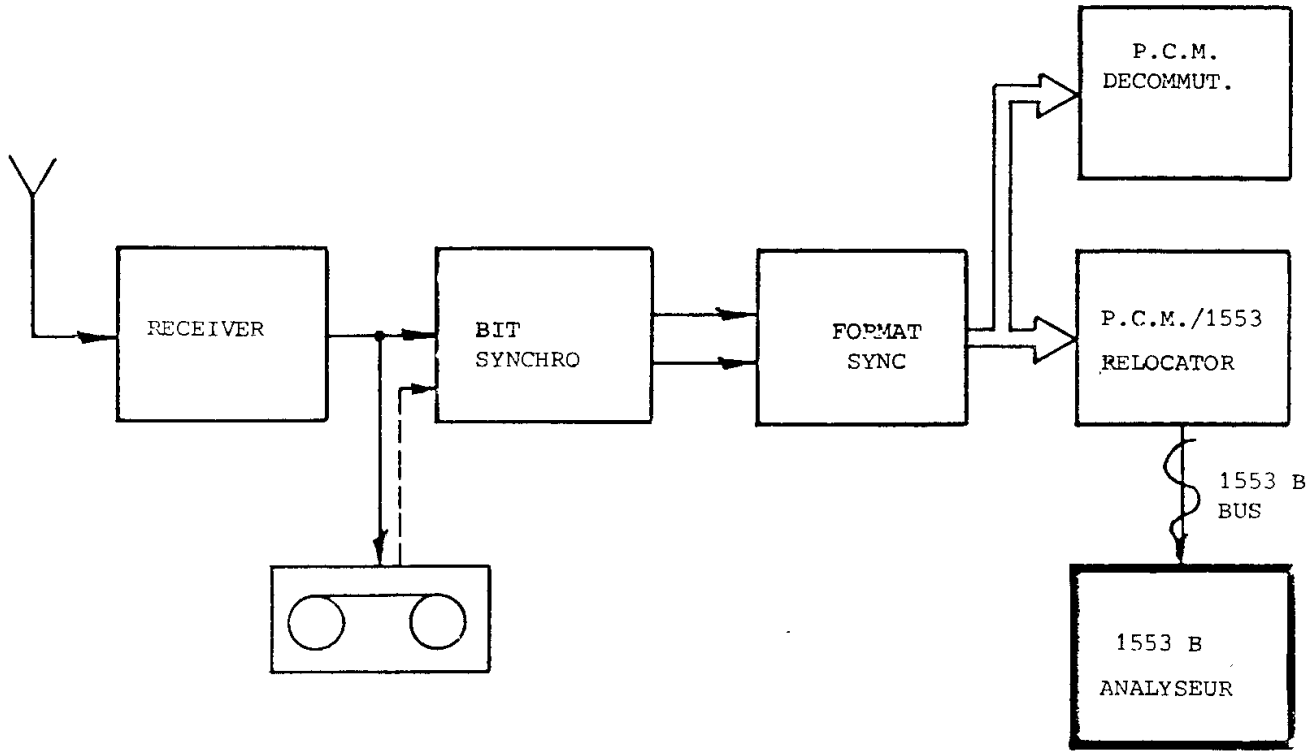
After synchronizing and sorting the data in the IRIG format the equipment creates three types of messages corresponding: to the missile message, to the dating and to the message found erroneous during acquisition on board.

2. PRINCIPLE OF THE LINK

The 1553 B controller connects the missile bus and is capable of recording all the data flowing in it. It therefore does not have any specific address at its disposal and is totally dumb. It can thus play its full part as spy.



ON-BOARD SEGMENT



GROUND SEGMENT

1553 B BUS TRANSMISSION

Progressively with the availability of the IRIG PCM format, the 1553 data are taken by the formatter in serial form. The latter can thus compose a message containing the encoding of the analog parameters and 1553 data.

The message thus created is sent to the ground via an S band transmitter associated to its antenna.

On the ground the signal received processed by the receiver is presented on the input of a magnetic recorder (offline processing or saving) or on the input of the bits synchronizer.

Then comes the format synchronizer which, coupled to a PCM decommutator, processes the purely IRIG data in real time.

In parallel on the PCM decomnutator format synchronizer, le PCM/1553 relocator takes the 1553 data which, after processing, are reconstituted to reform the missile 1553 bus. Dating data in 1553 message form are added to this bus.

The data of this reconstituted bus can then be decommutated in real time via ordinary standard equipment.

3. PRINCIPLE OF TRANSMISSION

The data transmission medium is any PCM/IRIG conventional format, only the length of the words is fixed at 8 bits with or without parity.

The analog encoded data are entered in the format in the usual way at fixed addresses. These parameters can have any computation The quantity of analog data that can be transmitted depends on the average speed of the 1553 B bus to be telemetered.

The encoded 1553 B data are entered sequentially inside the format at all the points left free by the analog parameters without any notion of addressing. Additional dating data are regularly placed between the 1553 B data.

If the speed of the 1553 B bus becomes insufficient to fill the format, special filling words completed.

3.1 1553 Message Encoding

The encoding has been adopted so as to limit the expansion factor (the pass band of the telemetering channel is limited to 1 MHz), encoding should also provide for synchronization research on the ground.

Each 1553 word generates three telemetering bytes. The composition of the bytes is as follows:

Sync	16 data bits	Parity
	4 status bits	

Byte 1	flag “1”	Byte 2	flag “0”	Byte 3	flag “1”

The four status bits have the following significance:

Bit A = “1” ; synchronization correct
Bit A = “0” ; synchronization incorrect
Bit B = “1” ; command or status word
Bit b = “0” ; data word
Bit C = “1” ; length of word transmitted = 20 bits
Bit C = “0” ; length of word transmitted < 20 bits
Bit D = “1” ; no biphase encoding error
Bit D = “0” ; biphase encoding error in the 1553 word transmitted.

3.2 Dating

It being impossible to send the 1553 data with certainty in real time, dating is inserted in the format.

Every 640 microseconds a dating request is deposited as of the arrival of an end of message, two dating bytes are inserted after the three bytes of the last 1553 word.

The dating data consists of a 14 bit word in binary (2^{13} to 2^{0}).

Byte 1 flag “1” Byte 1 flag “1”

The dating resolution is 20 microseconds.

In order to avoid loss of data in the case of the 1553 bus being heavily occupied, a buffer memory filling threshold is provided to inhibit dating.

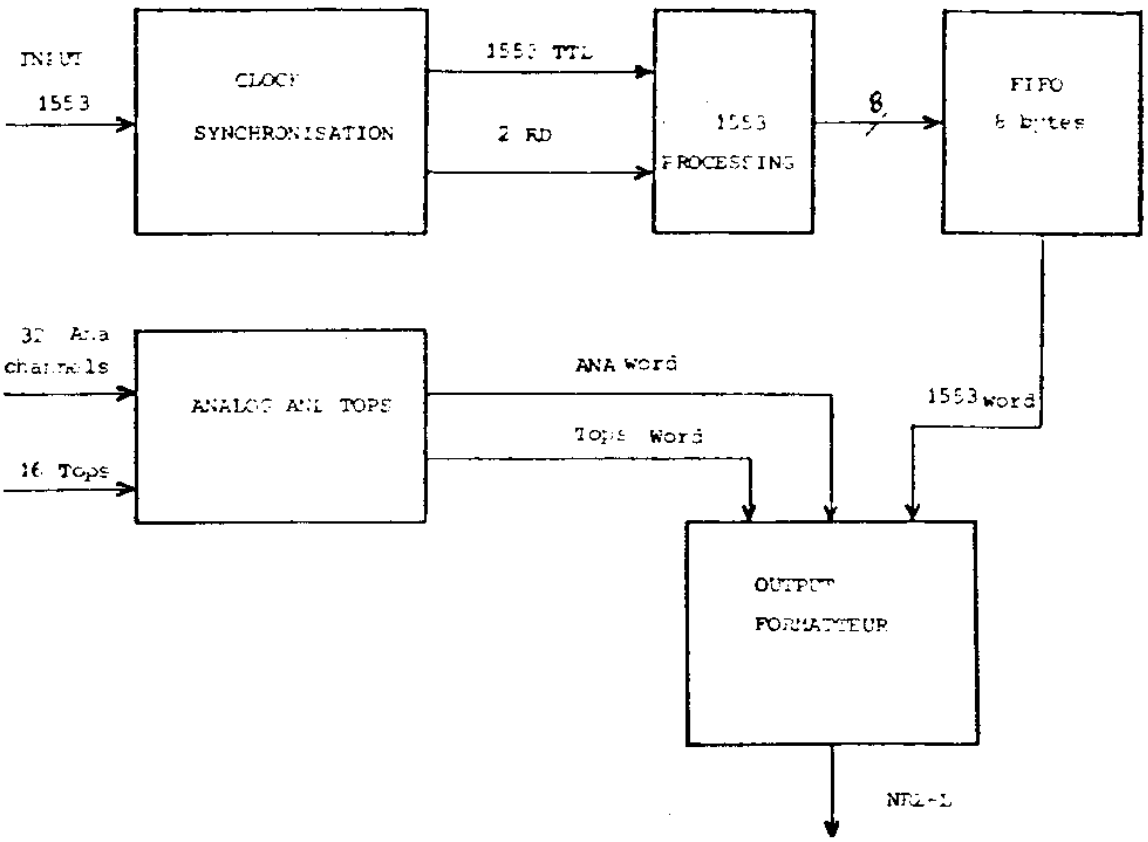
This threshold is programmable by strap.

- minimum threshold: 512 bytes
- maximum threshold: 8 Kbytes
- programming by steps of 512 bytes.

3.3 Blank Words

- In case of low activity of the 1553 bus blank words are inserted. They appear when the memory is empty.

They have the following format:



4. THE 1553 B CONTROLLER

4.1 General Principles

- clock synchronization

  THis function delivers a 2 RD synchronous clock of the 1553 TTL message as of its first bit, thus providing for analysis of the message half.bit by half-bit.

- 1553 management

  Organized around a number of PROM circuits , it analyses the message, prepares the statuses, provides the formatting in bytes and the dating.

- 8 Kbytes FIFO

  This queues the 1553 bytes during high activity phases on the bus. The bytes exit from this function in serial form on request from the formatter.

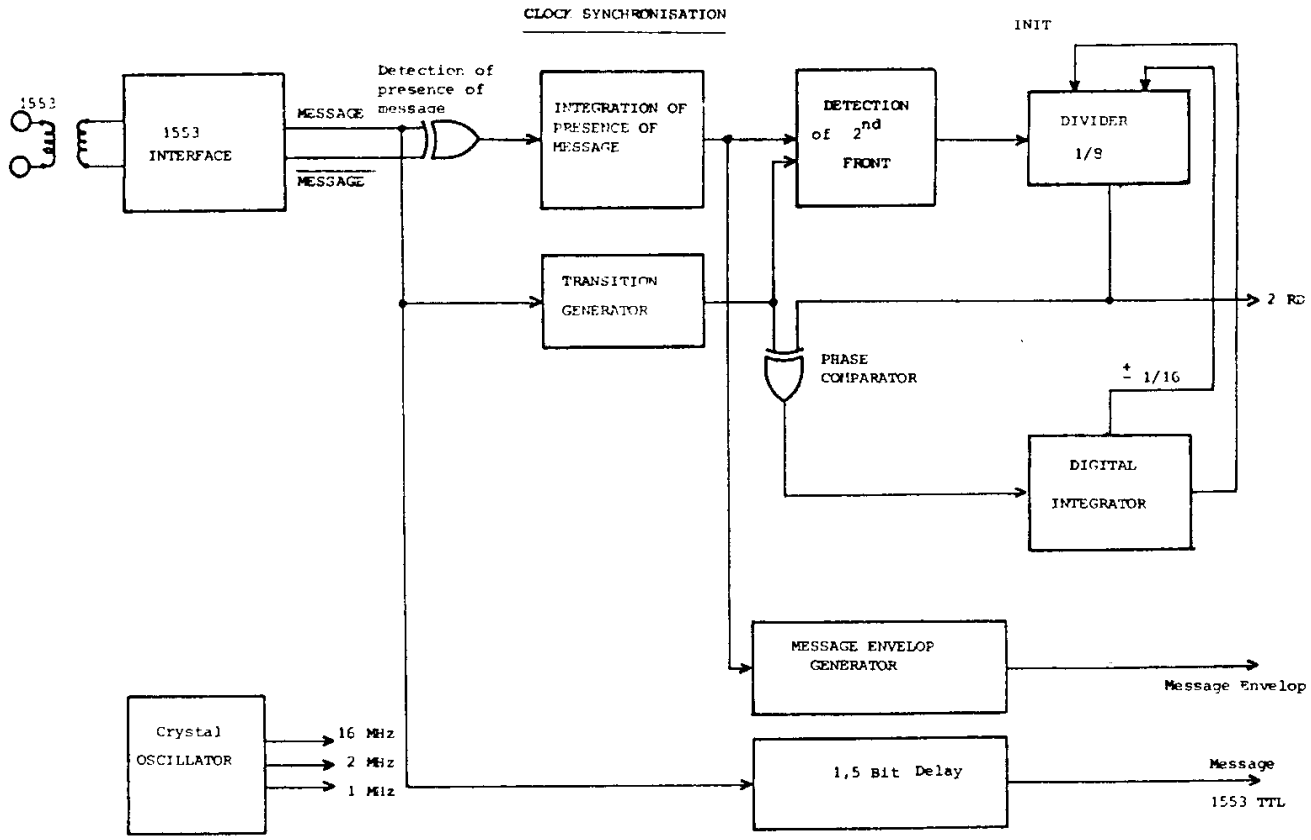
On input the 1553 B controller respects the technical and electrical specifications of the MIL 1553 B standard.

The frequency correction range is $\pm 5.10^{-3}$.

A 1553 message is transmitted from a length of 3.5 bits.

4.2 Principle of Clock Synchronization

- Clock synchronization block diagram



Ordinary standard circuits are not suitable, they reject the error words which is contrary to the “spy role” of the 1553 controller.

The principle adopted is the creation of the rate at 2 MHz, called 2 RD, from a controlled divider operating at 16 MHz.

This divider is initialized by the detection of the second edge of the message (synchronous edge of the remainder of the message).

The input interface delivers the through message data and complemented message, the complementary of the signals indicates the presence of a message.

This data is integrated numerically on five samples.

A generator delivers the message transitions.

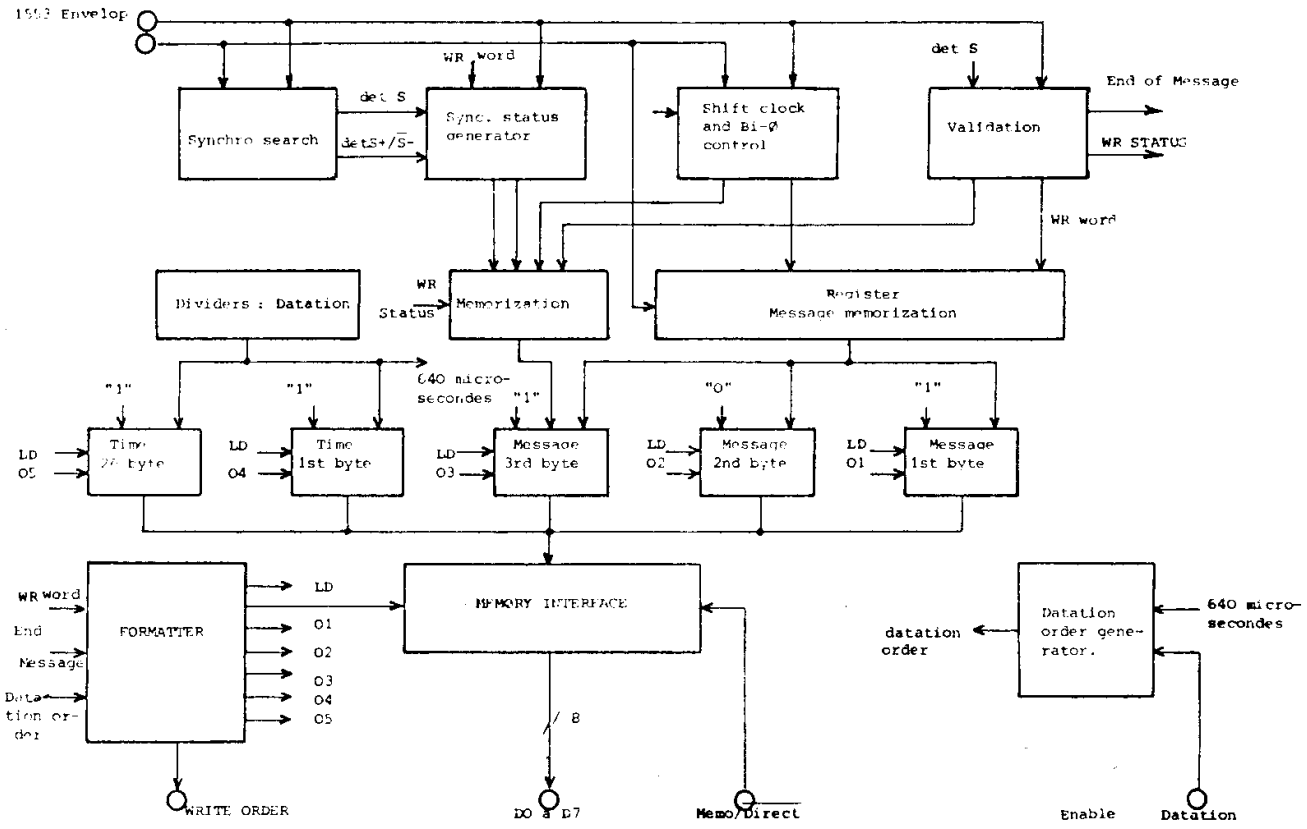
A phase locked loop consistinf of the phase comparator, digital integrator and divider, released from the presence of the message is initialized by the second edge of the message.

The integrator evolves between two thresholds. On arriving on one of the two thresholds the integrator operates on the divider adding or subtracting 1/16 to/from the 2 RD signal.

The 2 RD clock being phased in with the message from the second edge (central edge of the sync located 1.5 bit after its start), the message and message presence are delayed digitally by 1.5 bit.

This function has been hybridated except for the 1553 interface and quartz crystal driver.

4.3 Princple of the 1553 Management



Organized around 5 PROM circuits it produces status, retrieval of the message, or formatting in bytes, dating.

- synchronization research

  This research is permanent and important because it marks the start of a word and conditions its retrieval.

- preparation of the sync status

- preparation of the shift clock and biphase test

The serialization and BØ/NRZ conversion of the message are obtained in a serial/parallel register of 17 bits driven by the third sequencer.

- retrieval management

  At the end of the word the message is memorized in the 17 bit register on “Write Order”.

- formatting

  The previous data, 17 message bits, 4 status bits and the 4 dating bits are memorized in 5x8 bit registers on the order delivered by the sequencer.

  After common memorization of the five bytes this sequencer sends the bytes via the memory interface to the 8 Kbyte FIFO:

  - 3 message bytes only, or

  - 3 message bytes plus 2 dating bytes.

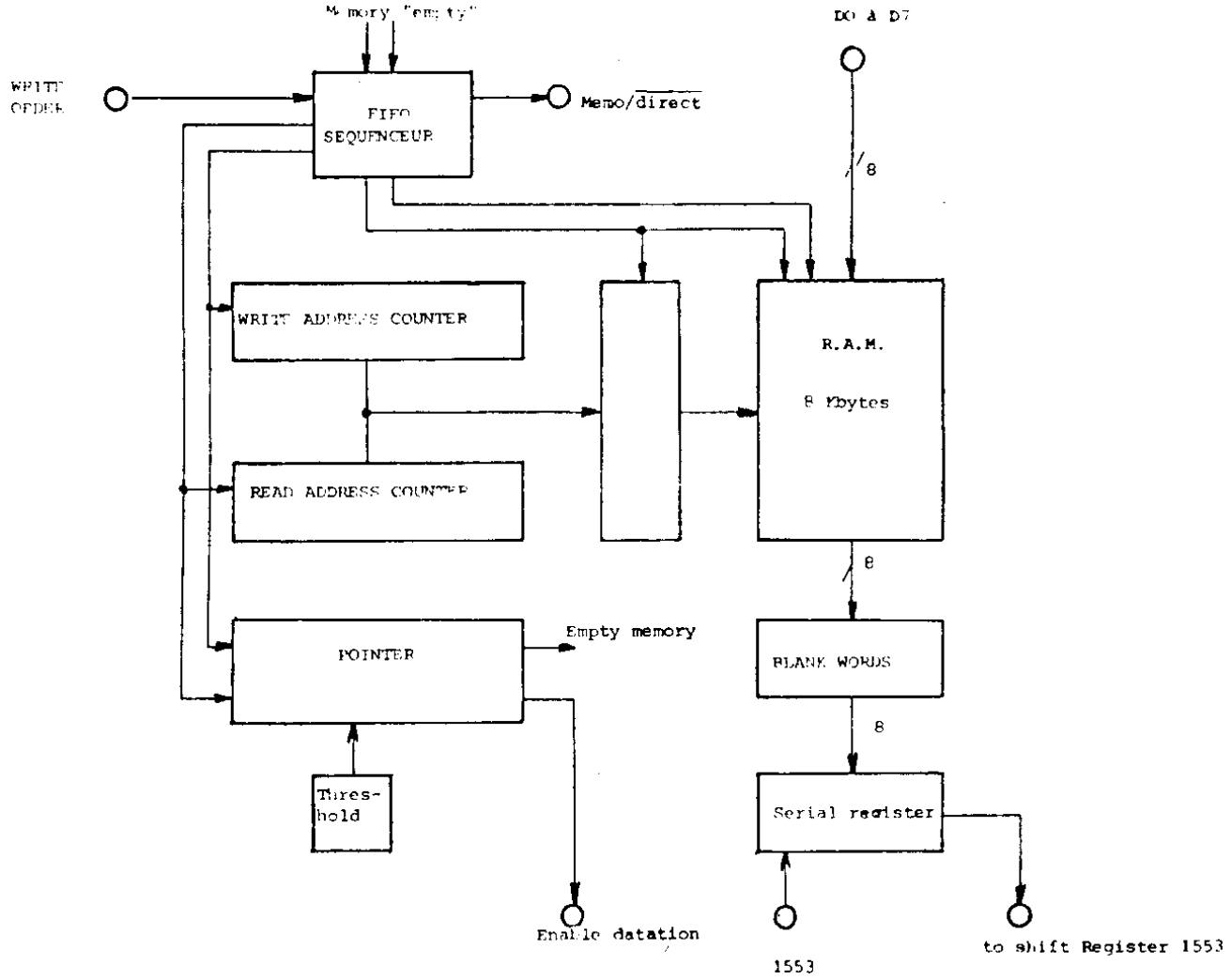
  The decision to send the dating is taken depending on the “end of message” signal and dating requests.

  Dating is halted if the FIFO memory is full.

4.4. Principle of the 8 bytes F1FO

The rate of exchanges on the 1553 bus being fully asynchronous in relation to the speed of 1553 telemetering data, the purpose of this function is to memorize the 1553 data until they are transmitted in the serial telemetering message.

This function organized in FIFO is obtained from an 8 Kbyte memory.



The addresses are supplied by the multiplexing of the states of two counters, one responsible for write addresses and the other for read.

The bytes read are memorized in a buffer register before being directed to the serialization register.

This three status output buffer register provides for the insertion of “blank” words when the memory is empty.

This data is delivered by a up / down counter which permanently monitors the status of the FIFO.

By comparing its status with a filling threshold a comparator provides the dating inhibition data.

All the command signals are prepared by the FIFO sequencer.

5. THE PCM/1553 RELOCATOR

Its task commences by the acknowledgement of the 1553 bytes telemetered within the PCM format. The relocator must then identify the 1553 words together with the dating by analyzing the profile of the bytes flags.

Depending on the contents of the bytes it determines the type of word acknowledged inside the message.

The PCM 1553 relocator sends the message on the 1553 bus respecting the response times together with the intervals between messages. It adds 18 most significant bits to the dating words and thus prepares messages containing dating on 32 bits.

It indicates certain errors discovered on board, or else in the transmission, by sending 1553 words commencing by an erroneous sync.

5.1 General Principle

The PCM/1553 relocator consist of three main functions :

- format synchronizer interface

This interface identifies the data concerning the 1553 bus in the telemetering format.

The 1553 data are identified by a nonvolatile memory addressed by a word counter.

So as to be compatible with different format synchronizers, the phases of the bit, word and long cycle rates can be programmed.

The user has 8 formats at his disposal with a length of 1024 words programmable in R/O memory, he can also program the type of parity.

This function is interfaced with the microcontroller to which it indicates the arrival of each 1553 byte.

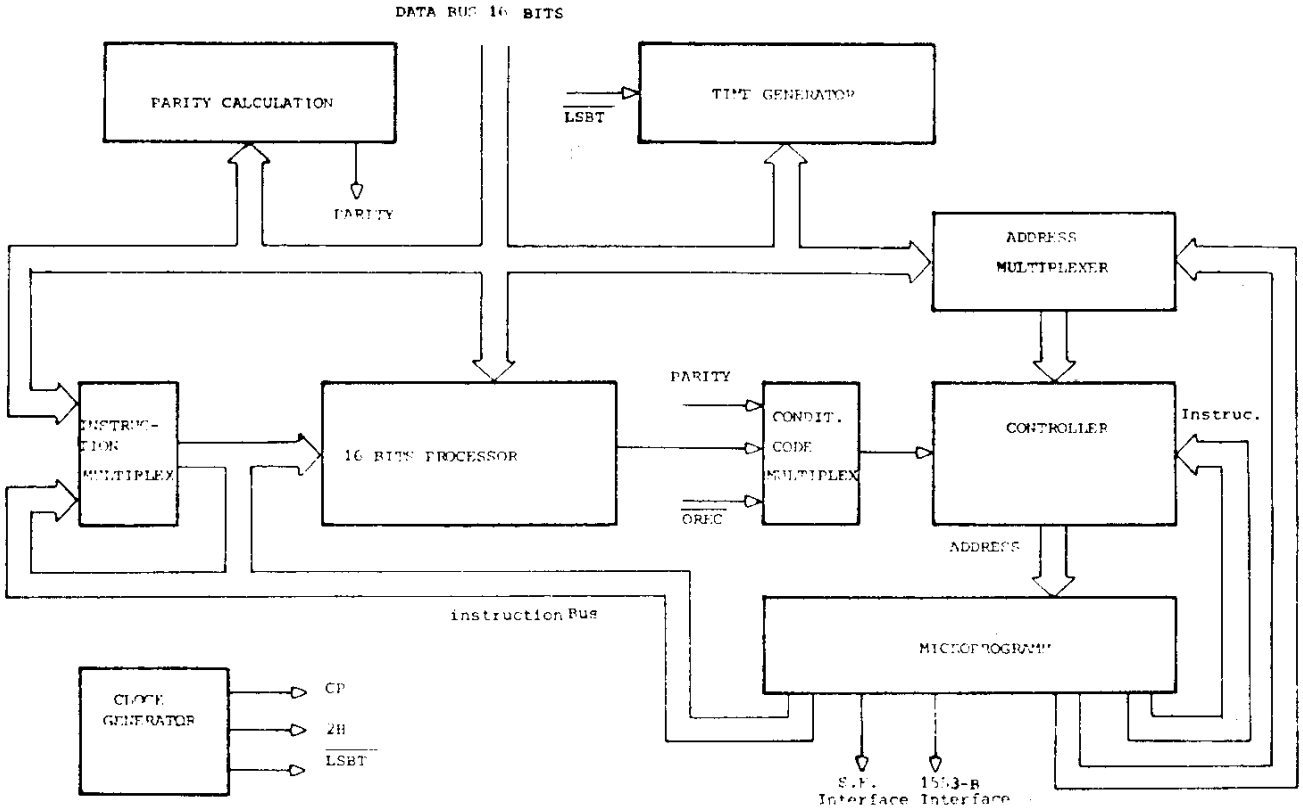
- the microcontroller

This is the heart of the system, it memorizes bytes only concerning the 1553 bus, identifies the 1553 words and dating by analysing the profile of the byte flags received.

- the 1553 interface

It uses the data delivered by the microcontroller to compose the 1553 messages, observing the intervals decided by the microcontroller.

5.2 The Microcontroller



The acknowledgement strategy is based on the detection of the 101 header profile of a sequence of five consecutive flags for a 1553 word and the 101 11 profile for the word following by dating.

The determination of the intervals to be reconstituted is made by analysing two consecutive words.

Each new word entered is used to determine the interval to be inserted behind the preceding word which has been temporarily queued.

Processing of the dating received is also done by the microcontroller.

The dating transmitted by the telemetering is in binary form and contains 14 bits. The dating message to be sent contains time data on 32 bits prepared from the telemetered dating.

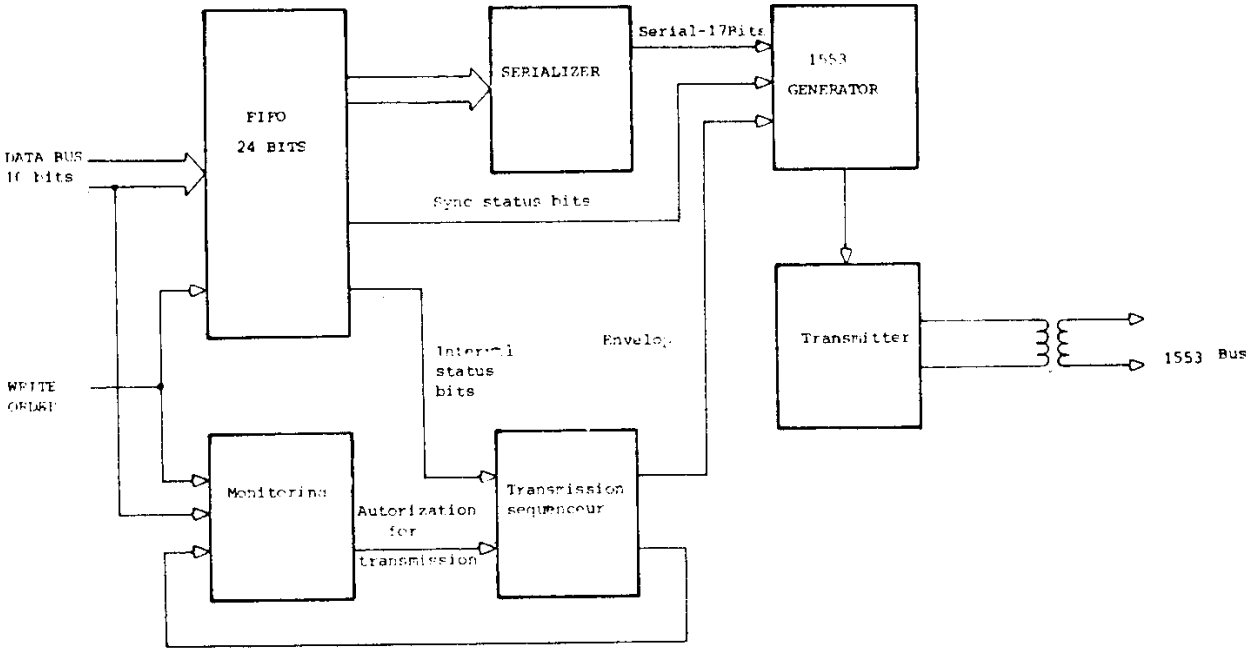
The principle adopted is to create a local dating on a 32 bit field and synchronize it with the least significant bits received.

The dating message prepared (four 1553 words: a command, a status word and two data words) is sent after the 1553 message dated by the 1553 controller.

The words thus processed and identified are sent to the 1553 interface.

This is obtained by the use of a 16 bit high speed processor driven by a microprogrammed sequencer.

5.3 The 1553 Interface



The duration of a 1553 word transmitted by telemetering is equal to 24 microseconds (3 bytes of 8 microseconds) minimum, in the case of a P.C.M. without parity.

The transmission time for the same word by the interface is 20 microseconds (20 bits x 1 microsecond).

Thus the 1553 interface contains on input an FIFO memory in which the 1553 words processed by the microcontroller are written. On output t transmission only commences when the FIFO contains a complete message.

This FIFO also absorbs the increase in speeds on input provided by the creation of the dating messages.

The response times recreated have a fixed duration of 4 microseconds.

The spaces between messages have a minimum duration of 4 microseconds also, in return their maximum duration varies according to the traffic of the missile bus.