

DIGITAL RECEIVER PROCESSING TECHNIQUES FOR SPACE VEHICLE DOWNLINK SIGNALS

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ABSTRACT

Digital processing techniques and related algorithms for receiving and processing space vehicle downlink signals are discussed. The combination of low minimum signal to noise density (C/N_0), large signal dynamic range, unknown time of arrival, and high space vehicle dynamics that is characteristic of some of these downlink signals results in a difficult acquisition problem. A method for rapid acquisition is described which employs a Fast Fourier Transform (FFT). Also discussed are digital techniques for precise measurement of space vehicle range and range rate using a digitally synthesized number controlled oscillator (NCO).

Keywords: Digital receiver processing techniques, Fast Fourier Transform, numerically controlled oscillator, space vehicle downlink signal acquisition, range and range rate measurement.

INTRODUCTION

This paper describes digital processing techniques for the acquisition and tracking of a space vehicle downlink signal with a residual carrier component. Range and range rate measurement techniques are also discussed. The dynamics of some space vehicle orbits result in a received downlink signal with high doppler and doppler rate and a large dynamic range in signal strength.

Accurate range and range rate measurements are made by phase tracking the received downlink ranging code and the residual carrier signals, respectively. Before the downlink signal can be phase-tracked a frequency acquisition is required to reduce the signal frequency uncertainty. High doppler rates require this frequency acquisition to be performed rapidly.

A typical procedure for initial signal frequency acquisition is to step a filter over the range of frequency uncertainty and measure power in the filter. Signal presence is declared when the power exceeds a threshold. Due to a large uncertainty in signal power, detection of a weak signal in the center of the filter can not be distinguished from a strong signal on the filter skirt. Hence, an additional frequency search after signal detection is required to center the filter on the signal in the case of a strong signal.

During the time required to perform these measurements the signal frequency can change significantly due to high doppler rate. The result is a poor estimate of signal frequency.

These difficulties result in the need for a complex algorithm to perform signal acquisition. A microprocessor-controlled receiver allows these algorithms to be performed. This implementation also permits a simple and accurate method to measure space vehicle range and range rate.

The digital processing techniques described in this paper are employed in a receiver for the Space-Ground Link Subsystem (SGLS). The SGLS provides the capability to perform space vehicle range and range rate measurements, as well as telemetry reception and commanding. A ranging code phase modulates the SGLS carrier. The phase modulation index is either 0.125 or 0.3 radians; therefore, a residual carrier component is present. The parameters for signal acquisition are given in Table I. The receiver performs initial signal acquisition using the FFT approach described below. During tracking range and range rate are measured.

TABLE I - SIGNAL ACQUISITION PARAMETERS

	Mode	
	I	II
Minimum Signal-to-Noise Density (dB-Hz)	29.7	38.0
Signal Power Uncertainty (dB)	50.0	50.0
Frequency Uncertainty (kHz)	±200	±200
Maximum Doppler Rate (Hz/sec)	±800	±3000
Maximum Search Time (sec)	11.5	0.575
Minimum Detection Probability	0.99	0.99

HARDWARE IMPLEMENTATION

The receiver hardware configuration is shown in Figure 1. The input radio frequency (RF) signal is downconverted to an intermediate frequency (IF). The signal is then downconverted to baseband and digitized by an analog-to-digital converter (ADC). A Fast

Fourier Transform (FFT), computed by a special purpose processor chip (Texas Instruments TMS 32010), is employed to perform the initial carrier signal acquisition. Samples for the FFT are taken at a 25.6 kHz rate. Carrier frequency and phase tracking are performed with a cross-product automatic frequency control (CPAFC) loop⁽¹⁾ and a phase lock loop (PLL), respectively, implemented in the single board computer (SBC). The sampling rate is reduced to 2 kHz in this mode and the presample filter bandwidth is reduced to 800 Hz.

Carrier frequency and phase control are accomplished via the numerically controlled oscillator (NCO) in conjunction with a single sideband modulator (SSM). This provides frequency shifts about the SSM reference frequency. The NCO generates discrete samples of a cosine and sine wave.⁽²⁾ Digital-to-analog conversion and lowpass filtering results in analog cosine and sine wave outputs. Hence, the NCO functions analogously to a voltage controlled oscillator (VCO), with frequency being controlled by a digital number rather than a control voltage. The advantage of using the NCO is that it supplies a stable, accurate frequency. The NCO is available as a single integrated circuit chip (Stanford Telecommunications, Inc. ST-1172). Range rate is computed by the single board computer using the carrier NCO updates.

An automatic gain control (AGC) is performed to maintain the signal level at a nominal operating point. The AGC loop filter is implemented in the single board computer. Discrete gain corrections are output to the digitally controlled attenuator.

A local ranging code is correlated with the downlink ranging code. The ranging code has a residual clock component. The single board computer implements the code clock PLL and the initial code acquisition process. Code clock phase tracking is performed via the code NCO. Range is computed by the single board computer using the code NCO updates.

ACQUISITION AND TRACKING ALGORITHMS

The sequence of events that leads to signal acquisition and tracking is shown in Figure 2.

Signal Detection

The first function is a spatial and frequency search in order to detect the satellite signal. The frequency search is performed over the maximum frequency uncertainty. The NCO is stepped across the search window in increments of f_s , where f_s is the input sample rate of the in-phase (I) and quadrature (Q) samples. After each step the receiver performs an N-point complex FFT ($N=64$), using the I and Q samples as the real and imaginary inputs, respectively. The FFT can be viewed as a convenient implementation of a bank of N filters⁽³⁾. Each filter response is determined by the data windowing function⁽⁴⁾. If power

in any of the FFT cells exceeds the signal detection threshold, then signal presence is declared.

After signal detection receiver gain linearization is performed because a signal which is much stronger than expected may saturate the receiver. Receiver saturation is detected by observing the FFT output. If, upon signal detection, the power in the signal detection cell is within 3 dB of saturation, the receiver gain is reduced by commanding the step attenuator.

The signal may be detected even though it is outside the receiver's input bandwidth (i.e., on the filter skirts), due to aliasing by the FFT algorithm. An alias check is performed using the FFT to search for peak power in a frequency range about the frequency where the signal was originally detected. If the initial signal detection was on an aliased component, then an additional gain linearization is performed. This is required since the signal may saturate the receiver as the signal is centered in the receiver's input bandwidth during the alias check. At the completion of the alias check, the receiver frequency is centered on the signal.

Cross Product Automatic Frequency Control (CPAFC) Loop

The accuracy of the carrier signal frequency estimate at the completion of the signal detection process is limited by the resolution of the of the FFT. The CPAFC loop is employed to derive a better estimate of signal frequency and to estimate doppler rate. These estimates are used to initialize the PLL for rapid acquisition. A functional block diagram of the digital CPAFC loop implementation is shown in Figure 3.

The implementation and performance of the CPAFC loop has been described by Natali⁽¹⁾. Using these results, the normalized discriminator characteristic for a sinusoidal input is:

$$D(\Delta\omega) = |H(j\omega)|^2 \sin\omega\Delta T \quad (1)$$

where:

$$|H(j\omega)| = \text{the amplitude response of the I and Q lowpass filters} \quad (2)$$

$$\Delta\omega = \text{frequency error (rad/s)} \quad (3)$$

$$T = \text{cross product delay time} \quad (4)$$

The discriminator provides an error signal to the loop filter that is approximately linear with frequency error for $\omega\Delta T < 1$.

Carrier Phase-Locked Loop (PLL)

The receiver automatically transitions from the second order CPAFC to third PLL operation at the end of the CPAFC loop settling period. The PLL configuration is as shown in Figure 3.

The transition from AFC to PLL operation is accomplished by switching the input to the loop filter and adding a constant gain path for phase error input to the NCO (the values of the gain constants are also changed to the appropriate values). This is an extremely convenient configuration as the loop filter contains the doppler and doppler rate estimates for the AFC to PLL handover. For example, suppose that the input signal exhibits a constant doppler rate. The second-order AFC loop tracks this signal with zero error* (in the absence of noise) and from Figure 3:

$$V_1(kT)=V_2(kT)=V_6(kT)=0 \quad (5)$$

$$V_3(kT)=V_4(kT)=\dot{f} \quad (6)$$

$$V_5(kT)=V_7(kT)=f(o)+(kT) \dot{f} \quad (7)$$

where:

$$kT=\text{the } k\text{-th loop update time} \quad (8)$$

$$f(o)=\text{doppler at the initial loop update} \quad (9)$$

$$\dot{f} = \text{doppler rate} \quad (10)$$

$$V_j(kT)=\text{the value of the corresponding reference points at time } kT \text{ in Figure 3 for } j=1, \dots, 7 \quad (11)$$

Similarly, the third order PLL tracks the same signal with zero error and the steady state conditions are the same as those given in equations (5) - (7). Therefore, the loop filter integrators contain the loop estimates of f and \dot{f} at the time of handover from AFC to PLL.

* This is strictly true only for a continuous analog loop. The digital loop will exhibit small errors due to quantization and sampling effects.

Range Rate Measurement

The digital PLL loop implementation allows a simple method for measuring range rate. The carrier PLL tracks the carrier doppler. The digital number input to the NCO is equal to the carrier doppler times a known scale factor. Space vehicle range rate can be derived from carrier doppler. Hence, by averaging NCO updates a smoothed estimate of range rate is obtained.

Range Measurement

The measurement of space vehicle range described is for the SGLS range code. The example ranging code and acquisition procedure described by Golomb⁽⁵⁾ is identical to the SGLS range code and the code acquisition procedure. Briefly, the SGLS ranging code consists of four code components and a clock component. A PLL tracks the residual code clock (Figure 4). Code clock acquisition is performed after carrier tracking has been achieved. The carrier PLL aids the code PLL with a scaled value of carrier doppler. An initial range measurement is provided by acquiring the code components.

Similar to the carrier code NCO inputs are proportional to the doppler on the code clock component. The accumulation of code NCO inputs is equal to the change in satellite range. The satellite range is output at discrete time intervals. The range at the k-th measurement interval is:

$$R(k)=R_o+\Delta R(k) \quad (12)$$

where:

$$R(k)=\text{satellite range at the k-th measurement interval} \quad (13)$$

$$R_o=\text{initial range measurement computed from code acquisition process} \quad (14)$$

$$\Delta R(k)=\text{range increment from } R_o \text{ at the k-th measurement interval} \quad (15)$$

Although the range measurement process described is for the SGLS range code this technique is applicable to other ranging codes. Once an initial range has been established additional changes are measured by accumulating NCO inputs.

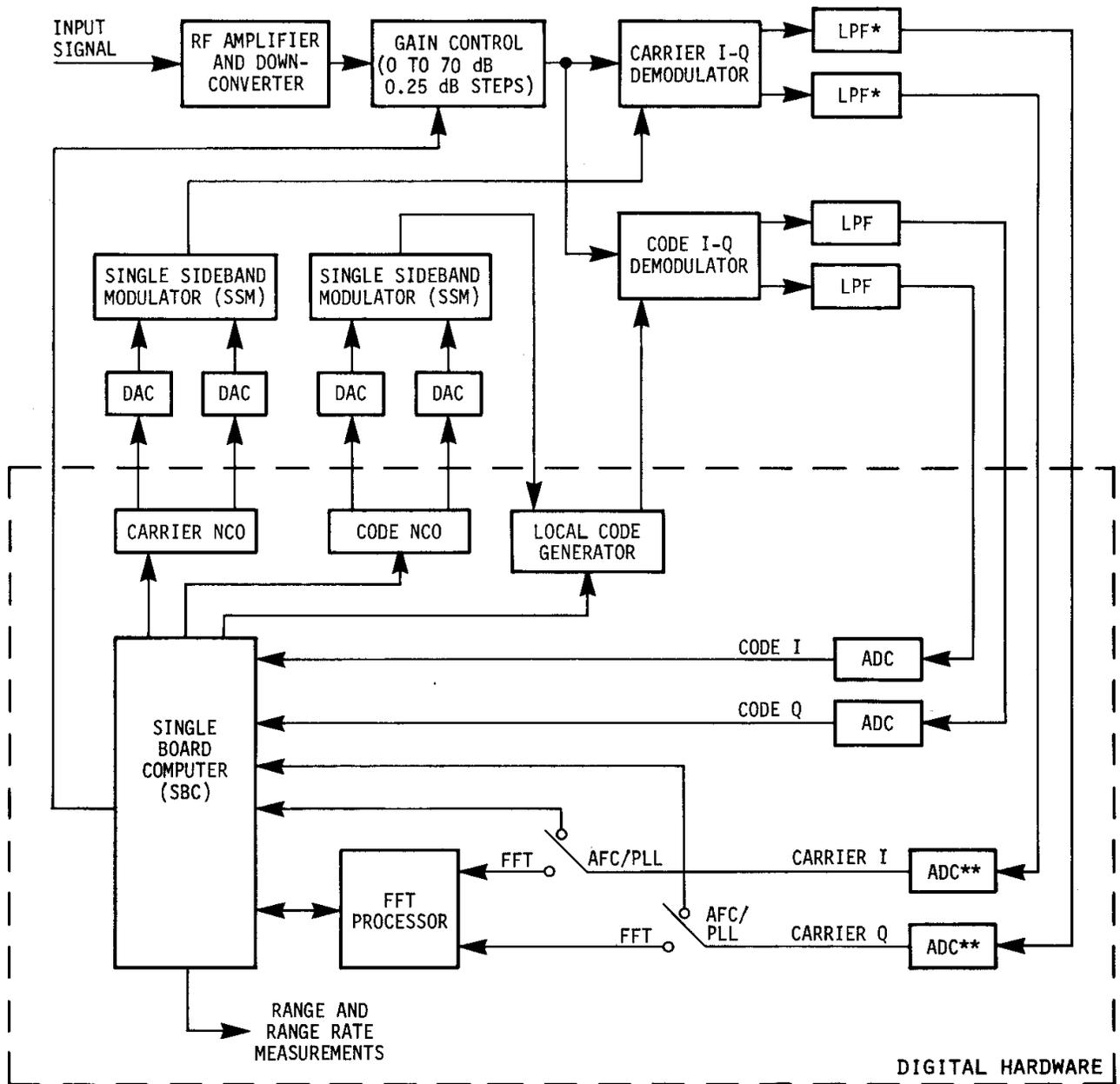
CONCLUSION

The microprocessor-controlled receiver implementation and use of a special purpose FFT processor chip allows a feasible, real-time solution to a difficult space vehicle signal acquisition problem. The digital receiver implementation also permits accurate

measurement of space vehicle range and range rate. The key element in the range and range rate measurement circuitry is the digitally synthesized number controlled oscillator (NCO) which is available as a single integrated circuit chip.

REFERENCES

- (1) Natali, Francis D., "AFC Tracking Algorithms," IEEE Transactions on Communications, Vol. COM-32, No. 8, August 1984, pp. 935-947.
- (2) Tierney, Joseph, Rader, Charles M., and Gold, Bernard, "A Digital Frequency Synthesizer," IEEE Transactions on Audio Electroacoust., Vol. Au-19, March 1971, pp. 48-56.
- (3) Bergland, G.D., "A Guided Tour of the Fast Fourier Transform," IEEE Spectrum, Vol. 6., July 1969, pp. 41-52.
- (4) Harris, Fredric J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Proceedings of the IEEE, Vol. 66, No. 1, January 1978, pp. 51-84.
- (5) Golomb, Solomon W., "Applications to Ranging," DIGITAL COMMUNICATIONS WITH SPACE APPLICATIONS, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1964, pp. 85-105.



* 6-POLE BUTTERWORTH, $B(3\text{ dB}) = 10.6\text{ KHz}$ FOR FFT FUNCTION.
 2-POLE BUTTERWORTH, $B(3B) = 800\text{ Hz}$ FOR AFC/PLL FUNCTION.

** $R_s = 25.6\text{ KHz}$ FOR FFT FUNCTION
 $R_s = 2\text{ KHz}$ FOR AFC/PLL FUNCTION

FIGURE 1 RECEIVER HARDWARE IMPLEMENTATION

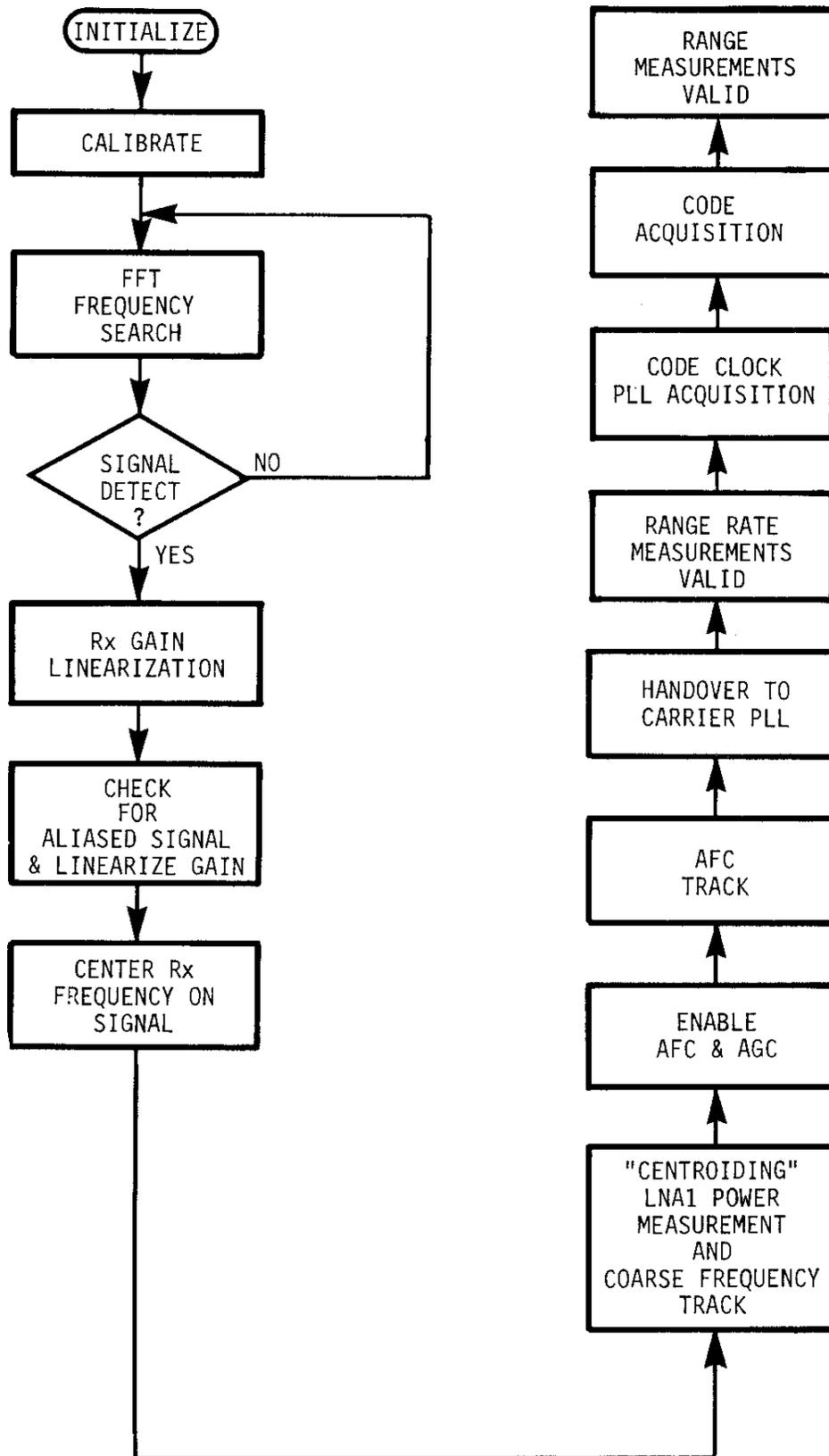


FIGURE 2 SIMPLIFIED FLOW CHART OF RECEIVER OPERATION

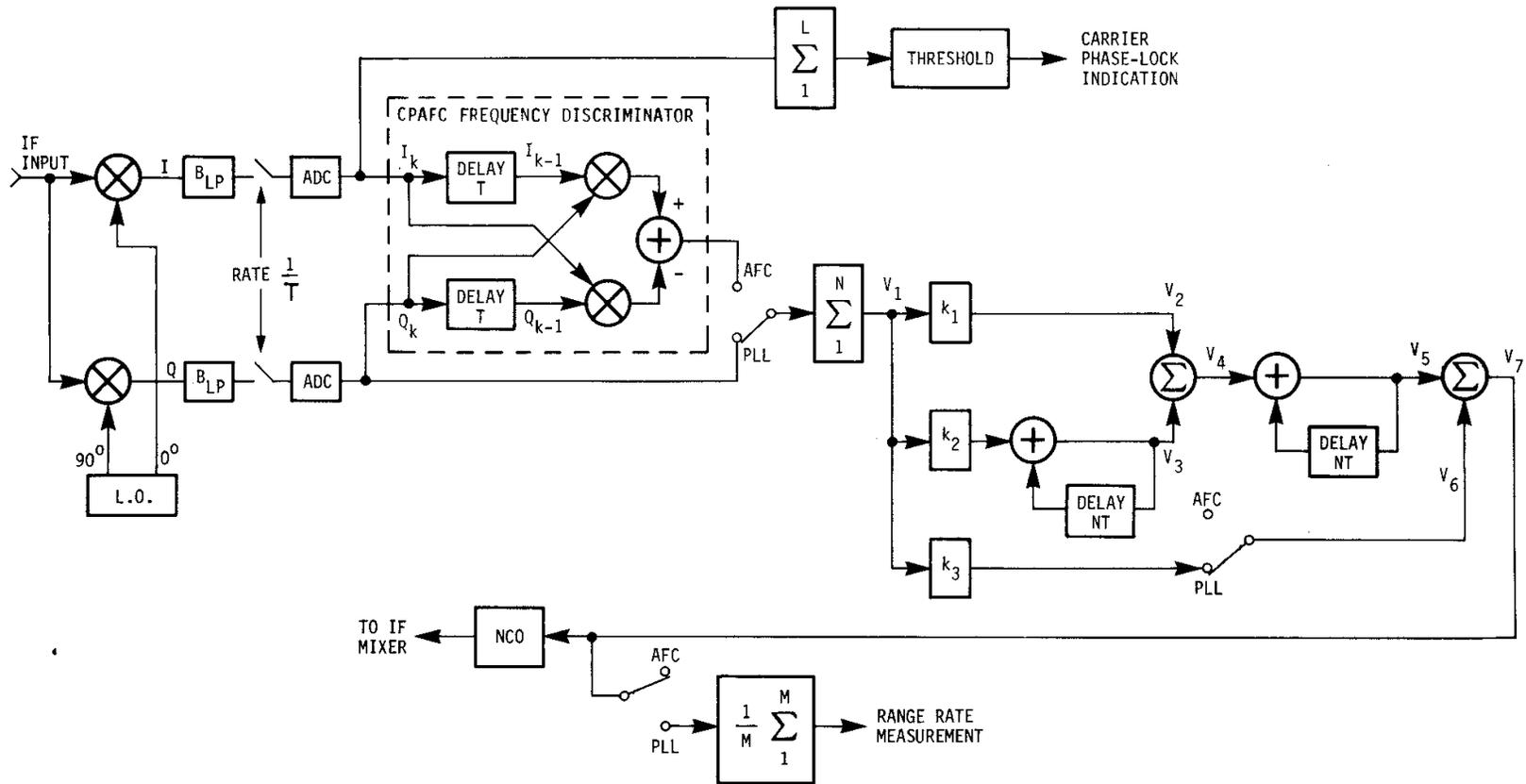


FIGURE 3 CARRIER SECOND ORDER CPAFC/THIRD ORDER PLL CONFIGURATION

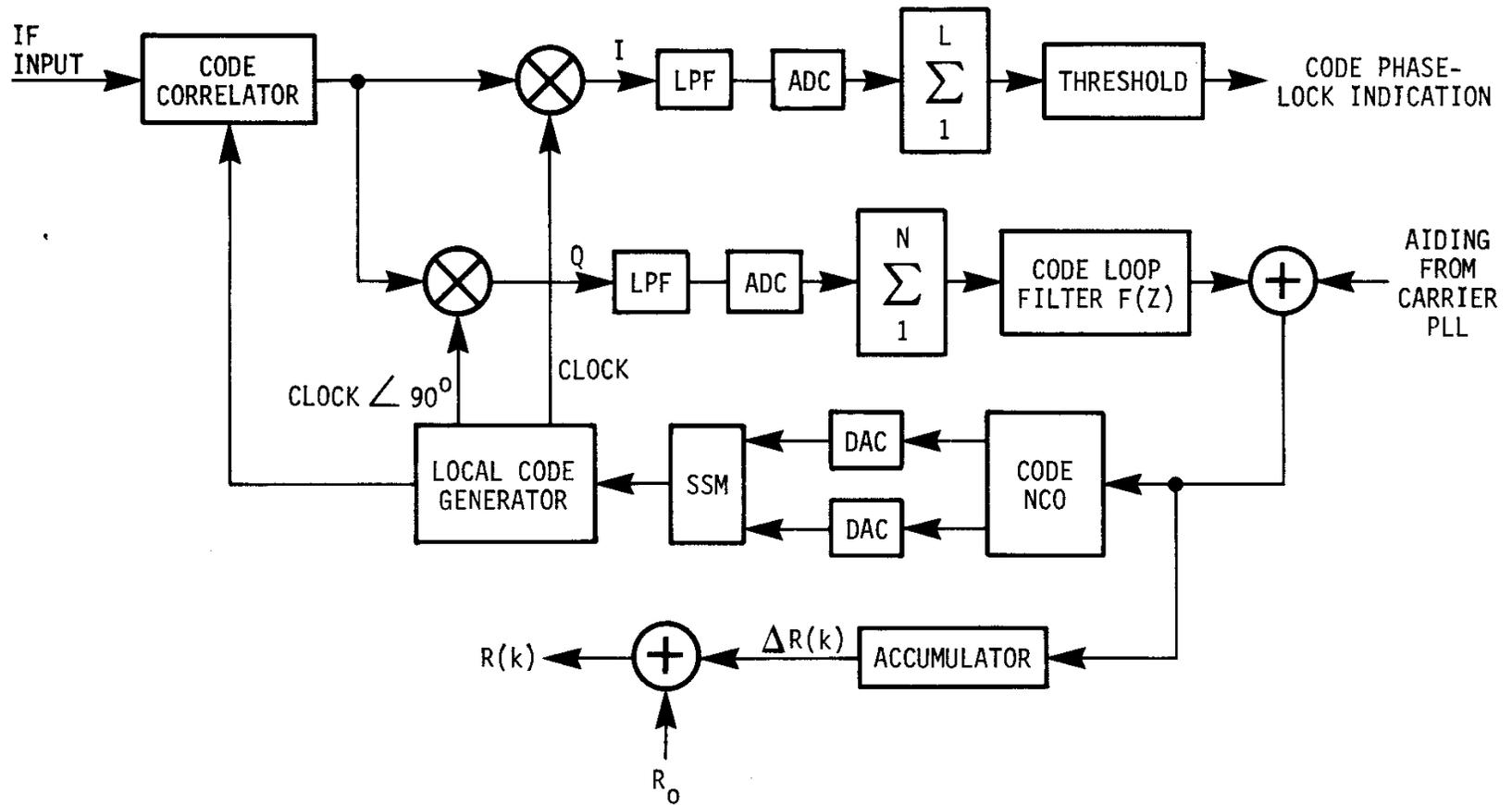


FIGURE 4 CODE PLL CONFIGURATION