ABSTRACT

In early 1981, the Physical Science Laboratory (PSL) was tasked by the Air Force Geophysics Laboratory (AFGL) to develop a portable Pulse-Code Modulation (PCM) telemetry station that would acquire and support the higher PCM data rates from Aries-type rocket payloads. The station would have to provide real-time and near real-time calibration, prelaunch and launch test support to AFGL researchers involved in space vehicle probe analysis. The station would also have to utilize a flexible software system, transportable hardware, and be easily expanded to meet the continually growing and varied needs of the researchers.

INTRODUCTION

Prior to the advent of PCM telemetry and even during the early days of PCM, the volume and complexity of telemetry data required very little in the way of display capability. A few strip chart traces provided all the information necessary to determine the operational integrity of the payload. However, the complexity of the newer payloads has become such that a computer is needed to determine the integrity of the experiments.

A survey was done by PSL to determine if any hardware existed that would meet the needs of AFGL. Hardware was found that would meet the needs, however, it was not portable. Likewise, the portable hardware found would not meet the required software and expansion needs. It was decided to modify an existing PSL system design. This system had a PSL built decommutator (DECOM) that was external to the computer and was connected to the computer via a PSL built direct memory access (DMA) interface. This system met the AFGL needs and with some redesign could be made portable. The decom was redesigned and combined with the DMA interface on one board that fits on the Digital Equipment Corporation (DEC) PDP-11 computer bus (UNIBUS). This redesign saved both weight and rack space. The new DECOM/DMA interface is the heart of the portable PCM telemetry station designed and built for AFGL.
SYSTEM DESCRIPTION

A. System Equipment

1. Computer - DEC model PDP-11/34A with the following options:
   A. 256 Kbytes of memory
   B. FP11-A floating point processor
   C. KK11-A cache memory
2. Disk system - A DEC RL211 controller with two (2) each DEC model RL02 disk drives (10.4 Mbytes removable disk cartridge each).
3. Console terminal - DEC model VT125 CRT terminal. The VT125 is a graphics terminal with DEC ReGIS protocol.
4. Auxiliary terminals - Two (2) DEC model VT100 CRT terminals. These provide additional non-graphic displays for the system.
5. Asynchronous interface - DEC DZ11 8-line asynchronous multiplexer. The DZ11 provides a RS-232 interface for the auxiliary terminals and the modem.
6. Digital Tape System - Two (2) each Kennedy model 9300 tape drives and Emulex model TCII tape controller. Each tape drive is 800/1600 BPI at 125 IPS.
7. Line printer - Printronix P300 and interface. The P300 is a dot matrix printer/plotter. Capability is 300 lines per minute in the print mode and 16.7 inches per minute in the plot mode.
8. Time Code Reader/Translator - Datum model 9310.
10. Parallel Interface - MDB model DR11-C. Programs the bit sync.
11. DECOM/DMA Interface - PSL model HS11-A.
12. PCM Simulator - PSL model 82.

B. PCM DECOM/DMA Interface (PSL Model HS11-A)

General:

The HSII-A PCM DECOM/DMA interface was developed by PSL for use on a DEC PDP11 computer. The interface is built on a hex height, extended length, double width wire wrap module board. The interface fits in a small peripheral slot (SPC) in the PDP11 UNIBUS. All power is supplied by the computer system. The interface consists of two (2) sections: a decommutator (DECOM) section and a direct memory access (DMA) section.

The UNIBUS communicates with the HS11-A interface via sixteen (16) device registers. Eight (8) device registers are used in the DECOM section and eight (8) device registers are used in the DMA section.
Decom Section:

The decommutator (DECOM) section of the interface converts the incoming serial PCM data to parallel data for use by the DMA section. The DECOM section takes the NRZ-L serial data and the 0 degree and 90 degree clocks from the bit synchronizer and converts them to 16 bit parallel data and various synchronous timing pulses. For purposes of this discussion, a frame is defined as a minor frame and a subframe as a major frame.

The synchronization (sync) of the PCM data in the interface is handled by two (2) digital correlators: one for the frame sync and the other for the subframe sync. Each digital correlator has three (3) serial 64 bit registers. The reference register is used to store the sync pattern. The PCM data are shifted through the data register and its parallel output is compared (exclusive ORed) with the parallel output of the reference register. The mask register masks or selectively chooses “no compare” bit positions enabling total length flexibility. The compared and masked parallel data go to a 64 bit digital summer. The summer outputs are used in the sync circuit for the detection of sync.

There are three (3) states of sync: Search, Check and Lock. These states pertain to both the frame and subframe syncs. The search state is when no correct sync patterns are being detected. One detected correct sync pattern will cause the DECOM to go into the check state. The DECOM will remain in the check state until seven (7) more correct consecutive sync patterns are detected in the correct word(s) and only then will the DECOM go into the lock state. Conversely, the DECOM will remain in the lock state until an incorrect sync pattern is detected. The DECOM will then go into the check state. Seven (7) incorrect consecutive sync patterns will cause the DECOM to go into the search state. The subframe sync will be forced into the search state whenever the frame sync goes into the search state.

The sync pattern detection circuits can handle various bit compares in the sync patterns. The number of bit compares can be set from zero (no bit compare), to the number of sync bits, a maximum of 64 bits. Three (3) registers are used to set the number of sync compares required: Check and Lock Compare, Search Compare and Subframe Compare. The Check and Lock Compare Register holds the number of compare bits in the frame sync pattern while in the check and lock modes. The Search Compare Register holds the number of compare bits in the frame sync pattern while in the search mode. The Subframe Compare Register holds the number of compare bits in the subframe sync pattern for all three modes: search, check and lock. The usual error scheme for frame sync is N-1 compares (one error) for the search compare and N compares (no errors) for the check and lock compare. The usual error scheme for the subframe sync is N compares (no errors).
The HS11-A interface transfers data in two modes. One mode will transfer data only when the data are valid; i.e., interface is in lock state or check state. The other mode will transfer data in any state: search, check or lock.

**DMA Section:**

The direct memory access (DMA) section takes the parallel data from the DECOM section and makes it available to the computer. The DMA section replaces the last frame sync word with two (2) timing words, 16 bits each, from a time code reader/translator. This is the only modification the DMA section does to the incoming data. Figure 1 shows the structure of the two (2) timing words and a representation of typical data words.

The DMA interface uses two (2) buffer address registers to transfer the data. These buffers will cycle automatically; i.e., one buffer will be “filling” up with data and the other buffer will be available for reading by a software application program. The word count register is used to control the number of words that are to be transferred to the computer, usually a multiple of the subframe if present. If not, it will be a multiple of the frame. The time data from the time code reader/translator can also be read into the computer by two (2) time data registers.

Three (3) I/O (input/output) connectors are used in the HSII-A. One input, from the bit sync, contains the NRZ-L data and the 0 and 90 degree clocks needed for the DECOM section. A second input is from the time code reader/translator. This input contains the timing information needed for the interface. A third input connects to the front panel of the computer. The front panel of the computer has been modified to contain the circuitry for displaying various functions of the DECOM section; search, check, lock, etc. The displays are for monitoring and trouble shooting the DECOM section.

**C. System Specifications and Capabilities**

1. Up to 2.0 megabits/sec.
2. Up to 16 bits/word.
3. Up to 1024 words/frame.
4. Up to 256 frames/subframe.
5. Up to a 64 bit frame sync word.
6. Up to a 64 bit subframe sync word, located anywhere in first 256 words of the frame.
7. Most significant bit (MSB) or least significant bit (LSB) first.
8. Normal frame sync or alternate code complement (ACC).
9. Up to 100 kiloword transfer rate to disk.
10. Up to 35 kiloword transfer rate to digital tape at 1600BPI.
Timing word 0 contains fifteen (15) bits of straight binary time of day in seconds.

Timing word 1 contains the 17th bit of time of day in seconds, frame not locked, subframe not locked and ten (10) bits of straight binary time in milliseconds. Bits 12, 13 and 14 are set to zero.

This is a typical data word structure presented to the UNIBUS for 8 bits per word PCM telemetry data. One (1) telemetry word is one (1) byte to the UNIBUS. DATA WORD 1 is defined as the first data word after the last sync word. DATA WORD 1, in this case, would be the most significant 8 bit byte after TIMING WORD 1.

This is a typical data word structure presented to the UNIBUS for 10 bits per word PCM telemetry data. One (1) telemetry word is ten (10) bits to the UNIBUS. DATA WORD 1 is defined as the first data word after the last sync word. DATA WORD 1, in this case, would be the first data word after TIMING WORD 1. The six (6) most significant bits are set to zero.

“FIGURE 1. TIMING AND DATA WORD STRUCTURE”
12. Additional CRT displays, non graphic, on the two (2) auxiliary VTIOO terminals.
13. High speed printout of text and graphics on the P300 line printer/plotter.
14. A 300/1200 baud modem for transferring of data or programs to other computer systems.

D. Software

Two conflicting philosophies exist pertaining to software systems for this type of application. One school favors the “do all things for all people” approach, the other favors the small scale specialized approach. PSL chose the second approach.

Operating Systems:

The RT-11 operating system was chosen because of its small size, speed, multi-tasking capability and easy access to the I/O page.

Set Up Software:

An interactive program was written and provided to enable the user to program the DECOM/DMA interface and the bit sync. This program will either set up the system from an existing parameter file or prompt the user for all required information. This allows the user to program the system one time for each different telemetry format to be supported and recall the parameters at a later time. Regardless of which path the user takes, all setup parameters are echoed to the CRT terminal for user verification before transmission to the DECOM/DMA interface and bit sync. The DECOM section of the HS11-A and the bit sync are set up independently from the DMA section. This allows the DECOM and bit sync to be active and lock up to the PCM serial data with no DMA transfers.

Application Software:

The application software is written in FORTRAN IV and MACRO-11 (DEC’s assembly language). The initial software system was developed for support of an AFGL sounding rocket payload. This system required the display of sixty two (62) parameters. These parameters were divided into three (3) pages and displayed on two (2) CRT terminals in engineering units and as character string messages.

The system user has the option of displaying any of these three pages on either CRT terminal. This arrangement allows two users to monitor different sets of parameters on a non-interference basis. Screen update rate is approximately once per second. This rate appears to minimize screen flicker while still providing an adequate refresh rate. Since the delivery of the prototype system to AFGL, PSL has used this hardware configuration and
software approach to provide support to several other customers including other sounding rockets and surface to air missiles. Experience has shown that once requirements are defined, a display/data collection software system can be designed, implemented and tested in approximately four (4) man weeks.

E. Portability

The need for portability required shipping containers that would protect the equipment and not hinder the setup. SHOCK-STOP and RACK-PACK cases from Thermodyne International, Ltd. were used on the system. The high density polyethylene SHOCK-STOP cases come with full foam cushioning that is custom cut to fit the equipment. The SHOCK-STOP cases are used in shipping the CRT terminals, line printer, and documentation. The RACK-PACK instrumentation case has an inner 19" rack frame built in. This frame is shock mounted to the ABS plastic outer shell with eight (8) elastometric shock mounts. Both the front and back covers remove quickly exposing the equipment for easy access. The RACK-PACK cases also come with four (4) removable casters on each case. The computer, disks, time code reader/ translator, PCM simulator, bit sync and digital tape drives are housed in these RACK-PACK instrumentation cases. These Thermodyne cases can be air shipped, if necessary. The system can be setup, checked out and ready to operate in less than two (2) hours.

SUMMARY/CONCLUSION

AFGL tasked PSL to develop a portable PCM telemetry station. The station was designed and built based on a DEC PDP-11/34A computer and a PSL built DECOM/DMA interface. Various peripherals are included with the station to enhance its capabilities. The PCM station was designed for Aries type sounding rockets, however, the station can process any PCM source that operates within the system specifications. The system has been successfully used on a recent AFGL Sounding Rocket Mission.

Planned system developments include: 1) interface of an Astro-Graph model 850 graphic recorder, adding strip chart capability; 2) programmable PCM bit synchronizer, with a bit rate up to 2 Mbits/sec; and 3) interface of the HS11-A DECOM/DMA to other computer systems.