PHASE CORRECTION AND PHASE CANCELLING NETWORKS IN QPSK MODEMS

Vasil Uzunoglu
Fairchild Industries
Germantown, MD 20874

Ann B. Maiorano
Fairchild Industries
Germantown, MD 20874

ABSTRACT

At bit rates lower than 100Mbit/s, the Synchronous Oscillator (SO) [1-4] has substantial tracking band combined with steep skirt selectivity to satisfy all the requirements of a carrier recovery network without the need for a phase correction network. At higher bit rates however, there is a need for a phase correction or phase cancelling network, if the BER variations with respect to hard wired case must be confined to less than 0.2dB with IF offsets of ±30kHz. At bit rates higher than 100Mbit/s, the multiply by four process in a QPSK modem deteriorates the signal-to-noise ratio by more than 15 dB (18dB at E_b/N_o = 6.4 dB) and the synchronization signal-to-noise ratio at the input to the SO drops below 0dB (−5dB at E_b/N_o = 6.4dB). This reduction in the signal-to-noise ratio reduces the tracking band of the SO which in turn increases the phase shift per unit frequency offset.

INTRODUCTION

Synchronous Oscillators (SOs) [1,4] have been used successfully as clock and carrier recovery networks in QPSK modems in continuous as well as burst mode operations. Experiments indicate that the quality factor of an SO, that is, its Tracking Band x Noise Rejection product is substantially higher compared to other synchronization and tracking networks, including the Van der Pol and Injection-Locked Oscillator [5-8]. In spite of this, at bit rates higher than 100Mbit/s, the synchronization signal for the carrier recovery has very low S/N (−5dB at E_b/N_o = 6.4dB) which reduces the tracking band of the SO and it results in high phase shift per unit frequency offset.

For example, for E_b/N_o = 6.4dB and frequency offsets of ±30kHz, the phase shift of the SO becomes as high as ±7°. This deteriorates the BER by almost 0.6dB for single SOs using

the multiply-by-four technique and almost by 1dB for SOs using data remodulation loop technique. The phase correction network (PCN) developed for the 120-Mbit QPSK-TDMA modem limits the BER degradation to less than 0.2dB. The PCN discussed in this paper is a universal one and can be used with any SO recovery technique.

CARRIER RECOVERY [9]

For carrier recovery two techniques are widely used, namely the multiply-by-four technique and the data remodulation technique.

For bit rates less than 100Mbit/s, the multiply-by-four technique results in S/N which is high. High S/N results in high tracking range, and, as a consequence, there is low phase shift per unit frequency offset. For example, for a 60-Mbit QPSK modem, an SO carrier recovery can have a tracking range of 8MHz at the center frequency of 280MHz.

For a ±50kHz frequency offset at 70-MHz IF, the phase shift (referred to 70MHz) amounts to ±2.25°, which affects the BER performance very little. On the other hand, in a 120-Mbit QPSK modem, the S/N level after the multiply-by-four process and filtering drops to less than 0dB. This low S/N reduces the tracking range to less than 1MHz, which results in a phase shift of ±18°/±50-kHz frequency offsets. As a result, the BER performance degrades considerably. The tracking range is determined by two factors:

1. the S/N of the input control signal; and

2. the division-by-four process.

For example, at E_b/N_o = 6.4dB with divide-by-four process, the tracking range is degraded by an order of magnitude.

It is not possible to improve the S/N level of the IF signal in a 120-Mbit QPSK modem after the multiply-by-four process if acquisition time must remain fast. But, by deleting the division process in the SO, over half an order of magnitude of tracking range is restored.

A PHASE CORRECTION NETWORK FOR BPSK*

One of the accepted PCNs presently in use is shown in Figure 1.

The 140-MHz recovered carrier is applied to a BPF with a center frequency of 280 MHz. This implies that the second harmonic of the 140-MHz IF is recovered through the filter.

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* PBSK = Bi-phase Phase Shift Keying

This is possible if the 140-MHz IF is rich in second haromonics, which may not be the case. Therefore, it is often necessary to multiply the 140-MHz IF frequency by two to secure the 280-MHz frequency. The output of the BPF1 must be applied to an RF amplifier to make up for the losses. The output of the RF amplifier 1 is applied to a hybrid divider which supplies one input to the BPF2 and the other input to the mixer M. The output of BPF2 is amplified again by A2 to compensate for the losses in the BPF2. This 280-MHz signal is divided by two applied to mixer M. The inputs to the mixer are given by

$$\sin (2\omega t \pm 2\theta) \quad (1a)$$

$$\sin (\omega t + 2\theta) \quad (1b)$$

and the output of the mixer becomes

$$1/2 \cos \omega t \quad (2)$$

where phase shift θ is eliminated from the output.

The efficiency of this technique relies heavily on the performance of the 280-MHz BPFs. They must have the same phase relations and insertion loss; otherwise there will be a high and varying phase error.

A NEW DESIGN

A new PCN in connection with the carrier recovery network is shown in Figure 2.

This section in thick lines represents the phase correcting network. It uses one mixer, one operational amplifier, a hybrid divider, and a phase reference delay cable to establish the proper operating point for the phase shifter $\emptyset$. This delay element can usually be deleted. The phase error between the input and the output of the SO is detected by the mixer M. The output of the mixer is applied to the amplifier which performs the necessary amplification to supply the proper amount of control voltage to the phase shifter $\emptyset$.

The output voltage variations versus the phase difference between the inputs of the mixer is given in Figure 3. It supplies ±35 mv for the ±30-kHz frequency offset.

The phase shifter introduces $\pm 7^o$ phase error for ±30kHz frequency offset, and per unit volt at its control input, the phase changes by 10^o (10^o/V). Therefore, to correct for $\pm 7^o$ phase shift, the phase shifter $\emptyset$ input must be ±700mV. Both the phase shifter $\emptyset$ and the phase detector are operating on their linear regions. The phase shift variations versus input control voltage of the phase shifter $\emptyset$ is shown in Figure 4.

It is found experimentally that the phase shifter has minimum VSWR at 6V bias level. At this bias level, the phase shifter has 120^o phase shift. This point is referenced to 0^o by using a coax cable which introduces 6^o phase shift per one inch. The operational amplifier accepts ±35mV and delivers ±700mV to the phase shifter ∅ to correct for the total phase shift within ±30-kHz frequency offsets. The complete circuit of the operational amplifier is shown in Figure 5.

The BER curves for the phase correction due to ±30-kHz frequency offsets are shown in Figure 6. The +30-kHz offset curve coincides with the no offset curve, whereas the −30kHz differs by less than 0.2dB. This difference is due to the frequency offset between the incoming IF and the SO natural frequency.

The above PCN is simple and inexpensive, and it can be added easily to any carrier recovery network using an SO without disturbing the basic operation of the modem. It degrades the acquisition time of the modem by less than 100μs.

It is possible to introduce other techniques in the design of phase cancelling networks, such as using a semiconductor delay element in series with the SO, where a change in frequency is detected and applied to the semiconductor delay element to change the electric field, which in turn changes the delay of the signal.

Another possible method is the adjustment of the center frequency of the bandpass filter as the frequency changes. This can be done by a varactor diode inserted as a tuning element into the bandpass filter.

The acquisition time of a 120Mbit/s modem including the phase correction network is shown in Figure 7. The E_b/N_o was 6.4dB and the preamble consisted of 48 1's and 128 alternate 1's and 0's.

The total time allocated for acquisition is 2.8μsec. The SO with all its associated circuitry acquires in less than 450nsec.

PHASE CANCELLING NETWORK

A Phase Cancelling Network is shown in Figure 8. The first SO constitutes the carrier recovery. If the incoming carrier is not at the center frequency of the SO, the SO introduces a phase error of 2θ between its input and output. This error is cancelled in the circuit shown in Figure 8.

As

$$\sin \alpha \sin \beta = 1/2 \cos (\alpha - \beta) - 1/2 \cos (\alpha + \beta) \qquad (3)$$

Let

$$\sin \alpha = \sin (2\omega_t + 2\theta) \quad (4)$$

and

$$\sin \beta = \sin (\omega_t + 2\theta) \quad (5)$$

The output of the mixer at point A becomes

$$\sin (2\omega_t + 2\theta) - \sin (\omega_t + 2\theta) \quad (6)$$

which results in

$$1/2 \cos (2\omega_t + 2\theta - \omega_t - 2\theta) - 1/2 \cos (2\omega_t + 2\theta + \omega_t + 2\theta) \quad (7)$$

Equation (7) can be simplified as

$$1/2 \text{ cost } \omega_t - 1/2 \cos (33\omega_t + 4\theta) \quad (8)$$

At the output of the 14OMHz filter equation (8) becomes

$$1/2 \cos \omega_t \quad (9)$$

which does not contain the phase error 6.

PHASE SKIP CORRECTION

At E_b/N_o lower than 5dB where standard carrier recovery techniques fail to function properly, the SO carrier recovery continues to operate. Some random phase skipping may occur at very low levels of E_b/N_o. To avoid such skipping a phase skip correction network is used.

The block diagram of such a circuit is shown in Figure 9. BPF1 accepts the 140-MHz IF and, after quantizing it, passes to BPF2 and the mixer M. The 140-MHz IF is filtered further in BPF2 and then divided by two. Mixer M receives thus two signals, one from the divide-by-two network FD1 and the quantizer. Mixer M mixes the 140-MHz and the 70-MHz signals to produce 70 MHz. The signal from FD1 is also applied to another divide by two network FD3. The signal after the divide by two network FD1 is filtered twice, namely by BPF1 and BPF2. Thus, it has a better S/N than the signal S/N after BPF1. The 70-MHz output of mixer M has a relatively poor S/N. This implies that the S/N of FD3 is better than that of FD2. If there is no skipping, the outputs of FD2 and FD3 will be coincident and the exclusive-or gate IC1 will not be conducting, whereas IC2 will be

conducting. If there is skipping, IC1 will be conducting, which will correspond to half a cycle timing or 180^{o} phase shift. This phase shifted signal supplements the missing signal at the exact time to provide continuation of the carrier signal.

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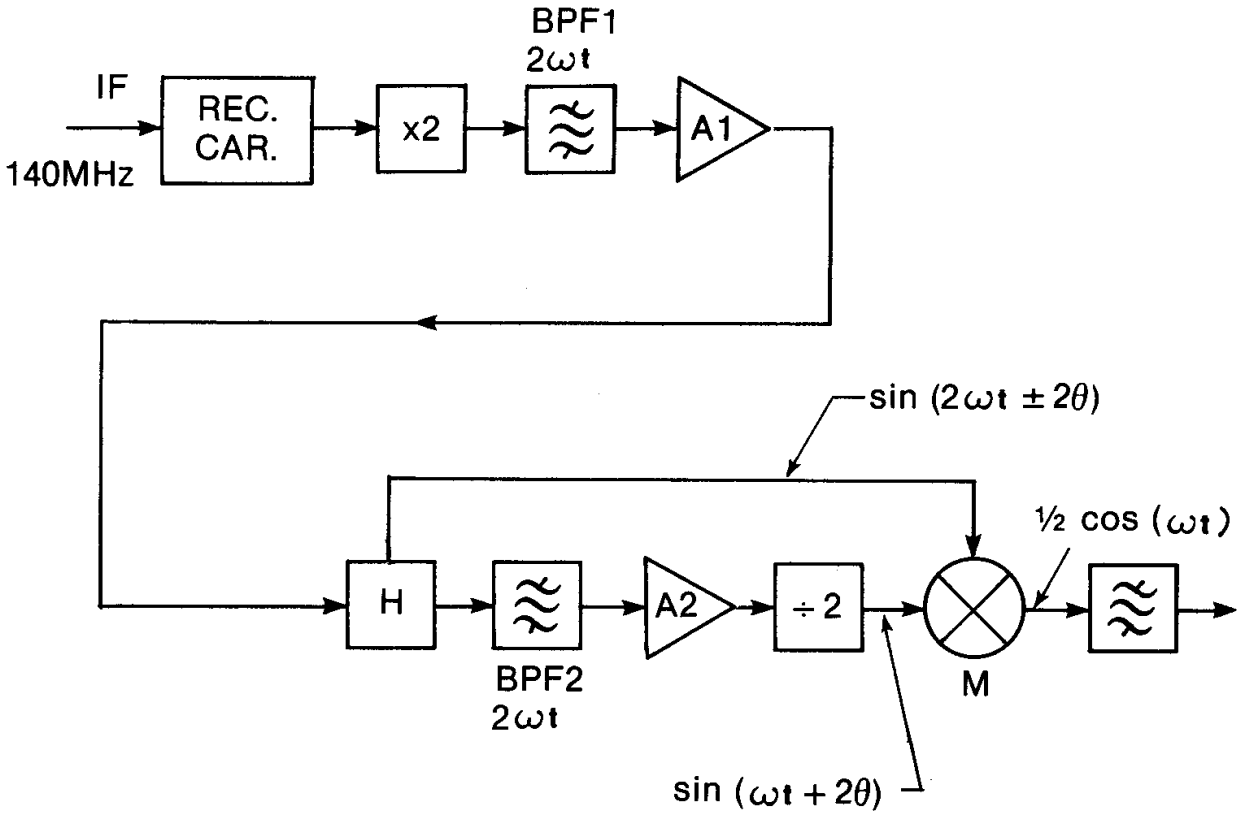

Figure 1. Phase Correction Network

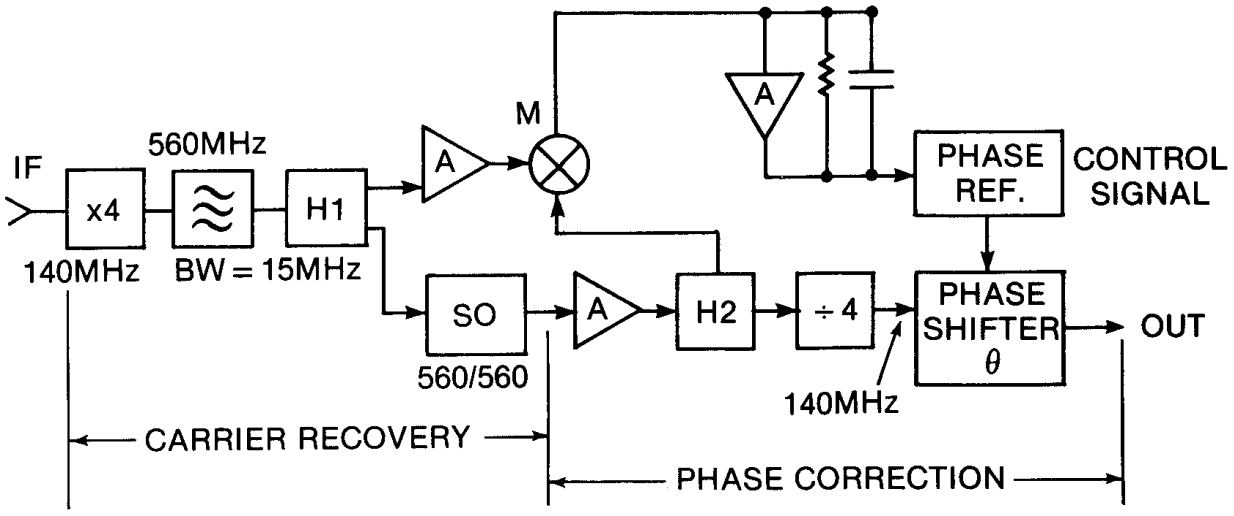

Figure 2. PCN Imbedded in Carrier Recovery Network

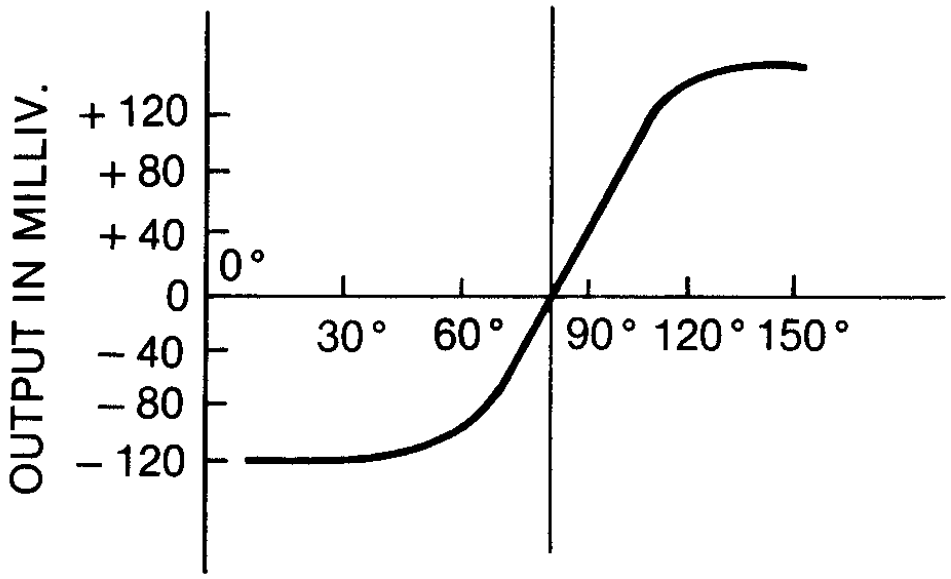

Figure 3. Output Voltage Variation vs. Phase Difference between Inputs of Mixer

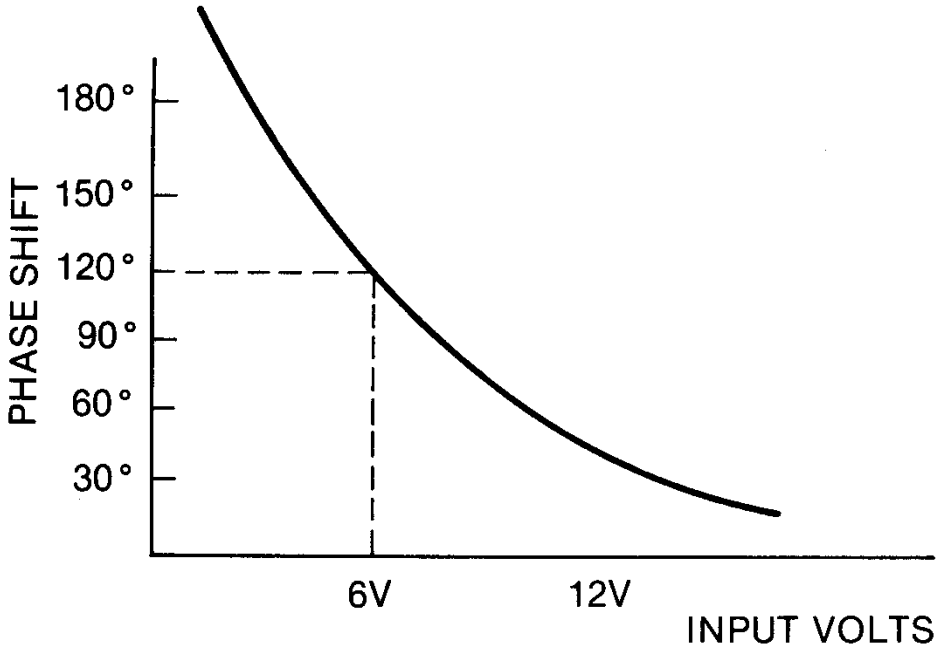

Figure 4. Phase Shift Variations vs. Input Control Voltage of Phase Shifter

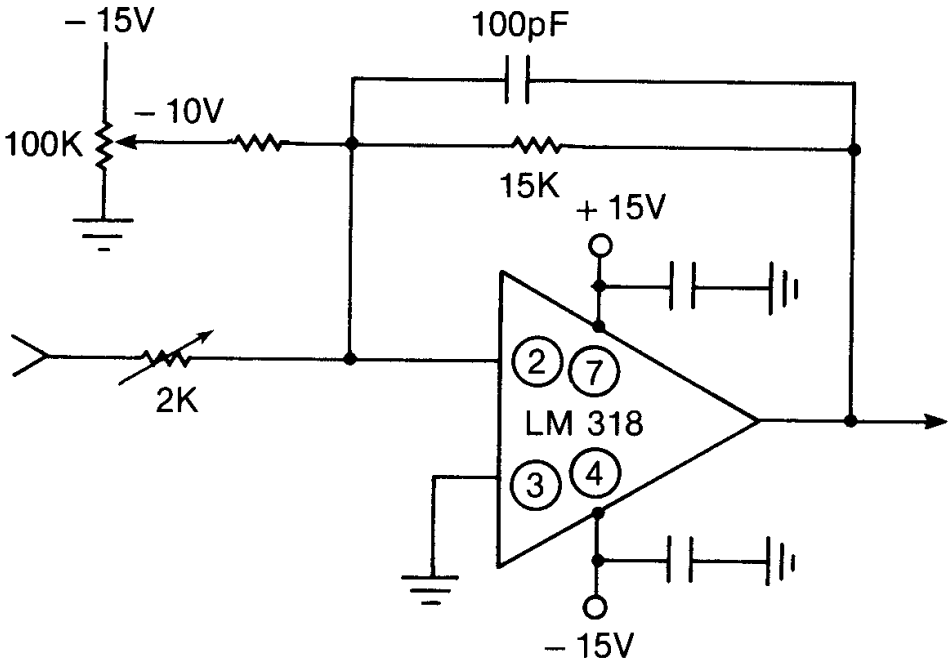

Figure 5. Complete Circuit of Operational Amplifier

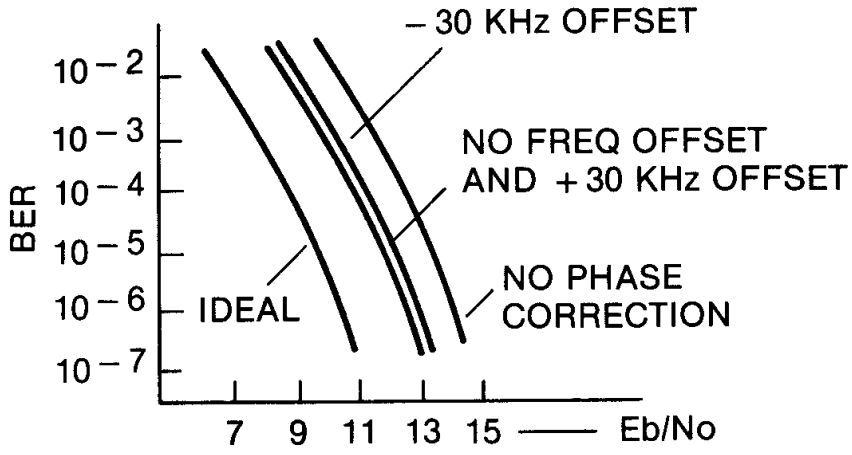

Figure 6. BER Curves with Phase Correction

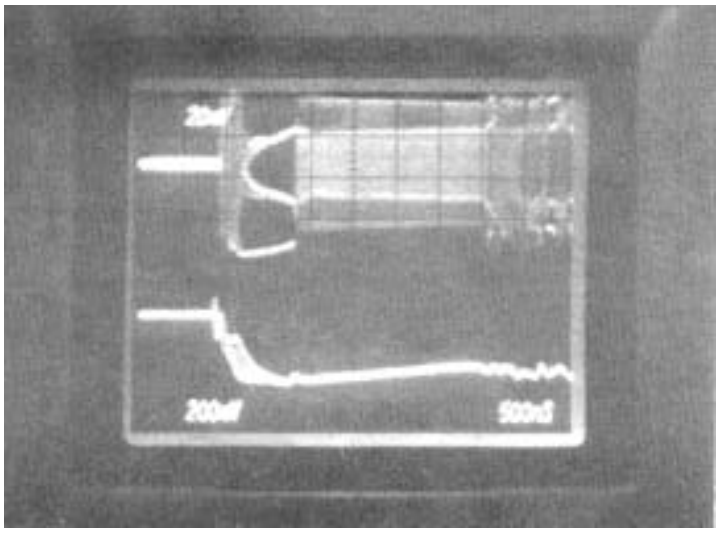

Figure 7. Phase Acquisition of a Carrier Recovery Incorporating Phase Correction

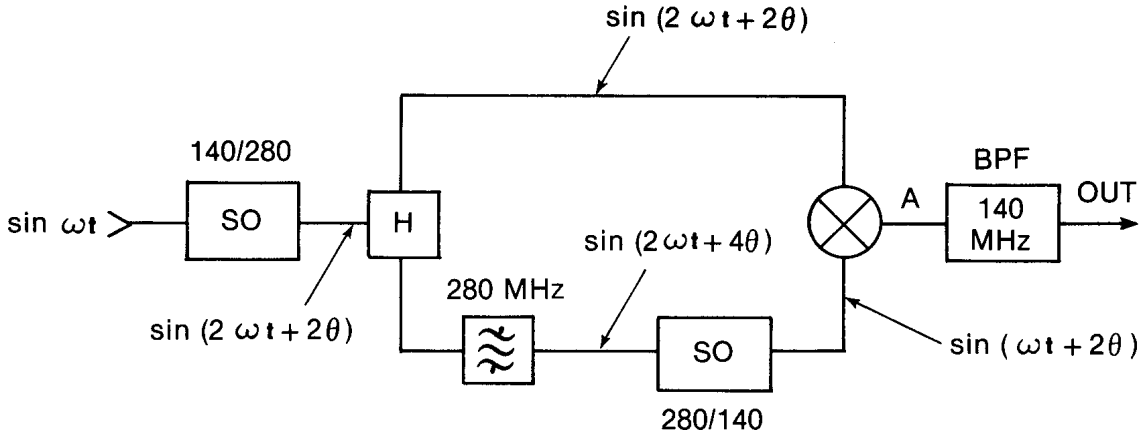

Figure 8. Phase Cancelling Network

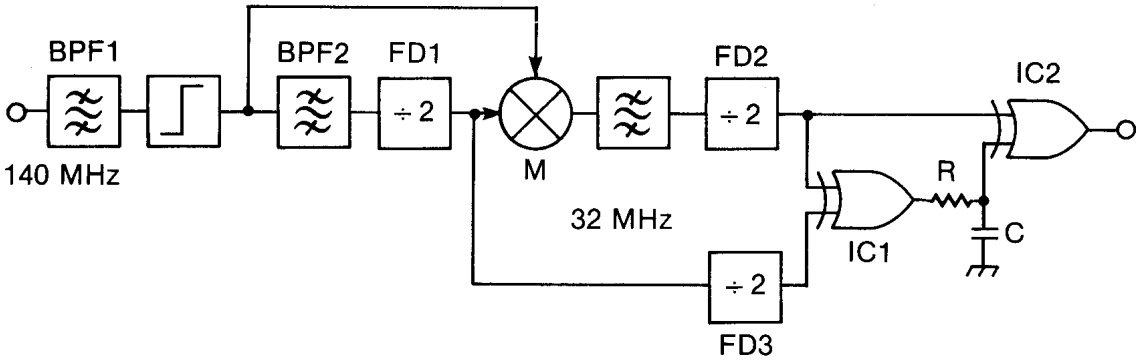

Figure 9. Basic Configuration of Phase-Skip Correction Circuit