EFFECT OF CLOCK JITTERS ON BIT ERROR RATE

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ABSTRACT

In this paper we have formulated a method of analysing the effect of clock jitters, which, even with the monomode optical fiber avaiable today, is still there to limit the operational distance of a digital fiber optic system. The main intention is to compare the system performance of a conventional binary system with that of a newly developed four-level pulse width modulation (PWM) system. Calculated results show an improvement in combatting clock jitters when using the four-level PWM system.

INTRODUCTION

For a digital optical fiber Communication system, it is well known that repeaterless distance of an optical fiber system is either loss limited or dispersion limited. With the emergence of monomode fiber and active devices available in the 1.55um wavelength range, effect of loss and dispersion are becoming lesser annoying, but the effect of clock jitters is still there to limit the operating distance of a digital optical fiber system [1,2,3,4]. So far we have not seen any papers giving analytical results regarding system performance degradation due to clock jitters. Reference [5] only gave experimental data on the relationship between error rate and static sampling offset. In this paper we attempt to introduce a method of analysing the effect of clock jitter on bit error rate with the special goal of comparing jitter effect on two digital optical systems, one is the conventional widely used binary PAM system, the other is a newly developed four-level PWM system (originally proposed by the auther), using time detection technique rather than ampltude detection, to utilize the wide bandwidth available with monomode fibers improving noise immunity of the system [6].

CLOCK JITTER AND BER RELATIONSHIP

4-level PWM system

At the transmitting end, four different pulse widths, each representing two different binary symbols, are sent along the optical fiber, while at the receiving end, three threshod gates of appropriate pulse widths are used to identify the pulse widths being sent [6]. Any clock jitters from the clock recovery circuit (here we used Phase Locked Loop for clock recovery) mean random time positioning of the threshold gate departing from its optimum timing position as shown in Fig. 1. In order to facilitate the calculation of the effect of clock jitter on BER, we solve the problem by assuming that no time jittering has occurred in the positioning of the threshold gate, but with additional pulse width jittering, this assumption is close to what actual happens in the detecting process, therefore clock jitters can be looked upon as pulse width jitters in incoming signals with ideal clocks from clock recovering circuit.

Total variation of incoming pulse width is

$$\Delta\tau = \Delta\tau_n + \Delta\tau_j \qquad (1)$$

here

$\Delta\tau_n$:pulse width variation due to thermal noise and shot noise inherent in optical signals.

$\Delta\tau_j$:equivalent pulse width variation due to clock jitters.

To find the relationship between clock jitter and BER, we have to find the probability density function (pdf) $P(\Delta\tau_n)$ and $P(\Delta\tau_j)$ of the random variables $\Delta\tau_n$ and $\Delta\tau_j$. Since $\Delta\tau_j$ is mainly determined by the parameters of the clock recovering circuit PLL and signal patterns, we can reasonably assume that $\Delta\tau_n$ and $\Delta\tau_j$ are statistically independent, so we have

$$P(\Delta\tau) = P(\Delta\tau_n) * P(\Delta\tau_j) \qquad (2)$$

where * denote convolution.

From Ref. [6] we have

$$P(\Delta\tau_n) = \frac{K_1}{\sqrt{2\pi}} \exp\left[-\frac{(K_1 \Delta\tau_n)^2}{2}\right] \qquad (3)$$

here

$$K_1 = \frac{V_{max}}{\sigma_t t_\sigma e} \qquad (4)$$

$$V_{max} = \left(\frac{\eta}{h\nu}\right) (qRA)\langle G\rangle \int_{iT}^{(i+1)T} P(\tau) h(t_i - t_\sigma + iT - \tau)\, d\tau \qquad (5)$$

η : quantum efficiency of APD

h : Planck’s constant

v : optical frequency

R.: input resistance of preamplifier

q : electrical charge

A : gain of amplifier
$\langle G \rangle$: average gain of APD
P(t) : optical power waveform
h(t) : impulse response of filter
T : reciprocal of bit rate.

$$\sigma_t = (\lambda_2 + \sigma_{th}^2)^{1/2} \tag{6}$$

σ_{th} : standard deviation of thermal noise of the amplifier
λ_2 : second culmulant of the output of the filter

$$\lambda_2 = \left(\frac{\eta}{h\nu}\right)(qRA)^2 \langle G^2 \rangle \int_{iT}^{(i+1)T} P(\tau) h^2(t_j + iT - \tau)\, d\tau \tag{7}$$

$$\langle G^2 \rangle = -(1-k)\langle G \rangle + 2(1-k)\langle G \rangle^2 + k\langle G \rangle^3 \tag{8}$$

k : ionization of APD.

Based on the procedures in Ref. [1] we can derive $P(\Delta\tau_j)$

$$P(\Delta\tau_j) \cong \frac{K_2}{\sqrt{2\pi}} \exp\left[-\frac{(K_2 \Delta\tau_j)^2}{2} \right] \tag{9}$$

Where

$$\frac{1}{K_2} \cong (1-P)\left[\sum_{j=1}^{\infty} \varepsilon_j^2 + \frac{1}{P}\left(\frac{\Delta f}{PK}\right)^2\right] B_L \tag{10}$$

Where
P : probability of symbol transition
ϵ_j : a factor associated with intersymbol interference
Δf : frequency offset of PLL
K : PLL gain
B_L : noise bandwidth of loop circuit.

Total pulse width variation $\Delta\tau = \tau - \tau_i$ where τ_j is the average pulse width with j=0,1,2,3. The p. d. f. of the random variable τ is shown in Fig. 2, where we can see how clock jitters affect the BER and why system performance degradation occurs.

Binary PAM system

As shown in Fig. 3 due to clock jitters sampling time deviate from its optimum value causing BER to increase. Along similar lines we can view the total amplitude variation ΔA

as generated by two statistically independent factors, ΔA_n and ΔA_j,
where

$$\Delta A = \Delta A_n + \Delta A_j \qquad (11)$$

A_n : amplitude variation due to thermal noise and shot noise.
A_j : equivalent amplitude variation due to clock jitters.

NUMERICAL EXAMPLE

Using the above derived equation and giving the parameters below, BER with and without the effect of clock jitters have been computed and tabulated in Tab. 1, also shown in Fig. 4.
Quantum efficiency of APD = 0.8
Ionization of APD = 0.02
Input resistance of amplifier = 700 Ω
Gain of amplifier = 1000
Optical frequency = 3.5×10^{14} Hz
Thermal noise of amplifier = 0.32×10^{-11} V/Hz
Bit rate = 100 Mb/s.

For 4-level PWM systems

Rise and fall times of the pulses are both 2ns with the four pulse width being t = 5ns, t = 8ns, t = 11ns, t = 14ns.
Period T = 20 ns.
Band width of the amplifier = 175MHz.
For binary PAM system, bandwidth of the amplifier is 50MHz.
Parameters of the PL.Lclock recovery circuit, normalized to bit rate are as follows:
Loop gain = 5×10^{-3}
Frequency offset = 10^{-5}
Loop circuit frequency 5×10^{-4}
Loop circuit damping factor = 0.707.
Calculated results have shown that 4-level PWM system, besides its noise immunity capability, is better than binary PAM system in combatting clock jitters.

CONCLUSION

In this paper we have introduced a method of analysing the effect of clock jitters on bit error rate. This will be of help in predicting system performance degradation when designing a fiber optical system. Experimental work is being carried out to support thepredicted theoretical results.

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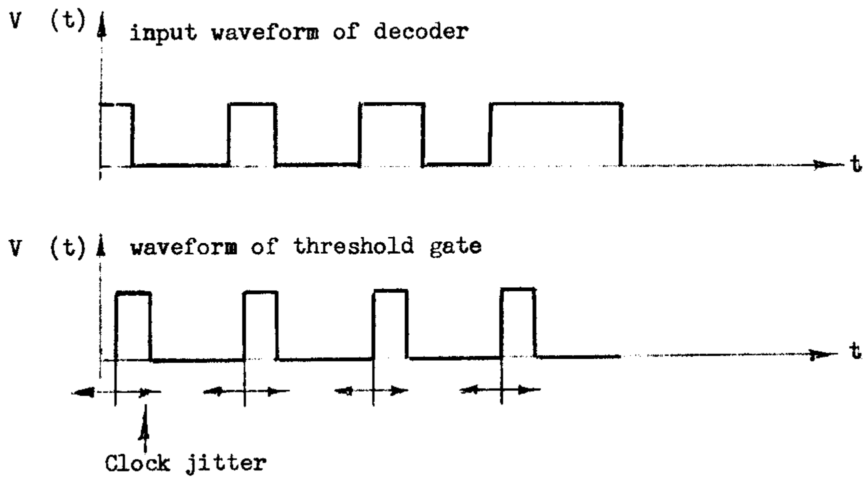

Fig.1 Clock jitters in 4-level PWM system

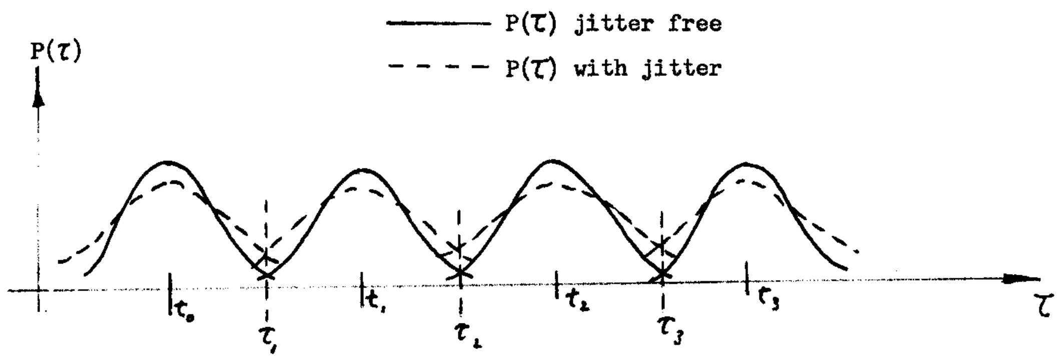

Fig. 2 Probability density function of 4-level pulse width with and wituout consideration of clock jitters

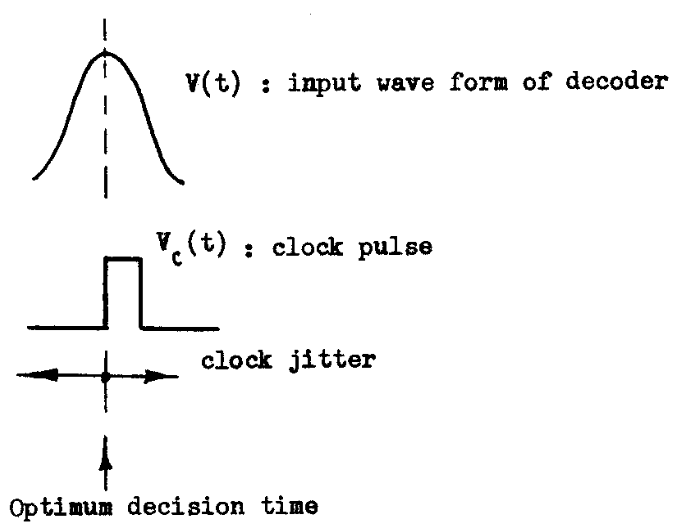

Fig. 3 Clock jitters in binary PAM system

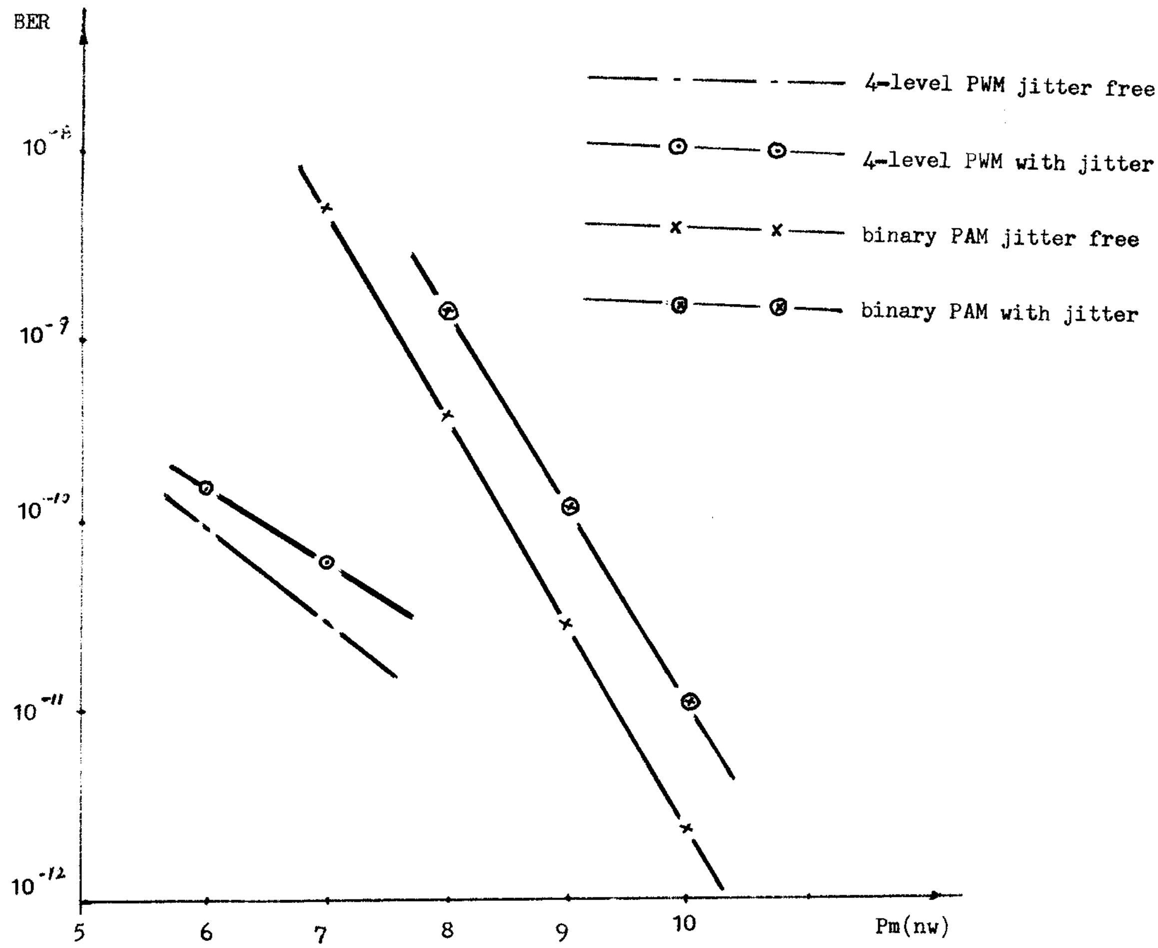

Fig. 4 BER versus Optical Power of binary and 4-level PWM systems considering the effect of clock jitters.

4-level PWM system			binary PAM system		
Optical power (nw)	BER jitter free	BER with jitter	Optical power (nw)	BER jitter free	BER with jitter
5	2.87×10^{-8}	4.36×10^{-8}	5	1.04×10^{-6}	2.26×10^{-6}
6	9.18×10^{-10}	1.69×10^{-9}	6	7.61×10^{-8}	1.82×10^{-7}
7	2.83×10^{-11}	6.62×10^{-11}	7	5.59×10^{-9}	1.52×10^{-8}
8	8.55×10^{-13}	2.65×10^{-12}	8	4.13×10^{-10}	1.31×10^{-9}
9	2.51×10^{-14}	1.07×19^{-13}	9	3.05×10^{-11}	1.18×10^{-10}
10	7.25×10^{-16}	4.45×10^{-15}	10	2.27×10^{-12}	1.1×10^{-11}

Table 1 BER versus optical Power with and without Clock Jitters.