

# FPGA-based rate-adaptive LDPC-coded modulation for the next generation of optical communication systems

DING ZOU\* AND IVAN B. DJORDJEVIC

Department of Electrical and Computer Engineering, University of Arizona, 1230 E Speedway Blvd., Tucson, Arizona 85721, USA

\*dingzou@email.arizona.edu

**Abstract:** In this paper, we propose a rate-adaptive FEC scheme based on LDPC codes together with its software reconfigurable unified FPGA architecture. By FPGA emulation, we demonstrate that the proposed class of rate-adaptive LDPC codes based on shortening with an overhead from 25% to 42.9% provides a coding gain ranging from 13.08 dB to 14.28 dB at a post-FEC BER of  $10^{-15}$  for BPSK transmission. In addition, the proposed rate-adaptive LDPC coding combined with higher-order modulations have been demonstrated including QPSK, 8-QAM, 16-QAM, 32-QAM, and 64-QAM, which covers a wide range of signal-to-noise ratios. Furthermore, we apply the unequal error protection by employing different LDPC codes on different bits in 16-QAM and 64-QAM, which results in additional 0.5dB gain compared to conventional LDPC coded modulation with the same code rate of corresponding LDPC code.

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## References and links

1. R. Rios-Muller, J. Renaudier, P. Brindel, C. Simonneau, P. Tran, A. Ghazisaeidi, I. Fernandez, L. Schemalen, and G. Charlet, "Optimized spectral efficient transceiver for 400-Gb/s single carrier transport," in *ECOC* (2014), paper PD.4.2.
2. J. Renaudier, R. Rios-Muller, P. Tran, L. Schemalen, and G. Charlet, "Spectrally efficient 1-Tb/s transceivers for long-haul optical systems," *J. Lightwave Technol.* **33**(7), 1452–1458 (2015).
3. S. Randel, D. Pileri, S. Corteselli, G. Raybon, A. Adamiecki, A. Gnauck, S. Chandrasekhar, P. Winzer, L. Altenhain, A. Bielik, and R. Schemid, "All-electronic flexibly programmable 864-Gb/s single-carrier PDM-64-QAM," in *OFC/NFOEC* (2014), paper Th5C.8.
4. ITU-T G. 975. 1, Forward error correction for high bit-rate DWDM submarine system, 2004.
5. D. Chang, F. Yu, Z. Xiao, Y. Li, N. Stojanovic, C. Xie, X. Shi, X. Xu, and Q. Xiong, "FPGA verification of a single QC-LDPC code for 100 Gb/s optical systems without error floor down to BER of  $10^{-15}$ ," in *OFC/NFOEC* (2011), paper OTuN2.
6. K. Sugihara, Y. Miyata, T. Sugihara, K. Kubo, H. Yoshida, W. Matsumoto, and T. Mizuochi, "A spatially-coupled type LDPC code with an NCG of 12dB for optical transmission beyond 100 Gb/s," in *OFC/NFOEC* (2013), paper OM2B.4.
7. D. Zou and I. B. Djordjevic, "FPGA implementation of concatenated non-binary QC-LDPC codes for high-speed optical transport," *Opt. Express* **23**(11), 14501–14509 (2015).
8. A. Leven, V. Aref, J. Cho, D. Suikat, D. Rosener, and A. Leven, "Spatially coupled soft-decision error correction for future lightwave systems," *J. Lightwave Technol.* **33**(5), 1109–1116 (2015).
9. (2015, Jul.). Technology options for 400G implementation [On-line], <http://www.oiforum.com/wp-content/uploads/OIF-Tech-Options-400G-01.0.pdf>.
10. R. Maher, A. Alvarado, D. Lavery, and P. Bayvel, "Modulation order and code rate optimization for digital coherent transceivers using generalized mutual information," in *ECOC* (2015), paper Mo. 3.3.4.
11. T. Koike-Akino, K. Kojima, D. Millar, K. Parsons, T. Yoshida, and T. Sugihara, "Pareto-efficient set of modulation and coding based on RGMI in nonlinear fiber transmissions," in *OFC/NFOEC* (2016), paper Th1D.4.
12. D. Zou and I. B. Djordjevic, "An FPGA design of generalized low-density parity-check codes for rate-adaptive optical transport networks," *Proc. SPIE* **9773**, 97730M (2016).
13. M. P. C. Fossorier, "Quasi-cyclic low-density parity-check codes from circulant permutation matrices," *IEEE Trans. Inf. Theory* **50**(8), 1788–1793 (2004).
14. M. Arabaci, I. B. Djordjevic, R. Saunders, and R. M. Marmorcia, "Polarization-multiplexed rate-adaptive non-binary-quasi-cyclic-LDPC-coded multilevel modulation with coherent detection for optical transport networks," *Opt. Express* **18**(3), 1820–1832 (2010).

## 1. Introduction

Current coherent optical transmission systems focus on single carrier solutions for 400-Gbit/s to support traffic growth in optical fiber communications, together with a few carriers frequency division multiplexed solutions for next generation data rate towards 1-Tb/s [1,2]. With the advance of analog-to-digital converter technologies, high order modulation formats up to 64-QAM with symbol rate up to 72-Gbaud has been demonstrated experimentally with Raman amplification [3]. To accommodate such high-speed optical communication system, the high-performing FEC engines that can support throughputs of 400-Gbit/s or multiple thereof are needed, which have low power consumption, providing high net coding gains at a target bit error rate of  $10^{-15}$ , and that are preferably adaptable to the time-varying optical channel conditions [4,5]. Recently, soft-decision binary and non-binary LDPC codes with an outer hard-decision code pushing the system BER to levels below target BER have been proposed in [6,7]. Meanwhile, a spatially coupled LDPC code has been demonstrated to have very low error floors below the system's target bit-error rate (BER) [8,9]. While it is essential to design an optimized FEC code offering the best coding gain, determining the optimal tradeoff between high-order modulation formats and the overhead of FEC codes is highly concerned in next generation 400-Gbit/s technology. Most recently, DP-QPSK, DP-16QAM, DP-64QAM, with varying code rates have been studied to achieve the highest generalized mutual information (GMI) at a given signal-to-noise ratio (SNR) and this study explored a total of 10 modulation formats to find the best combination of spectral efficiency and highest span loss budget [10,11].

In this paper, we propose an adaptive FPGA-based LDPC-coded modulation for the next generation of optical communication systems. Our motivation is two-fold. Firstly, a well-constructed capacity-approaching LDPC code offers the promise of substantial performance gain. Secondly, a unified architecture of LDPC decoder together with various modulation formats have been shown to allow a wide range of performances for OTN, where large number of parameters can be reconfigured in order to cope with the time-varying optical channel conditions and service requirements. The contribution of our paper can be summarized as follows: i) To the best of our knowledge, this is the first work on real-time implementation of rate-adaptive LDPC codes with overhead ranging from 25% to 42.9% in BPSK, QPSK, 8-QAM, 16-QAM, 32-QAM, and 64-QAM transmissions over spontaneous emission noise (ASE) scenario. ii) We provide detailed hardware architecture implementation and its explicit resource utilization and power analysis to help researcher better access its figure of merit. iii) We provide detailed analysis of rate-adaptive LDPC codes when applied to the higher-order modulation formats and demonstrate that an enhanced net coding gain (NCG) can be achieved with proposed rate-adaptive LDPC coded modulation schemes.

The rest of this paper is organized as follows. In Section 2 we first present the data flow of the LDPC-coded modulation emulator and the associate unified FPGA-based architecture and the corresponding performance, as well as the logic utilization, power consumption, latency, and throughput analysis. In Section 3, we then proposed a rate-adaptive LDPC coding scheme combined with higher order modulation formats. Section 4 concludes our paper.

## 2. FPGA-based LDPC-coded modulation emulator

Let  $LLR_{s_i}$ ,  $LLR_{b_j}$  represent the symbol log-likelihood ratio (LLR) of symbol  $i$  and bit LLR of bit  $j$  in one symbol, and let  $P(s_i | r)$  represent *a posteriori* probability of the symbol  $i$  given the received symbol  $r$ . For LDPC decoder, let  $R_{cv}^{k,l}$ ,  $L_{vc}^{k,l}$ , and  $L_v$  represent the check  $c$  to variable  $v$  message, the variable  $v$  to check  $c$  at  $k$ -th iteration and  $l$ -th layer message, and the LLR from the channel, respectively; where  $k = 1, \dots, I_{\max}$  and  $l = 1, \dots, \gamma$ . The layered scaled min-sum algorithm (with scaling factor  $s$  set to 0.75) is adopted in this paper [12]. The emulation processors can be summarized as Eqs. (1)-(6), where Eqs. (1)-(3) correspond

to symbol LLRs calculation (Eq. (1)) and bit LLRs calculation (Eq. (3)). On the other hand, Eqs. (4)-(6) correspond to the layered decoding algorithm.

$$LLR_{s_i} = \log(P(s_i | r) / P(s_0 | r)) \quad (1)$$

$$LLR_{b_j} = \log(\sum_{s_i(b_j)=0} P(s_i | r) / \sum_{s_i(b_j)=1} P(s_i | r)) \quad (2)$$

$$LLR_{b_j} = \max^* (\sum_{s_i(b_j)=0} LLR_{s_i}) - \max^* (\sum_{s_i(b_j)=1} LLR_{s_i}) \quad (3)$$

$$L_v^{k,l} = L_v + \sum_l R_{cv}^{k,l'} \quad (4)$$

$$L_{vc}^{k,l} = L_v + \sum_{l' \neq l} R_{cv}^{k,l'} \quad (5)$$

$$R_{cv}^{k,l} = s \times \prod_{v' \neq v} \text{sign}(L_{v'c}^{k,l}) \min_{v' \neq v} |L_{v'c}^{k,l}| \quad (6)$$

## 2.1 FPGA architecture

We study the performance of the proposed rate-adaptive LDPC-coded modulation in a field programmable gate array (FPGA) platform, whose high-level diagram is illustrated in Fig. 1(a). The platform consists of three parts: a set of PRBS 31 generators, a  $M$ -QAM mapper, two Gaussian noise generators, a symbol log-likelihood ratio calculator, a bit log-likelihood ratio calculator, a rate-adaptive LDPC decoder based on layered scaled min-sum algorithm, and an error counter circuit. The PRBS 31 generator is based on linear feedback shift register with a 31-bit initial value. A  $M$ -QAM mapper is stored in two read only memories (ROMs). The Gaussian noise generator using two linear feedback shift register (LFSR)-based uniform generator combined with Box-Muller algorithm generates samples of the white Gaussian noise. Such generated sequence of samples is multiplied with standard deviation of noise  $\sigma$  and fed to the symbol log-likelihood ratio block which is implemented based on Eq. (1). It is worth noting that the max star operation is replaced by max operation due to its simplicity. Then the quantized bit LLR is obtained based on Eq. (2) and fed to LDPC decoder based on Eqs. (3)-(5). In the architecture, a microblaze-based software configuration interface is implemented to set up initial configuration and to read from register. The setup process includes configuring noise variance, the number of iterations, and the length of shortening. Meanwhile, the BER is obtained by accessing registers storing the number of errors and the number of codewords that have been emulated.

The architecture of the code rate reconfigurable binary LDPC decoder is shown in Fig. 1(b). There are three types of processors shown in the figure: (i) variable node unit (VNU) based on Eqs. (3)-(4) will take input from memories  $L_v$  and  $R_{cv}$  and produce  $L_v^{k,l}$  and  $L_{vc}^{k,l}$ , (ii) scaled min-sum check node unit (CNU) based on Eq. (5) take inputs  $L_{vc}^{k,l}$  and produce  $R_{cv}^{k,l}$ , (iii) early termination unit (ETU) that is making a bit decision based on  $L_v^{k,l}$ . In addition, there are four types of memories in the implementation: (i) memory for  $R_{cv}$  with size of  $\gamma \times n \times W_R$  stores  $R_{cv}^{k,l}$ , (ii) memory for  $L_v$  with size of  $n \times W_L$  stores the initial LLRs, (iii) memory for  $\hat{c}$  with size  $n$  stores the decoded bits. In discussion above,  $\gamma$  denotes the column weight,  $n$  is the codeword length,  $W_R$  and  $W_L$  represent the word-lengths for  $R_{cv}$  and  $L_v$ . The most computational complexity block is involved in CNU, shown in Fig. 1(c). The ABS-block first takes the absolute value of the inputs and the sign XOR array produces the output sign. Then we find the first minimum value via binary tree and trace back the survivors to find the second minimum value as well as the position of the first minimum value. At last, we will reconstruct the output data from sign bits and the three outputs from

scaled two minimums' finder block. Furthermore, we can take advantage of the technique to significantly reduce the memory usage.

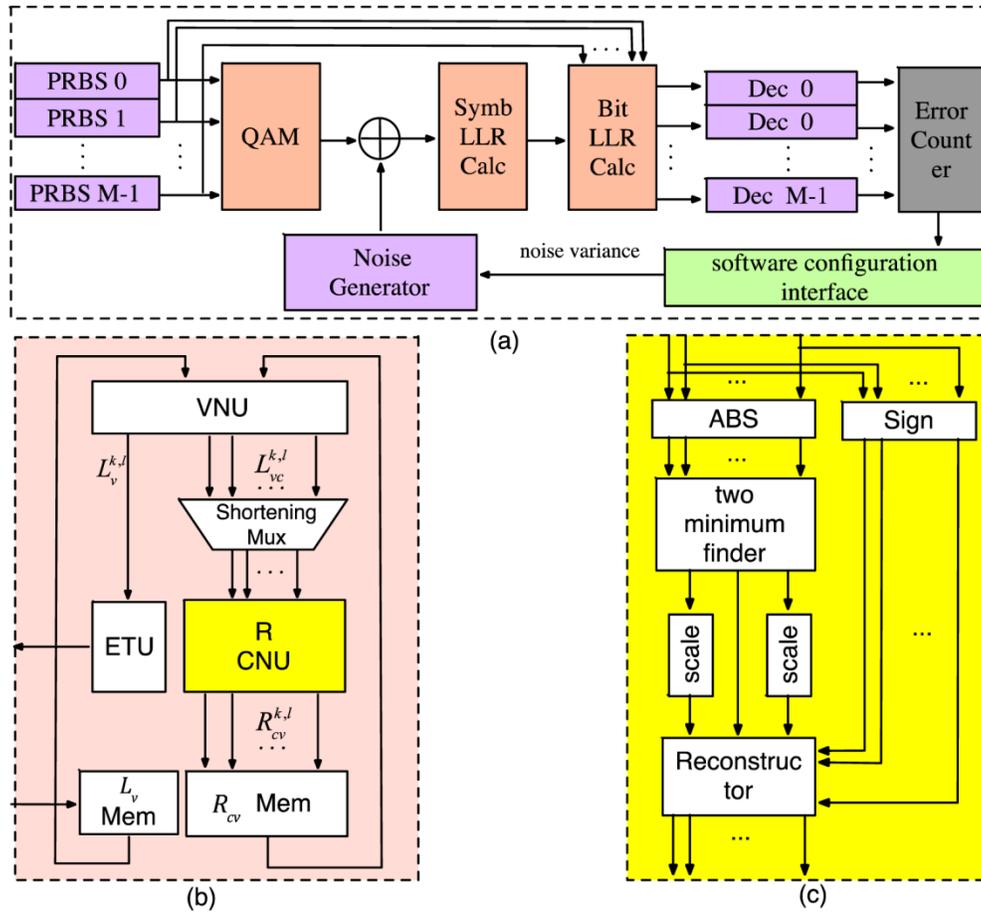


Fig. 1. FPGA architecture of rate-adaptive LDPC-coded modulation: (a) overall architecture, (b) architecture of LDPC decoder, and (c) architecture of check node processor.

### 2.2 Emulation results and analysis

The mother LDPC code (3, 15) (34635, 27710) is constructed based on permutation matrices due to its efficient implementation [13], and the rate adaptation is achieved by eliminating several blocks from a mother code by setting the initial log-likelihood ratio (LLR) into largest integer value. We employ the 8-bit uniform quantization scheme for messages ( $L_v$ ,  $L_{vc}^{k,l}$ ,  $R_{cv}^{k,l}$ ) to ensure that the error floor phenomenon is due to the code-design itself instead of finite precision representation, while keeping the decoding complexity reasonably low.

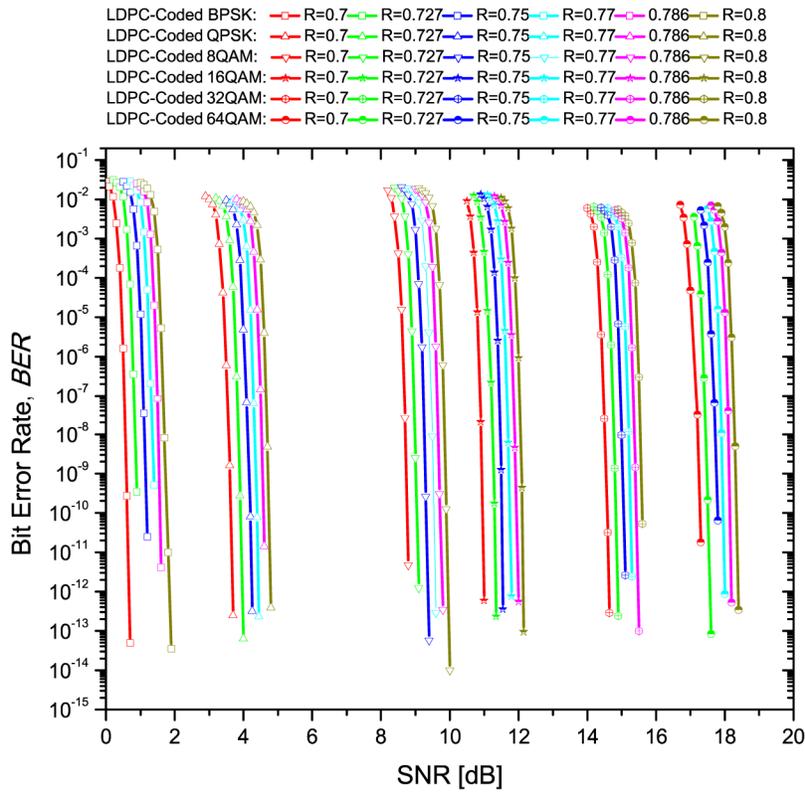


Fig. 2. BER performance curves for LDPC coded modulation with various code rates and modulation formats.

Table 1. Coding gains (in dB) of LDPC-coded modulation scheme.

| Code Rate | BPSK  | QPSK  | 16-QAM | 64-QAM |
|-----------|-------|-------|--------|--------|
| 0.7       | 14.28 | 14.28 | 13.92  | 13.79  |
| 0.727     | 14.02 | 14.02 | 13.58  | 13.53  |
| 0.75      | 13.71 | 13.71 | 13.33  | 13.29  |
| 0.77      | 13.52 | 13.52 | 13.12  | 13.12  |
| 0.786     | 13.33 | 13.33 | 12.92  | 12.91  |
| 0.8       | 13.08 | 13.08 | 12.78  | 12.72  |

The BER vs. SNR performance of the proposed rate-adaptive LDPC code with number of layered iterations set to 45 is presented in Fig. 2, in which we have shown a set of LDPC component codes of code rates {0.8, 0.786, 0.77, 0.75, 0.727, 0.7} in which rate-adaptation is performed via shortening, combined with a set of modulation formats, namely, BPSK, QPSK, 8-QAM, 16-QAM, 32-QAM, and 64-QAM. Table 1 presents coding gains at BER of  $10^{-15}$ , obtained via extrapolation. One can clearly observe that a flexible NCGs ranging from 13.08dB to 14.28dB can be achieved by employing the proposed rate-adaptive LDPC coding. Additionally, when combined with higher-order modulation formats, the proposed rate adaptation when applied to both component code rates and modulation format size can offer extremely flexible performance by adapting to time-varying optical channel conditions. It is worth noting that the coding gain decreases as the constellation size increases. We will explain and address this observation in next section.

### 2.3 Implementation analysis

Apart from error correction performance of the rate-adaptive LDPC-coded modulation, logic utilization, power consumption, and latency represent another important aspect. We compare the logic utilization and power consumption of six LDPC-coded modulation schemes, which have been implemented in Xilinx xc6vsx475t. Each emulator comprises  $\log_2(M)$  PRBS generators ( $M$  is the signal constellation size), one or two Gaussian noise generator for BPSK and others modulation formats, respectively, one symbol LLR calculator, one bit LLR calculator and one reconfigurable LDPC decoder. The resource utilization is summarized in Table 2. One can clearly notice that the occupied slices usage increases as the modulation format size increases, while the memory utilization is almost the same due to negligible amount of memory utilization except inside the LDPC decoder. In addition, the on-chip power consumption from clocks, logics, signals, BRAMs, DSPs, MMCMs, and IOs are shown in the last column in Table 2. The power consumption increases as we increase modulation format size, while this increase is reasonably low.

**Table 2. Logic Utilization and Power consumption summary of LDPC-coded modulation.**

| Modulation Formats | Occupied Slices            | RAMB36E1               | RAMB18E1              | Power (W) |
|--------------------|----------------------------|------------------------|-----------------------|-----------|
| BPSK               | 10% (7,724 out of 74,400)  | 10% (113 out of 1,064) | 6% (137 out of 2,128) | 1.205     |
| QPSK               | 10% (7,860 out of 74,400)  | 10% (113 out of 1,064) | 6% (137 out of 2,128) | 1.223     |
| 8QAM               | 11% (8,758 out of 74,400)  | 10% (113 out of 1,064) | 6% (137 out of 2,128) | 1.267     |
| 16QAM              | 12% (9,181 out of 74,400)  | 10% (113 out of 1,064) | 6% (137 out of 2,128) | 1.357     |
| 32QAM              | 14% (10,465 out of 74,400) | 10% (113 out of 1,064) | 6% (137 out of 2,128) | 1.538     |
| 64QAM              | 20% (15,182 out of 74,400) | 10% (113 out of 1,064) | 6% (137 out of 2,128) | 2.024     |

As we discussed above, we duplicate four LDPC-coded modulation emulators in one FPGA and with four FPGAs available in our rapid prototyping platform, in total 16 emulators are employed. Each decoder consists of 3 CNUs and 45 VNUs in the implementation, hence the throughput of the decoder can be calculated by  $F_{clk} \times n / [B / (p + \delta) \times I_{max}]$ , where  $F_{clk} = 200\text{MHz}$  is the FPGA running frequency,  $n$  is number of bits per codeword,  $B = 2309$  is the block size,  $p = 3$  is the pipeline depth,  $\delta = 7$  is the latency of VNP and CNP,  $I_{max} = 45$  is the maximum number of layered iterations. It is worth noting that the decoder will converge fast at high SNR regime ( $\sim 24$  iterations verified by simulation). The aggregation throughput of the mother code will be  $\sim 3.17\text{Gbit/s}$  at low SNR regime and  $\sim 5.94\text{Gbit/s}$  at high SNR regime, while the throughput of code rate of 0.7 will be  $\sim 2.11\text{Gbit/s}$  and  $\sim 3.96\text{Gbit/s}$  respectively.

### 3. Proposed rate-adaptive LDPC-coded modulation

The uncoded and coded BER performance vs. SNR of each bit in BPSK, QPSK, 8-QAM, 16-QAM, 32-QAM, and 64-QAM are shown in Figs. 3(a) and 3(b), respectively. A close look at Fig. 3 reveals that each bit in higher order modulation is protected unequally. For instance, the first bit and second bit have the same performance (the same applies for the third and the fourth bits) in 16QAM. Additionally, at input BER threshold of  $4.2 \times 10^{-2}$  of LDPC code with code rate of 0.75, the corresponding SNR limits of first and second bit in 16QAM are 9.37dB and 11.72dB, respectively. This phenomenon is illustrated in Fig. 3(b) as well since the SNR gap of coded BER is approximately 2.4dB. The overall SNR limit of post-FEC BER of  $10^{-15}$  will be limited by the worst bit performance, which inspires us to use our proposed rate-adaptive LDPC codes for different component bits combined with higher-order modulation formats. Another interesting observation is the best bit performance in 64-QAM is comparable to the worst bit performance in 16QAM. In addition, there are slightly different in the slope of performance curves associated with different bits in high-order modulation formats since the distribution of bit LLR is not Gaussian anymore.

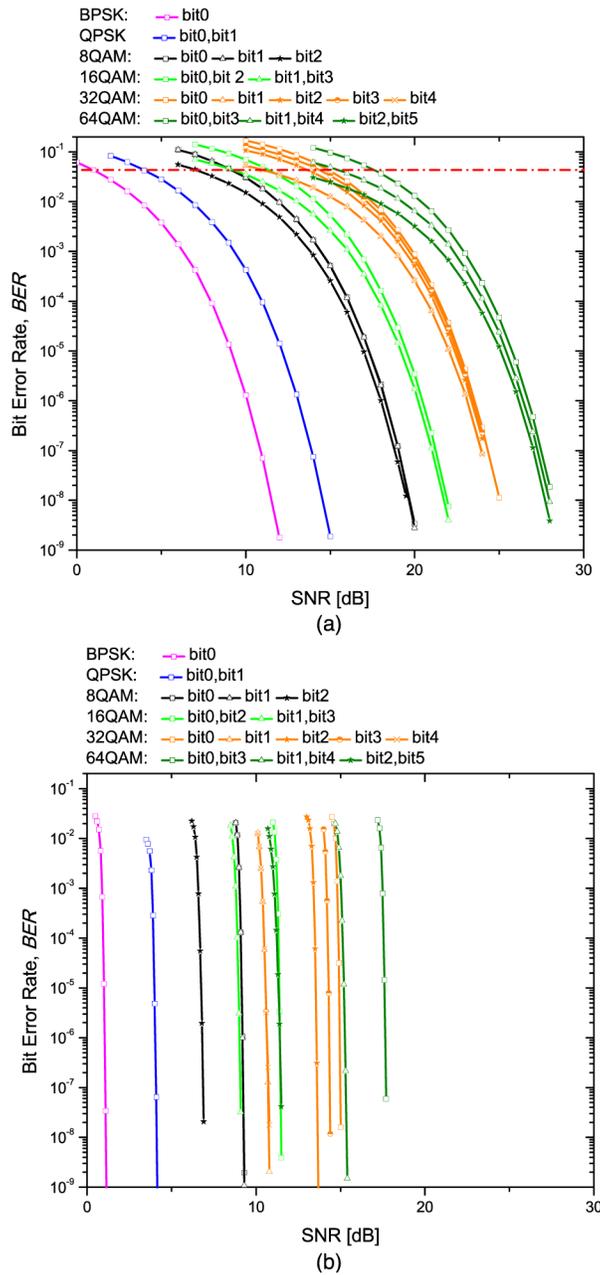


Fig. 3. BER vs. SNR performance for LDPC coded: (a) uncoded, (b) LDPC-coded cases.

In order to bridge the gap between different bits in high-order modulation formats, non-binary LDPC codes can be employed [14]. Due to its extremely high implementation complexity [7], we propose to use different error correction performance codes to different bits in high-order modulation format. Namely, instead applying code rate of 0.75 to all four bits in 16-QAM and six bit 64-QAM, we employ code rate of 0.7 to first and third bit and code rate of 0.8 to second and fourth bits in 16-QAM. Meanwhile, we apply code rate of 0.7, 0.75, 0.8 to the first and fourth pair, second and fifth pair, and third and sixth pair bit in 64-QAM; both configurations will result in the same code rate of 0.75. As shown in Fig. 4, the

BER vs. SNR performance reveals the existence of coding gain improvement of proposed scheme compared with the conventional scheme. More specifically, the proposed scheme provides 0.5dB additional gain at the BER of  $10^{-15}$  compared to the corresponding (3, 12)-regular QC-LDPC (27708, 20781) code when 16-QAM and 64-QAM are used. Meanwhile, there is no error floor phenomenon observed at BER of  $10^{-15}$  after  $\sim 10^{16}$  bits have been emulated, which implies the effectiveness of designing high-girth QC-LDPC code. It is worth noting that we can further bridge the gap between different bits in large constellation by more flexible component codes, however, addressing the difference of latency and the throughput of different component decoder will be very interesting.

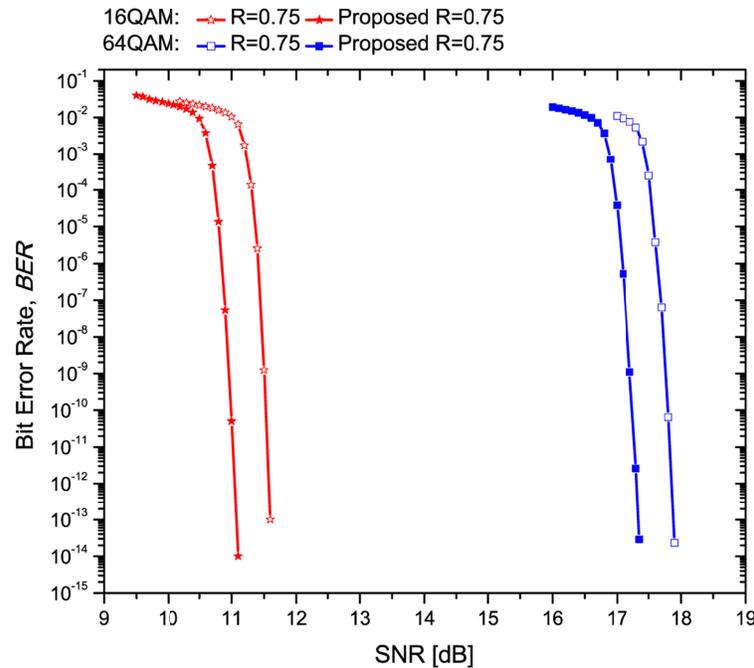


Fig. 4. BER performance vs. SNR with maximum number of layered iterations set to 45.

#### 4. Conclusion

In this paper, we have proposed a novel class of reconfigurable rate-adaptive LDPC codes with overhead ranging from 25% to 42.9% for high-speed optical transmission systems. The BER performance has been verified through FPGA emulation system and it has been shown that the proposed LDPC-coded modulation schemes exhibit a superior waterfall performance and excellent error floor performance down BER of  $10^{-15}$ . In addition, additional SNR gain of 0.5dB can be achieved by employing the rate-adaptive LDPC codes to 16-QAM and 64-QAM. To the best of our knowledge, this is the first FPGA implementation results of flexible LDPC-coded modulation. We believe that the proposed rate-adaptive QC-LDPC codes together with six modulation formats is one of the promising candidates for the next generation of optical communication systems.

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