Software Defined Radio MIMO Telemetry Transmitter

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ABSTRACT

This paper describes the development of a small, low-cost, and flexible telemetry transmitter that can be used for multiple-input multiple-output (MIMO) communication systems. In the intended application, the transmitter will collect data from sensors on small quad copters or drones, regarding the vehicle's attitude, location, movement, and other flight data. This will be combined into a single data stream, and base-band modulation applied by a field programmable gate array (FPGA). The FPGA output will control a separate RF modulation board, which will generate a pair of RF signals suitable for use in a 2x2 MIMO system. The original application uses the 902-928MHz ISM band. The modulation format can be altered by changing the software for the FPGA.

INTRODUCTION

This paper will discuss the plan for designing and building a transmitter board small enough to fit on a small airborne object. The physical size of the transmitter board will be approximately 200 sq. cm. The transmitter will initially be used for testing of a 2x2 MIMO system in an application where it is mounted on a rapidly spinning vehicle [1]. The transmitting antennas will be mounted on opposite sides of the object, causing them to go in and out of line sight with the receiving antennas on the ground, as illustrated in Figure 1.
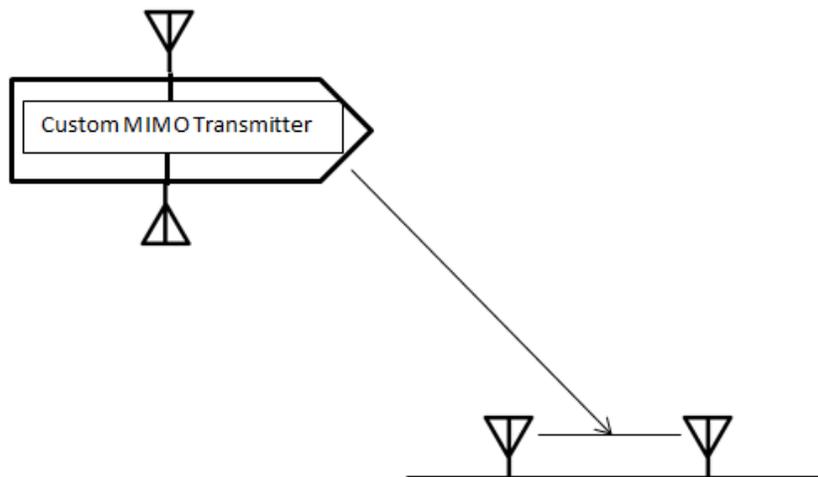

Figure 1 Geometry of the Problem

The ground receivers will typically need to estimate the channel coefficients, and/or combine the received signals using conventional MIMO techniques.

The receivers should be at a location where size, power and weight are not a significant concern. In addition, we expect the receivers can be protected from environmental extremes. Because of this, we plan to use commercial hardware for the receivers in this system.

We anticipate the transmitter will have more stringent constraints. We do not have highly defined specifications at the moment, but are assuming there will be significant size, power and weight constraints. We expect the transmitter may be subject to harsh environmental conditions, high acceleration, and may be on an expendable vehicle. These anticipated requirements motivated us to develop a custom transmitter board.

Another motivation for a custom transmitter was the ability to be flexible in both the transmit modulation and coding format, and also in the transmit carrier frequency. The initial system is intended to perform 2x2 Alamouti coding [2], BPSK modulation, and use carrier frequencies in the 900 MHz ISM band. However, the design is intended to be general enough that it can use other space-time block codes, convolutional coding, interleaving, other modulation formats, and carrier frequencies from approximately 900 MHz to 2.5 GHz. And with a full custom design, we hope to be better able to handle varying demands place on size and power sources.

MIMO TRANSMITTER

The transmitter will be broken into two separate printed circuit boards (PCB). The baseband data section will handle the entire digital signal processing components. This section will consist of a field programmable gate array (FPGA) logic block, along with a pair of Digital to Analog converters (DAC). The carrier section will perform I/Q frequency up-conversion to the desired carrier frequency. The sectional design will allow the user to change carrier frequencies simply by interchanging different custom carrier section boards.

The carrier section will initially be optimized to a frequency of 902-928 MHz. A follow-on design will extend this range by either altering the original board, or making a series of pin compatible boards to cover the frequency range from 900 MHz to 2.5. We anticipate transmission line constraints might limit us to a limited range of carrier frequencies for each board, but this is still an area of research for the team.

The expected bandwidth of the carrier board will be approximately 1 MHz, to allow simple modulation and coding of data rates in the range of 1 Mbit/sec. The clock rate for the data section will be sufficient high to allow multiple samples per transmitted bit, to accommodate pulse shaping and other coding and modulation constraints. A high level block diagram of the transmitter is shown in Figure 2.
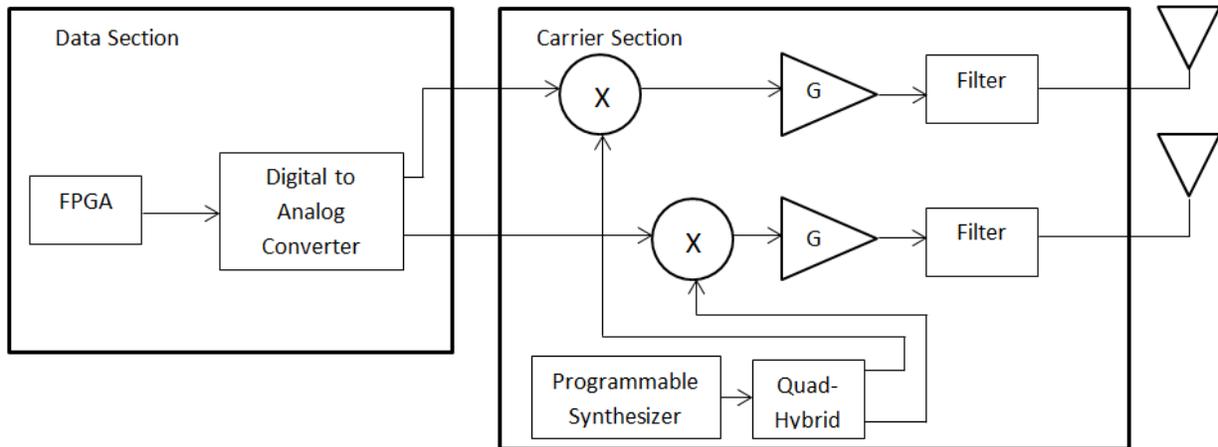
Figure 2 High Level Overview of Design

CARRIER SECTION

The carrier section of the transmitter is responsible for sending the signal received from the pair of DAC out through the antennas at a chosen carrier. This will be achieved by the use of several off the shelf products (COTS), micro strip technology, and custom PCB. We expect all the major components such as analog mixers, synthesizers, amplifiers, filters, antennas, clocks, and quadrature hybrid can all be COTS to save time development time and reduce both the recurring and non-recurring costs.

Four layer boards will be used to accommodate a multiple signal layers, a power layer, and a ground layer [3]. We have concerns the board may be used in environment with strict EMC constraints, so care will be taken in the design to insure minimal radiation from the board, and that the board operates in a robust manner when subjected to externally generated fields. Details such as the dielectric material to be used, and component placement is on-going, as we learn more about the constraints of the problem we are facing.

The output power levels may vary from one application to the next. The plan is for the base transmitter board to generate approximately 0 dBm of signal energy, and then to use external amplifiers to raise this to the power level needed for any particular application.

PROGRAMMABLE SYNTHEIZER

A synthiezer is responsible for generating the carrier signal. Most sytheizers generate the high frequency signal by exciting a crystal inside the VCO. There are many control options on the market for syntheizers. The most considered for this project are a voltage controlled fixed oscillator and a programmable PLL RF syntheizer [4].

The voltage controlled fixed oscillator that works in the ISM band would be the simplest, as it requires the fewest external components. The downside with this option is the limited flexiabilty because the carrier frequency, power level, and phase noise would be fixed.

The advantage of a programmble PLL RF syntheizer is it's flexabilty. The features that make it so flexiable include two outputs each having programmble frequencies, power levels, and phases. The price to pay for the flexiability is complexity. This surface mount chip requires an external 200 MHz oscillator, external loop filter to adjust the Q factor, serial interface components, many capaitors and resitors for the 40 pins, high frequency harmonics from the programmable channel dividers and a slighty higher cost. Since flexability is highly valued in this application, we consider the cost of the programmable PLL to be worth the extra cost. Initial simulations of the PLL have been completed and their performance estimated (Figure 3).
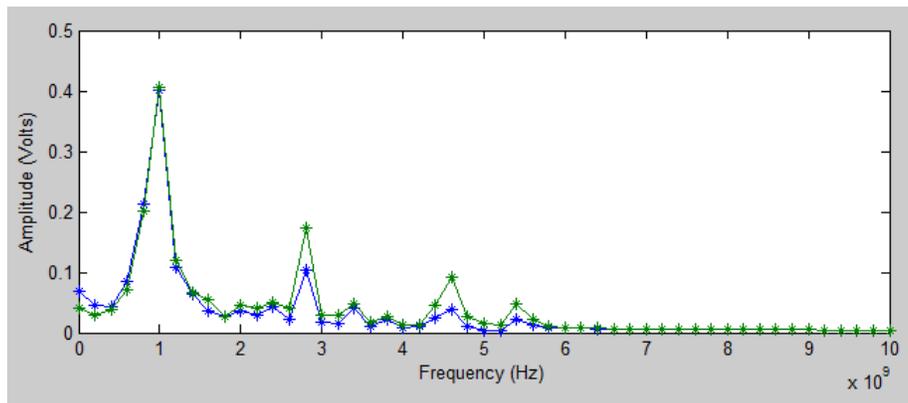

Figure 3 Fourier Transform of PLL synthesizer Outputs

QUADRATURE HYBRID

The quadrature phase shifter splits the input signal from the synthesizer chip into two output signals, to create a pair of sinusoids which are equal amplitude and 90 degrees out of phase with each other. There are many different ways to implement a 90 degrees phase shift, such using a branch line coupler, Lange coupler, 3 dB quadrature (90 degree) hybrids, or negative feedback loop amplifier circuits.

For this application, a COTS solution would be best due to project time constraints. If the needed phase shifter cannot be found on the market then the branch line coupler will be the next option. For this application a narrowband phase shifter would be sufficient. This eliminates a lot of the other microstrip options that are more complex. The geometry of the branch line coupler we are considering using as an alternative can be seen in Figure 4.
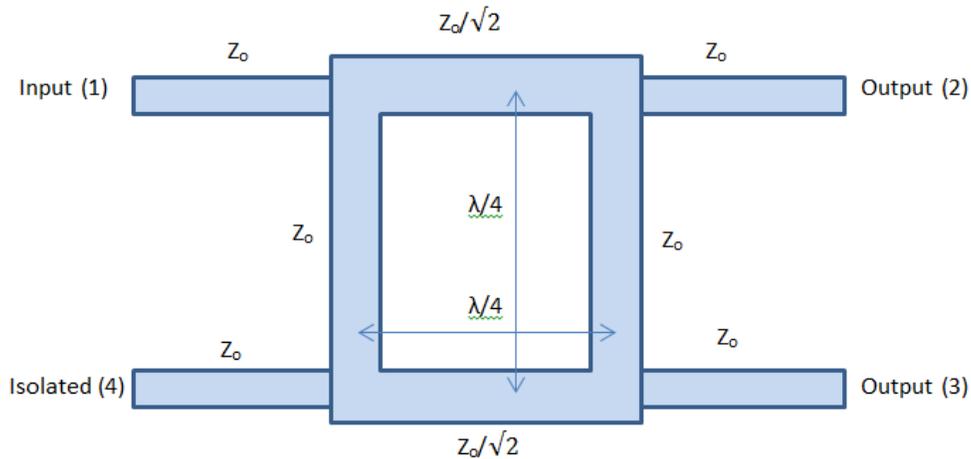
Figure 4 Branch Line Coupler

In Figure 4, Isolated (4) or pin 4 needs to be well grounded and shielded from outside noise for the system to work [5]. The difference in phase from the outputs is 90 degrees. The design of the branch line hybrid coupler will use 50 ohm micro strip lines on four layer PCB board with an undecided substrate material for a center frequency in ISM band.

Transmission line design tools such as LineCalc will be used to solve for the trace line dimensions (width and height) to get 50 ohm and 35.355 ohm impedance. The spacing can be solved by the equation below

$$\lambda = \frac{c}{f \times \sqrt{\varepsilon}}. \tag{1}$$

This method is simple in theory but maybe difficult to implement on a four-layer board. Trial boards will need to be manufactured to understand the difficulty of implementing this solution.

There are some potential limitations with the option. The user wouldn't be able to take advantage of thee programmable synthesizer because the hybrid coupler only works at a designed narrowband frequency. The synthesizer would only be able to be programmed slightly to counter de-modulation errors. A wideband phase shifter would need to be used to keep the programmable frequency functionality. Another disadvantage is the physical room needed which will be approximately 5 centimeters by 5 centimeters.

ANALOG MULTIPLEXER

After the data from the FPGA has been converted to an analog signal it will be joined with the carrier signal from the RF phase shifter. Several options are available for completing this process. The two being considered are the analog multiplexer and analog switch.

The multiplexer was chosen as it was more familiar and could complete the assignment dependably. Currently two multiplexers will be incorporated into the circuit, one for each output from the DAC. However, options are being considered to incorporating the process into one component. The features needed for the multiplexer include a wide bandwidth to

enable changes in frequency if needed and accommodate large data bandwidth sizes. In addition, having a laser-trimmed multiplier would eliminate external components. The part currently being considered is Texas Instruments MPY634KU.

RF AMPLIFIER

After the data and carrier signal are combined they will be sent to an RF amplifier. The RF amplifier will then boast the power levels, in turn, the signal radiating out of the antenna will be stronger. The most significant attributes that defines an RF power amplifier include output power, gain, linearity, stability, DC supply voltage, efficiency, and flexibility [6].

For this application, we are most concerned about linearity, stability, and DC supply voltage. Output power and gain are not as important for this application because of ISM band power regulations (1 watt output power maximum). Linearity and stability of the RF amplifier are important because we want the flexibility to change between many different types of data modulations. A low DC voltage supply is best to minimize the physical size of the design. Another option would be to pick an amplifier that requires the same voltage as a different component on the board. This would help minimizes the number of power supplies, or step or step down voltage circuits.

Some types of common amplifiers include class A, class B, class AB, class C, and class E. Type A amplifiers are used in low-power, high linearity, high gain, broadband operation, or high frequency operation. Another advantage with the Type A amplifiers are its low harmonics generated during the amplification process, since there are no sudden change in voltages or currents. There are less drastic changes in voltage and current because unlike the other types the class A conducts the full 360 degrees of its input. Type A is the most known amplifier in the group because it is commonly taught in electronics classes. The downside of the Type A amplifiers are their low efficiency. Another possible solution is the Class E amplifier.

Time is critical so a less time consuming option to implementing a custom amplifier design would be to buy an off the shelf amplifier. This method cuts down on external components which in turn safes physical PCB board space. The tradeoff for the saved space is less flexibility because one cannot change out external resistors, inductors, or capacitors to maximize the efficiency of the circuit.

RADIO FREQUENCY FILTER

We anticipate the need to have a band-pass or low-pass filter on the output of RF amplifier to attenuate harmonics and spurious emissions that all outside of the licensed band. We are still in the process of investigating the best method for implementing this filter. As the operating frequency is beyond the range of most operational amplifiers, we assume many active filter topologies would be impractical. For this reason, we are investigating engineering methods. Transmission lines or micro-strips can be laid out in such a way to build filters without lumped elements. Some examples of low-pass filters include L-C ladder type filters and semi lumped filters. End-coupled half-wavelength resonator, parallel-coupled half wavelength resonator, and the hairpin-line filters are examples of bandpass filters which we are current investigating

DATA SECTION

This section is best described as a digital signal processing application. This section will be very similar to an arbitrary waveform generator. This will be required to perform the necessary MIMO coding and modulation wave shaping. The coding will be stored in the FPGA's memory and activated when needed.

To maximize our chances of success we will implement error detection and correction techniques, and interleaving techniques. Error detection and correction are techniques that enable reliable delivery of digital data over unreliable communication channels. This code will become very valuable when we test over large distance. Interleaving is a technique of spreading error caused by interference such as lighting strike over many bytes instead of a centralized group of wrong bytes. This can be thought of as writing rows of data to a matrix, then reading that matrix as columns.

FPGA

The FPGA will be receiving the data from the sensors and sending it to the DAC. For this project a FPGA with at least 24 I/O ports needed. This includes I/O ports to accommodate the digital to analog convertor and interface to frequency. Moreover, the FPGA needs to have enough memory to collect the data needed to communicate with the drone or quadcopter and store signal processing modulation coding techniques.

There are many options in the market that would satisfy the criteria for this project. However, as Missouri S&T had the software and development board for the XEM6010 from Opal Kelly Incorporated, therefore this model will be chosen. In addition to the availability and low cost associated with the part, experience had been gained using it and the accompanying software from labs taken at the university. Moreover, the XEM6010's high-speed USB 2.0 interface provides fast configuration downloads and PC-FPGA communication. Additionally, the FPGA features the Xilinx Spartan-6 FPGA, 1 Gb (64 Mx16-bit) DDR2 SDRAM, high-efficiency switching power supplies. Quartus II Software and an Alter DE2 board (development and educational) with Cyclone II will be used to program the FPGA. Quartus software includes Graphical User Interface (GUI), VDHL Design Files, HDL or VHDL design file, and AHDL languages.

DIGITAL TO ANALOG

The DAC is the link between the FPGA and the multipliers and is responsible for providing an analog signal from the digital data given by the FPGA. The preforming function at this step of the process is a standard procedure and there are many components to choose from to complete it. The ideal component needed for this project will have at least a dual 10 bit voltage output with buffered reference inputs. Though a DAC with an internal state machine is an option, this project will use an external one. Additionally, to simplify this part of the project the DAC will have a single voltage supply and will be capable of repeatable startup conditions. A DAC with a fast enough sampling rate will need to be chosen to avoid aliasing. If one is to slow then the

measured rotation of the airborne object will not be very accurate. Currently the best part found that fills the requirements is Texas Instruments TLC5618A.

CONCLUSION

This paper establishes an overall general plan to develop a small, low-cost, and flexible telemetry transmitter that can be used for multiple-input multiple-output (MIMO) communication system. This design has several advantages that make it best suited for research and development projects. The discrete component design will allow the transmitter to be easily modified for a wide variety of applications. The FPGA will give the flexibility to store my different data modulation techniques and troubleshooting algorithms. The modular design will make it possible to connect a variety of signal carrier boards.

If possible, a signal carrier board will have a programmable frequency ranging from 900 MHz to 2.4 GHz. These advantages will give this transmitter an advantage in flexibility over the single chip MIMO packages.

Once this transmitter is successfully built future work can focus on expanding its capabilities. The transmitter can be tested with additional higher frequency carrier. New signal processing technique can be programmed into the FPGA and tested. Due to the versatility and flexibility of this design, the transmitter can be used to solve other wireless transmission problems, other than 2x2 MIMO applications. Since all of the FPGA inputs aren't being used, work can go into sending more data to the FPGA from a variety of sensors. This board will hopefully be useful in a wide range of communication system development and testing laboratory settings.

REFERENCES

[1] Muralidhar, A. "Multiple-Input Multiple Output System on a Spinning Vehicle with Unknown Channel State Information", 2015 International Telemetry Conference, Las Vegas, NV

[2] Alamouti, S., "A Simple Transmit Diversity Technique for Wireless Communications", IEEE Journal on Selected Areas in Communications, vol 16, iss. 8, Oct. 1998

[3] Bowick, C., John B., and Cheryl J.. *RF Circuit Design*, Newnes/Elsevier, 2008, Amsterdam

[4] Banerjee, D., *PLL Performance Simulation and Design Handbook - 4th Edition*, Texas Instruments, 2006. Web. 16 June 2016. <http://www.ti.com/tool/pll_book>.

[5] Pozar, D., *Microwave Engineering*. Wiley, 2005, Hoboken, NJ:

[6] Cripps, S., *RF Power Amplifiers For Wireless Communications*, Artech House, 2006. Boston.

[7] Winder, S. *Analog and Digital Filter Design*. Amsterdam: Newnes, 2002.

[8] Hong, Jia-Sheng, and M. J. Lancaster. *Microstrip Filters for RF/microwave Applications*. Wiley, 2001, New York: