3D Printed Parts for a Multilayer Phased Array Antenna System

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Abstract—In this work, a 3D-printable multilayer phased array system was designed to demonstrate the applicability of additive manufacturing for RF systems. A hybrid process incorporating a thermal wire-mesh embedding method for conductors and thermoplastic material extrusion for dielectrics is employed. The designed phased array, operating at 3.5 GHz, consists of three functional layers: a 1-to-4 Wilkinson divider at the bottom, embedded voltage-controlled phase shifters at the center, and patch antennas on the top. Standalone parts of the proposed multilayer phased array were printed to verify the integrated dielectric-conductor printing process as well as the incorporation of active semiconductor devices at room temperature.

***Index Terms*—3D printing, Multilayer, Phased Array**

I. Introduction

PHASED array systems are commonly used for high gain antennas and provide electronic beam steering for communication and sensing applications. A phased array usually consists of multiple RF components including feed networks, radiating elements, and active devices such as phase shifters, amplifiers and switches. To reduce the system footprint and increase functionality while keeping a compact size, it is desirable to utilize a multilayer structure [1]. The conventional fabrication method for a multilayer structure is usually complicated, requiring high cost and / or high-temperature firing that may damage the embedded components or substrate [1-3]. Manufacturing fast prototyping, compact, reliable and low cost multilayer phased array system remains a challenge.

Additive manufacturing (AM), or often-referred to as 3D printing, has been argued to be the future of manufacturing given its huge potential in revolutionizing both design and manufacturing methodologies. 3D printing allows 3D objects with arbitrary geometry to be printed automatically layer by layer, enabling the realization of complicated geometries such as 3-D conformal shapes [4-10], gradient index structures [11, 12] and more flexible design [13, 14]. In addition, 3D printed systems can benefit from part consolidation eliminating conventional packaging and assembling processes and consequently reducing manufacturing costs. Thus, 3D printing may be a promising technique to manufacture RF components and systems.

To realize a multilayer phased array using 3D printing, both dielectric and conductive materials, as well as active devices need to be incorporated into the printing process. Conductive ink/paste is commonly utilized for the printing of conductive components [15-18]. However, the conductivity of the ink is much lower than regular bulk metal conductors [15, 17, 18], thus increasing loss and decreasing system efficiency. High-temperature sintering can increase conductivity [16] but may induce deformations or damage to the dielectric substrate, and prevent potential integration of active semiconductor devices. A novel 3D printing hybrid technique for fabricating functional RF components (antennas, microstrip) at room temperature that maintains good electromagnetic performance has been demonstrated in [19-21]. In these articles, the dielectric portion is printed using thermoplastic material extrusion [22], and the conductive portion is printed using an ultrasonical/thermal embedding technique that incorporates wire, mesh or foil structures and avoids the commonly required annealing process at high temperature while providing bulk metal performance at microwave frequency [19, 21]. This wire-mesh embedding technique is compatible with the material extrusion process and enables embedding semiconductor devices that are sensitive to temperature. Seamless integration of these two techniques allows robust and flexible RF components and potential RF systems to be fabricated with automation. In this work, for the first time, this hybrid printing technique combining dielectrics and conductors was applied to manufacture a multilayer phased array system, to explore the challenge and applicability of the printing technique for RF system integration. This work is more advanced than the current state of the art in 3D printed phased array components which primarily focus on conductive ink/paste traces on polymetric materials [23]. This work is different in that the manufactured metal conductivity using wire mesh embedding is about 10 times higher than conductive paste. In this work, the critical parts of the

The research presented here was conducted by The University of Arizona and The University of Texas at El Paso within the W.M. Keck Center for 3D Innovation (Keck Center). Through funding from the State of Texas Emerging Technology Fund, the Keck Center recently expanded to over 13,000 sq. ft., housing state-of-the-art facilities and equipment for additive manufacturing processes, materials, and applications. Specifically, this research was supported by funding from National Science Foundation under Award 0925220 and 1408271, the National Aeronautics and Space Administration under grant number NNX13AR17A, the Intelligence Community Postdoctoral Research Fellowship Program under grant no. 2012-12071000005, as well as the state of Arizona under TRIF. All statements of fact, opinion, or analysis expressed are those of the author and do not reflect the official positions or views of the Intelligence Community or any other U.S. Government agency.

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multilayer phased array were printed, demonstrating for the first time through experimental verification that the hybrid printing technique using thermaplastic extrusion and wire mesh embedding is applicable for RF system integration.

This paper is organized as the following. In Section II, design and implementation procedure based on 3D printing techniques for various parts of the phased array is described. In Section III, the experimental verification of the 3D printing method for the multilayer RF integrated system is presented. In Section IV, the conclusion is given.

II. Design and Implementation

The multilayer phased array (operating at 3.5 GHz), fed by a coaxial SMA (SubMiniature version A) connector from the bottom, was designed as shown in Fig. 1. It consists of three functional layers: a one-to-four Wilkinson power divider in stripline form at the bottom, four voltage-controlled phase shifters including DC bias lines mounted on grounded coplanar waveguides (GCPWs) at the middle, and four probe-fed patch antennas working at 3.5 GHz at the top. The patch antennas have a size of 23.36 × 31.07 mm^2 and are separated 45 mm apart. Good isolation between functional layers is achieved by inserting a ground between the adjacent layers. The vertical transitions from the coaxial connector to the stripline and the stripline to the GCPW are optimized to reduce the transmission loss between layers. Some through-substrate vias connecting grounds are added to ensure that only the desired mode is supported in the frequency band of interest. The system was designed with a minimum substrate layer thickness of 3 mm (detailed thickness as shown in Fig. 1(b)) since the thermoplastic extrusion printing method has a thickness resolution of approximately 0.1 - 0.4 mm. In the design, the metallic layers of the phased array system are made of copper (conductivity of 5.2x10^7) with a thickness of 0.1 mm. The substrate layers are made of polycarbonate (PC) thermoplastic with a dielectric constant of 2.7 and a loss tangent of 0.005. All individual parts were modeled and simulated using ANSYS HFSS software [24].

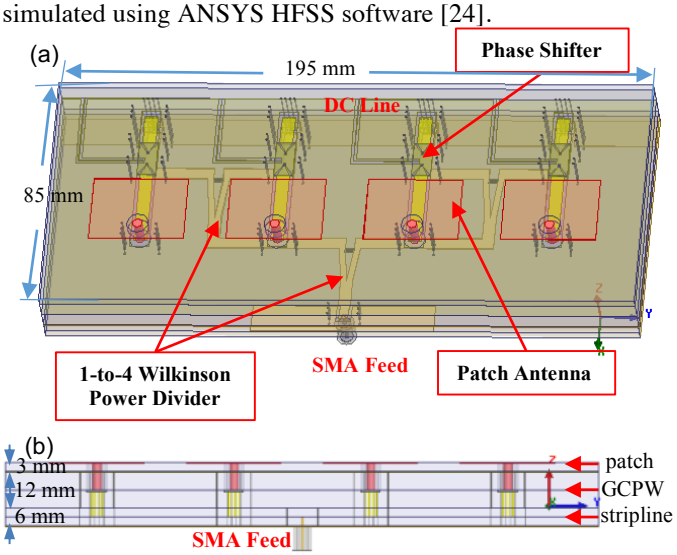

Fig. 1. Geometry of the designed 3D printable multilayer phased array: (a) perspective view and (b) side view.

To verify the phased array performance, the entire system (Fig. 1) was also simuated. The *S*-parameters of the phase shifter chip HMC928LP5E [26] under various bias voltages were included in the simulation. The array system shows a beam scanning range of +/-40° in the y-z plane (with respect to the z direction), which is reasonable for the 4–element array. It was observed that the array system has simulated reflection coefficients < -10 dB from 3.43 to 3.56 GHz and high directive beams (directivity 11.5 – 12.5 dB) at 3.5 GHz for various scan angles. The simulated array has a radiation efficiency of ~77% at scan angle of 0° at 3.5 GHz. Given these simulated results, it was determined that the proposed design is sufficient in order to fabricate and test 3D printed prototypes of each component of the phased array.

To determine the constraints necessary for manufacturing the full multilayer phased array system applying the integrated dielectric-conductor printing process as well as the incorporation of active devices at room temperature, individual parts of the array were fabricated. The printing process was completed using a multiple-interruption build sequence. A Stratasys Fortus 400mc material extrusion 3D printer with polycarbonate (PC) thermoplastic was employed to print the substrate. The Fortus 400mc was outfitted with a T16 printing tip to produce a printed raster of width and height of 254 µm. At each pause, the printed part was conveyed to an integrated gantry for the addition of through-substrate vias, mounting of components, such as resistors and phase shifters, and the submerging of metallic layers into the thermoplastic, whenever necessary. The through-substrate vias were realized using wire-mesh strips. The metallic layer was submerged using the thermal wire-mesh embedding method [21]. The procedure was to heat a wire mesh (0.1 mm wire diameter and 0.25 mm wire spacing) of a desired pattern using a resistive heater and simultaneously press the mesh into the thermoplastic – integrating plastic and metal structurally. After all necessary processes, the printed part was re-registered on the build plate of the 3D printer, and the build was resumed to print the subsequent substrate layers on top of the incomplete part. The additive process was repeated until the entire structure is finished. The full automation of the integrated printing and embedding process is under development [25].

III. Results

A. *Wilkinson Power Divider*

The one-to-four Wilkinson power divider is printed by the process discussed in the previous section. For testing purpose, five SMA connectors are mounted at the input and output ports. Figure 2(a) shows an image of the printed power divider without the upper substrate layer and top ground plane. Figures 2(b) and 2(c) show the top and bottom views of the completed divider with SMA connectors. The measured thicknesses of the upper and lower substrate layers are 3.4 mm and 3.7 mm respectively. The printing error in thickness is due to the re-registering process.

The *S*–parameters of the power divider were measured using an Agilent E8361A vector network analyzer (VNA). Good reflection coefficient performance was observed. The comparison of the measured and simulated (using ANSYS HFSS software [24]) transmission coefficients is shown in Fig. 3(a). It can be observed that the power divider exhibits

increased (0.9 to 2.9 dB) losses compared to simulations, and the measured losses have discrepancies among ports. The main causes of the discrepancies stem from potential contacting problems at the SMA-to-stripline transitions, stripline-to-SMA transitions, ground contacts and via contacts. For example, the substrate was made of PC, which has a glass transition temperature of approximately 155 °C. When soldering the SMA connector to the stripline using a soldering iron, the substrate underneath the wire mesh was unintentionally melted at the soldering temperature. Thus, the melted substrate penetrates the copper mesh, leading to weak contact between the SMA connector and the stripline. In addition, an unreliable connection between the ground and the ground vias can lead to undesired propagation modes, causing excess insertion loss. These contact / connection issues can be resolved by incorporating copper foil to replace wire mesh or by using low temperature soldering.

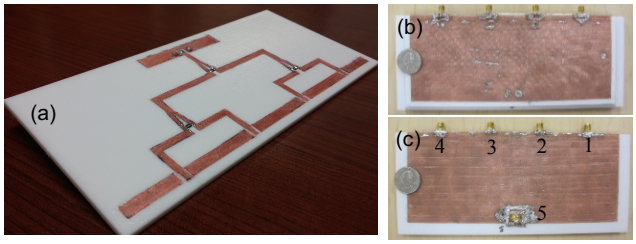

Fig. 2. Image of the printed 1-4 Wilkinson power divider: (a) without the top substrate and ground, (b) top view and (c) bottom view of the completed divider with SMA connectors.

As a verification of some of these loss-factors, a modified power divider model with a non-ideal contact between the bottom SMA and the stripline was simulated. To create this effect, the contact area between the center pin of the vertically mounted SMA and the signal trace of the stripline was reduced. In addition, the dielectric constant of the substrate was modified to 2.4 to include a non-ideal filling factor of the printed substrate, where the variation in porosity causes a frequency offset. The substrate thickness, which impacts the stripline impedance, was also altered according to the experimentally measured value. As shown in Fig. 3(b), the modified model has higher loss than the previous model and correlates better to the experimental results.

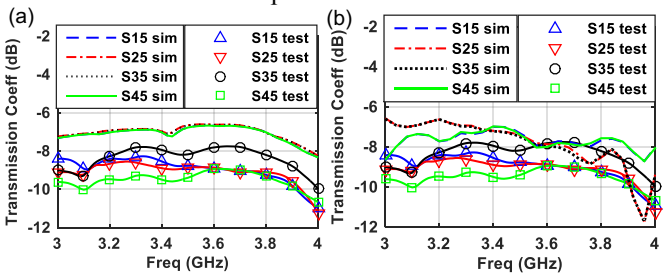

Fig. 3. (a) Measured and simulated transmission coefficients of the power divider. (b) Simulated transmission coefficients of the modified power divider model.

B. *Phase Shifter Structure*

The phase shifter structure was also printed. Figure 4(a) shows an image of the printed GCPW structure, incorporating a phase shifter without the upper-layer substrate and the top ground plane. An HMC928LP5E phase shifter chip [26] was mounted on an RT/Duroid 5880 board of a 31 mil thickness. Then the board was inserted into a pre-designed pocket in the GCPW. The phase shifter chip can also be connected using direct laser weld soldering. And this method is compatible for embedding other semiconductor devices. Figure 4(b) is the top view of the completed phase shifter structure with two N-type connectors for testing purpose. The measured thickness of the cover substrate layer is 6.1 mm, and the bottom substrate layer is 6.75 mm. The *S*-parameters of the phase shifter structure was measured using a VNA. A DC power supply (GW INSTEK PST3202) was used to control the bias voltage of the phase shifter. Good reflection coefficients were observed. The simulated and measured transmission coefficients are compared in Fig. 5(a) for bias voltages of 6V and 9V. The measured insertion loss (3 to 3.72 GHz) has 0 – 1.2 dB deviation from the simulated structure. However, the measured insertion loss is up to 4.7 dB higher than the simulation at 4 GHz. This increased insertion loss is primarily due to a spurious mode introduced by poor electrical contact between some ground vias and grounds. Figure 5(b) plots the normalized phase shift vs. bias voltage at 3.5 GHz, where the phase shift at 0V bias is used as the reference. The measured phase voltage sensitivity is close to the simulated result.

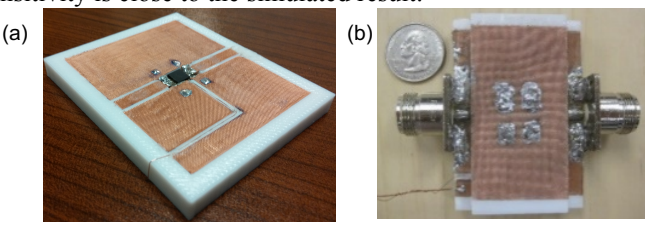

Fig. 4. Image of the printed phase shifter structure: (a) without the top substrate and ground, (b) top view of the completed structure with N-type connectors.

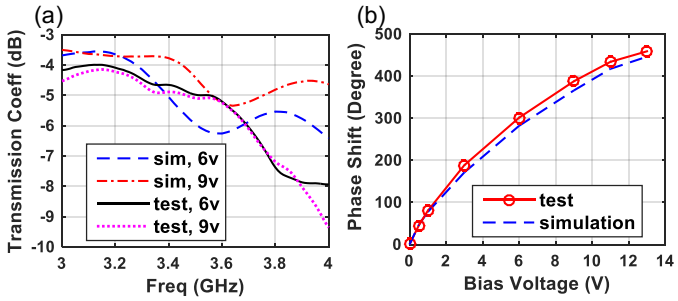

Fig. 5. Comparison of the simulated and measured (a) transmission coefficients and (b) the normalized phase shift vs. bias voltage at 3.5 GHz, of the phase shifter structure.

To verify that the connection between some ground vias and ground planes is the primary cause of higher loss observed at higher frequencies, a modified model was simulated. This model incorporates multiple open contacts between ground vias and the ground plane of the GCPW. For consistency, a dielectric constant of 2.4 and the experimentally measured substrate thicknesses were applied in the model. As shown in Fig. 6, the simulated results of the modified model are in better agreement with the experimental results, indicating the importance of reliable connections between the ground and the through-substrate vias.

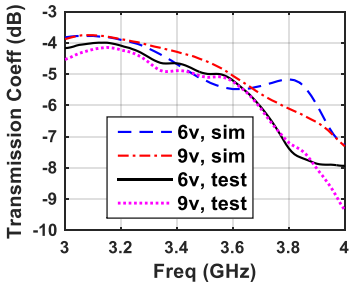

Fig. 6. Transmission coefficient of the phase shift layer from the measurement and the simulation of the modified-model.

C. *Patch Antenna*

Figure 7(a) and 7(b) are the top and bottom views of the printed patch antenna, which is probe-fed from the bottom GCPW. An N-type connector is edge-mounted to the GCPW for testing purpose. The measured substrate thicknesses from top to bottom (from the patch to the GCPW) are 4.8 mm, 6.4 mm, and 6.4 mm. The comparison of the measured and simulated reflection coefficients is plotted in Fig. 7(c). Good reflection performance is obtained. The slightly up-shifted working frequency is mainly due to the non-ideal filling of the printing material (porosity), which leads to a lower effective permittivity of the substrate. For antenna gain measurement, a calibrated double-ridged horn antenna (ETS / Emco 3115) was used as the reference antenna, and a WR340 horn antenna of 16-dB gain was used as the transmitter. The patch antenna under test was placed 3.16 m away from the transmitter (in the far-field zone of the transmitter), and the radiation pattern was measured using a VNA. The measured and simulated gain patterns at 3.5 GHz are mostly consistent for both co- and cross- polarization as shown in Fig. 8. However, the measured gain is approximately 2 dB lower than that of the simulation, which is attributed to measurement uncertainties and the probe-feed fabrication tolerance.

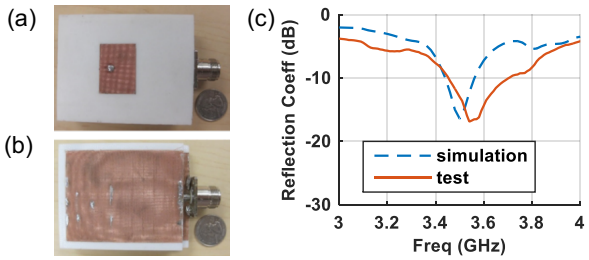

Fig. 7. Image of the (a) top view and (b) bottom view of the printed patch antenna with an N-type connector; (c) comparison of the simulated and measured reflection coefficients of the patch antenna.

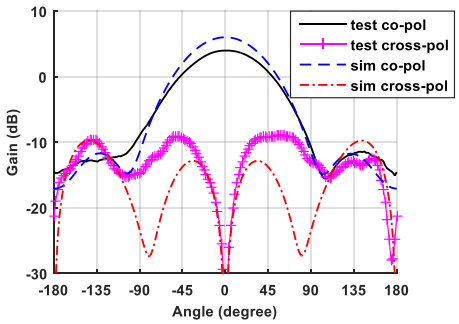

Fig. 8. Comparison of the simulated and measured antenna gain of the patch antenna at 3.5 GHz.

IV. CONCLUSION AND DISCUSSION

A proof-of-concept demonstration of an integrated dielectric-conductor printing technique at room temperature for microwave system is presented. A 3D printable compact multilayer phased array operating at 3.5 GHz was designed. All the relevant parts of this multilayer phased array were 3D printed at room temperature using the thermal wire-mesh embedding for the conductive portion and the FDM technique for the dielectric portion. An active phase shifter was also embedded during the build sequence. Measurement results of the functional parts are consistent with simulation, but with higher loss. The issue of potential contact problems between the coaxial connector and the stripline/GCPW and between grounds and through-substrate vias was investigated. Besides, the contact issue is currently being mitigated by incorporating copper foil to replace wire mesh [27] or by reducing the temperature of soldering. Another issue found from the proof-of-concept demonstration is the fabrication error in the substrate thickness, which is especially critical for applications at high frequencies. Despite the challenges found during the fabrication of the components of the multilayer phased array, this work represents a step forward that can help scientists advance toward the final goal of a fully functional 3D printed phased array. Overall, the reported techniques integrating conductor, dielectric parts, and active devices is promising for realizing multilayer microwave integrated systems, and has great potential to realize more sophisticated EM structures for microwave applications.

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