

ON CARRIER FREQUENCY AND PHASE SYNCHRONIZATION FOR CODED 16-APSK IN AERONAUTICAL MOBILE TELEMETRY

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ABSTRACT

This paper examines the problem of carrier phase and frequency estimation for coded 16-APSK in aeronautical mobile telemetry. Given the fact that coded systems tend to operate at lower signal-to-noise ratios than uncoded systems, the synchronizer must operate at these lower signal-to-noise ratios. For a 30 kHz frequency offset and a 10 Mbit/s 16-APSK signal, the conventional phase lock loop (PLL) system does not achieve consistent lock to be a useful approach. Consequently, a blind feed-forward approach, based on the FFT, and an initialized feedback approach based on the PLL were examined. The feed-forward estimator is capable of achieving BER ideal performance for $E_b/N_0 \geq 6$ dB using 1024 symbols. The feedback estimator, initialized using a feed-forward estimate based on 1024 symbols is also capable of achieving BER ideal performance for $E_b/N_0 \geq 6$ dB. Both synchronizers require a sufficiently good blind estimate: the estimate based on 2014 symbols appears to be the minimum value to achieve good performance.

INTRODUCTION

As a result of the loss of spectrum due to the AWS-3 auctions [1], there is increased interest in more bandwidth efficient transmission techniques. One of the obvious ways to increase spectral efficiency is to use a non-binary linear modulation with a bandlimited pulse shape. The challenge associated with using a non-binary linear modulation in aeronautical mobile telemetry is the greater-than-unity peak-to-average power ratio (PAPR) of these modulations. (In contrast, the current IRIG 106 [2] modulations PCM/FM, SOQPSK-TG, and ARTM CPM, are all variants of continuous phase modulation and therefore possess unity PAPR.)

PAPR is important when using an RF power amplifier in its non-linear mode. When $PAPR > 1$, the modulated carrier possess amplitude variations. These amplitude variations are compressed by the non-linear characteristic of the RF power amplifier. The compressed amplitude variations cause

signal distortion and significant spectral spreading. To reduce the spectral spreading, the input to the RF power amplifier is reduced to produce a signal that corresponds to the linear region of the RF power amplifier characteristic. This “linear” behavior is achieved at the expense of output power: the more linear the operating point, the lower the output power. For this reason, non-binary linear modulations with low PAPR are of interest.

16-APSK has one of the lowest PAPRs of all 16-ary linear modulations. This is why it was adopted by the DVB-S2 standard [3] for video broadcast from satellites. Motivated by its low PAPR, 16-APSK was investigated for CCSDS telemetry in [4]. The parameters of 16-APSK were optimized for aeronautical mobile telemetry in [5] and an accompanying pulse shape that minimizes PAPR was developed in [6]. The behavior of 16-APSK through RF-power amplifiers used in aeronautical telemetry was investigated in [7, 8, 9]. The performance of equalization methods for 16-APSK over the aeronautical telemetry channel was evaluated in [10].

Because the PAPR for 16-APSK is greater than unity, the *average* output power from an RF power amplifier is less than what it would be for the current IRIG 106 modulations. The reduced average output power reduces the received signal-to-noise ratio at the ground-based receiver. This, in turn, reduces the range over which a 16-APSK link can be maintained. To recover the loss in range, error control coding can be used. But because code rates are less than one, there is a spectral efficiency penalty associated with the error control code. For this reason, high-rate codes are of interest. The performance of the IRIG 106 LDPC codes was investigated in [11].

One of the consequences of using LDPC-coded 16-APSK with reduced RF power amplifier output is the fact that symbol and carrier phase synchronizers must operate at a lower-than-usual signal-to-noise ratio in aeronautical mobile telemetry. Carrier phase synchronization is particularly challenging because of the frequency offset due to oscillator uncertainty and Doppler. We show that the traditional phase lock loop (PLL)-based approach is unable to acquire lock at a low signal-to-noise ratio and with a typical frequency offset. This is a well-known fact. An alternative feedforward approach, based on a blind estimate using the FFT, was examined in [12] for DVB-S2 using QPSK. These results were expanded and extended to 16-APSK in [13].

In this paper we compare the feedforward approach to a “hybrid” approach where an FFT-based estimate is used to initialize a PLL. This “hybrid” approach is compared to a pure feedforward approach using the uncoded bit error rate (BER) as the basis for comparison. The results show that both approaches depend on the feedforward estimate. For the $E_b/N_0 \geq 6$ dB, a feedforward estimate computed from 1024 symbols is the minimum that produces ideal BER performance.

16-APSK FOR SERIAL STREAMING TELEMETRY IN AMT

16-APSK is a linear modulation with 16 4-bit symbols described by the constellation shown in Figure 1. The bit-to-symbol mappings are shown for each symbol. Because there are four bits per symbol, the symbol rate is $1/4$ -th the bit rate. The points are arranged in two concentric circles. This arrangement reduces the PAPR. The PAPR contribution for the constellation points is 1 dB (the pulse shape contributes more to PAPR). By comparison, the PAPR contribution for the tradi-

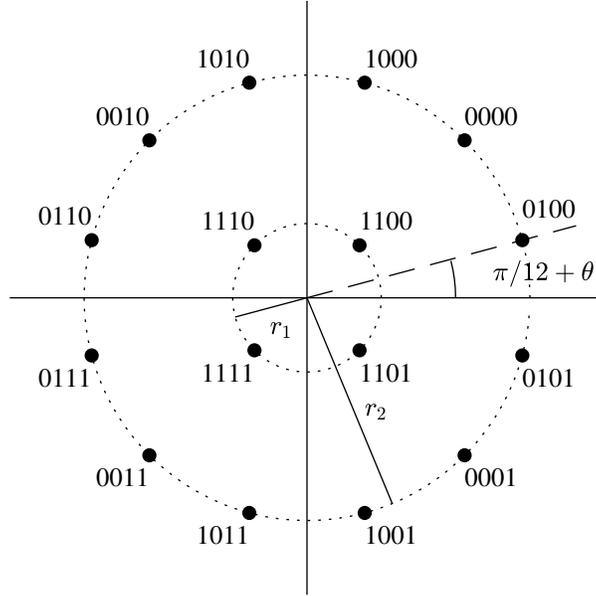
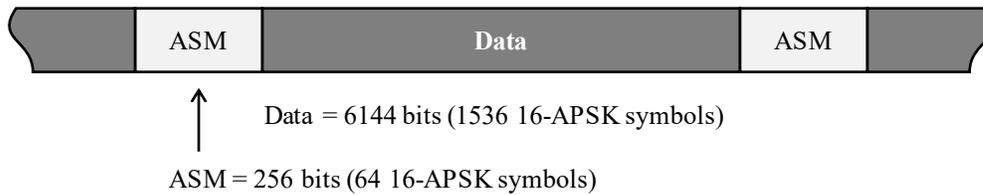


Figure 1: The 16-APSK constellation.



ASM = FCB88938D8D76A4F 034776C7272895B0 FCB88938D8D76A4F FCB88938D8D76A4F

Figure 2: The data format for serial streaming telemetry using 16-APSK.

tional square 16-QAM is 2.6 dB. The constellation is defined by two parameters, the ratio of the radii r_2/r_1 and the phase angle for the outer ring θ . The optimum values for these parameters in aeronautical mobile telemetry were derived in [5].

The data format for coded-16-APSK in serial streaming telemetry is illustrated in Figure 2. The data field corresponds to an LDPC codeword described in Appendix 2-D of IRIG 106-17 [2]. (The results presented below are for *uncoded* 16-APSK.) Preceding each codeword is the Attached Sync Marker (ASM). The results presented below use the “long form” of the ASM given in Table D-10 of Appendix 2-D of IRIG 106-17 [2].

We assume 10 Mbit/s (= 2.5 Msymbol/s) transmission with a 30 kHz frequency offset. Because of the reduced power due to PAPR, we are interested in carrier phase synchronization at relatively low signal-to-noise ratios, i.e., E_b/N_0 in the range 6 dB to 12 dB.

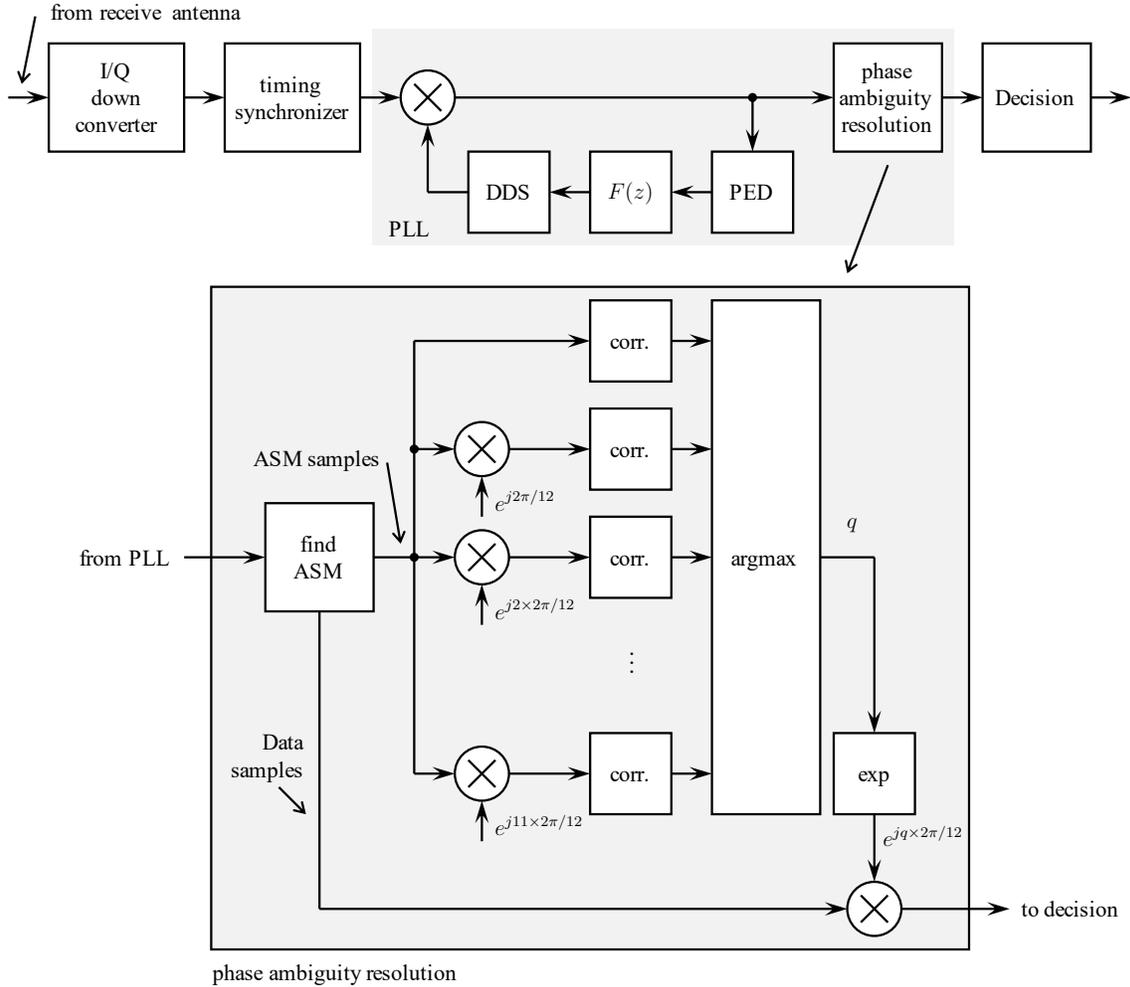


Figure 3: A block diagram summarizing the PLL-based approach.

PLL-BASED METHOD

The first technique investigated is based on a traditional discrete-time carrier phase PLL. A block diagram of this method is illustrated in Figure 3. The PLL comprises a phase error detector (PED), a loop filter with transfer function $F(z)$, and a direct digital synthesizer (DDS) [14]. Here, we use the blind, low signal-to-noise ratio PED. The S-curve for this PED is plotted in Figure 4. The circles indicate the stable lock points. Note that the stable lock points correspond to the rotational symmetry of the outer ring and is a common feature for blind and decision-directed PLLs [14]. This property is commonly referred to as a “phase ambiguity.”

Except for the stable lock point at 0° phase error, the PLL may lock with a static phase error. This means an additional phase rotation is required to remove the phase ambiguity prior to detection. The phase ambiguity may be resolved by differential encoding or by exploiting the presence of a known data sequence in the data. Differential encoding is used for SOQPSK-TG and is described

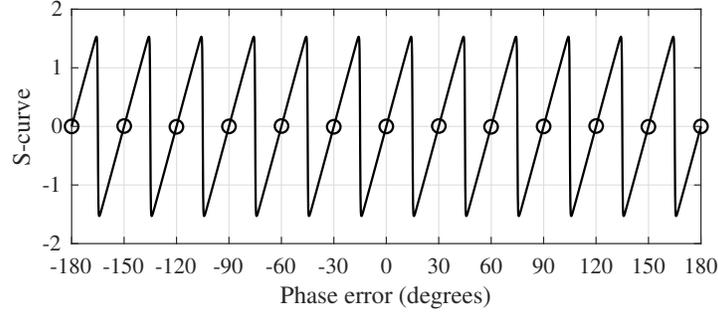


Figure 4: The S-curve for the blind, low signal-to-noise ratio PED for 16-APSK used in the simulation results. The PED gain is $K_p = 6.36$. The circles indicate the stable lock points for this PED.

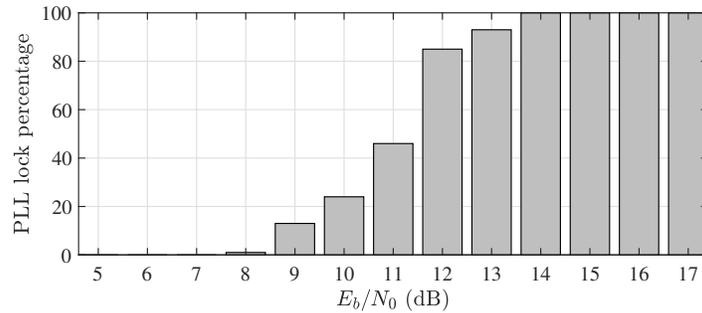


Figure 5: Lock rates for the PLL-only approach summarized in Figure 3 for a closed loop bandwidth of 0.015 cycles/symbol.

in Appendix 2-B of IRIG 106-17 [2]. Here, we leverage the periodically inserted ASM field to compute the phase ambiguity. The phase ambiguity resolution block in Figure 3 first finds the location of the ASM in the PLL output. Next, the PLL outputs corresponding to the ASM symbols are rotated by the twelve possible fixed rotations and correlated with a locally-stored copy of the ASM symbols. The maximum of the real parts of the twelve parallel correlator outputs is used to identify the phase ambiguity. The PLL outputs corresponding to the data symbols are derotated by phase ambiguity.

The challenge with the traditional PLL-based approach is the difficulty acquiring lock at low signal-to-noise ratios in the presence of a frequency offset. Simulation results, for a PLL with a proportional-plus-integrator loop filter scaled to produce a closed-loop bandwidth of 0.015 cycles/symbol, are summarized in Figure 5. The PLL is only able to consistently lock for $E_b/N_0 \geq 14$ dB. The necessity to lock at lower values of E_b/N_0 motivates examination of alternative approaches.

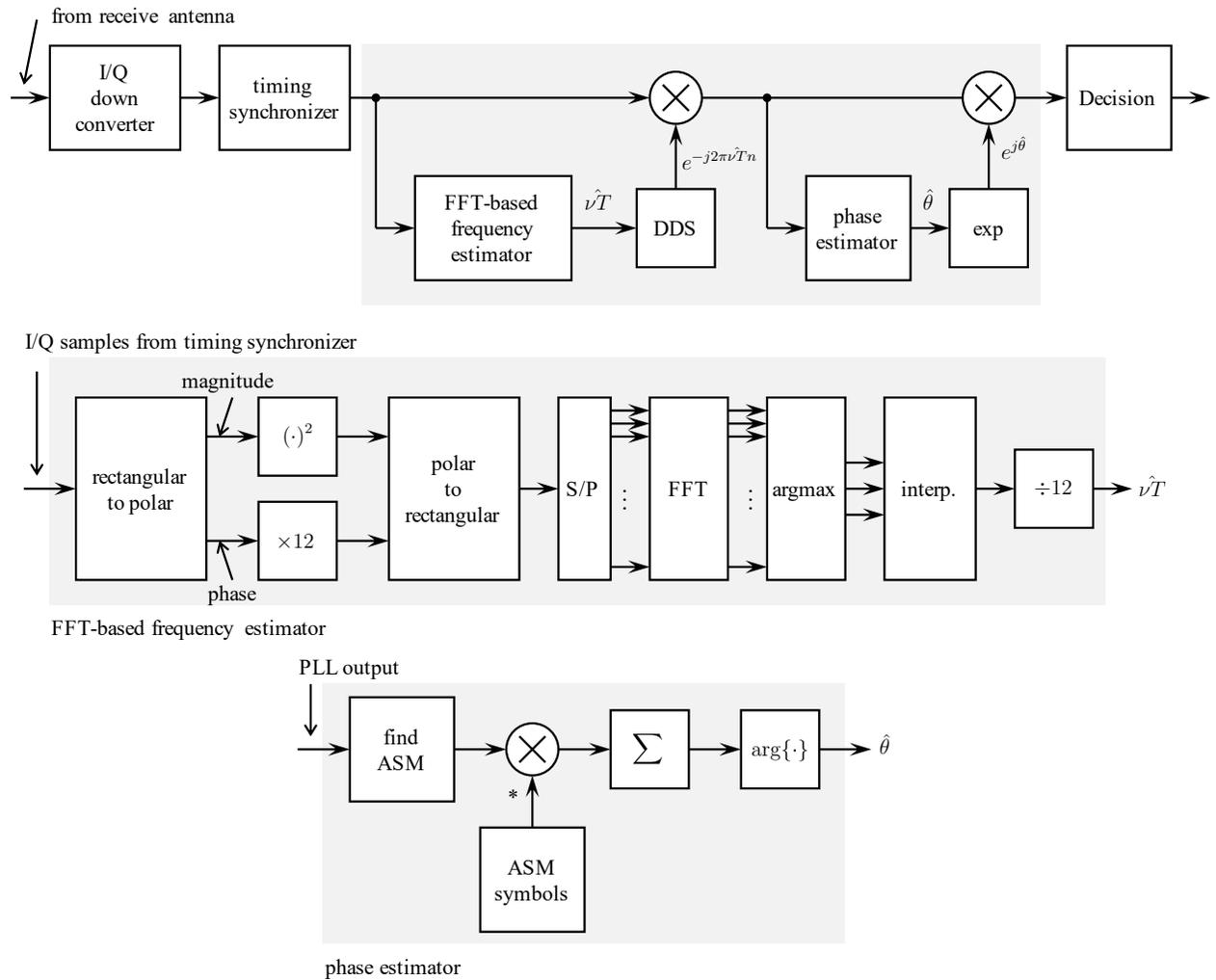


Figure 6: A block diagram summarizing the FFT-based approach.

FEEDFORWARD ESTIMATOR BASED ON THE FFT

The feedforward estimator is a blind frequency offset estimator summarized by the block diagram in Figure 6. A non-linear transformation is applied to the matched filter outputs (sampled at one sample per symbol). The transformation is designed so that a peak occurs at the frequency offset in the DTFT of the transformed sequence. To find this peak, the periodogram formed from the FFT is used. The index of the maximum of periodogram is identified and an interpolation is used to refine the frequency estimate.

The frequency offset is used to derotate the matched filter output samples. A data-aided phase estimator, based on the periodically inserted ASM, is used to estimate the residual phase offset. The phase offset estimate is used to derotate the the matched filter outputs in preparation for decisions.

The number of data symbols L_v , the length of the FFT L , and the method of interpolation are design

Table 1: Accumulated phase error at the “corner values” of E_b/N_0 for each FFT length in Figure 7.

L_v	E_b/N_0	$\Delta\theta$
256	8.75 dB	14.1°
512	7.50 dB	8.4°
1024	6.50 dB	2.5°
2048	5.50 dB	1.4°
4096	5.00 dB	0.9°
8192	4.25 dB	0.4°

parameters for this method. The performance of this method, as a function of the FFT length and the interpolation method is described in [13]. A representative example of the performance is illustrated in Figure 7. In this figure, the simple maximum of periodogram based on the length- $L = 2L_v$ FFT is used for the coarse search. Parabolic interpolation was used to refine the estimate [12]. For all FFT lengths the error variance decreases rapidly with increasing E_b/N_0 until E_b/N_0 reaches a “corner value” after which the decrease in error variance is much more modest with increasing E_b/N_0 .

One way to interpret this data is to consider the “corner value” as the lowest value of E_b/N_0 at which the estimator achieves good performance. In general, the corner value decreases as the FFT length increases. The performance of the estimator may be quantified by calculating the accumulated phase error due to the RMS frequency error. The RMS frequency error is the square-root of the estimator error variance in Figure 7. When using an erroneous frequency estimate to derotate the data, phase error accumulates until it is corrected by the phase offset estimated from the ASM. The accumulated phase error is given by

$$\Delta\theta = f_{\text{RMS}} \times L_d \times 360^\circ, \quad (1)$$

where f_{RMS} is the RMS frequency error and $L_d = 6144/4 = 1536$ symbols is the number of symbols between each occurrence of the ASM. The accumulated phase error for each FFT length at the “corner value” of E_b/N_0 is summarized in Table 1. Above their corner values of E_b/N_0 the estimators for $L_v \geq 512$ are able to achieve sufficiently good performance. The desire to operate at $E_b/N_0 \geq 6$ dB suggests that L_v must be 2048 or higher. The simulation results presented below show that $L_v = 1024$ also achieves good performance at $E_b/N_0 = 6$ dB. This fact demonstrates that caution should be exercised when using the data in Figure 7 at values of E_b/N_0 just slightly below the “corner value” of E_b/N_0 : the performance curves are very steep and small statistical variations can produce huge changes in performance.

The acquisition time for the feedforward estimator described in this section is L_v , the number of symbols required to produce the frequency estimate. Could a properly initialized PLL produce possess a shorter lock time?

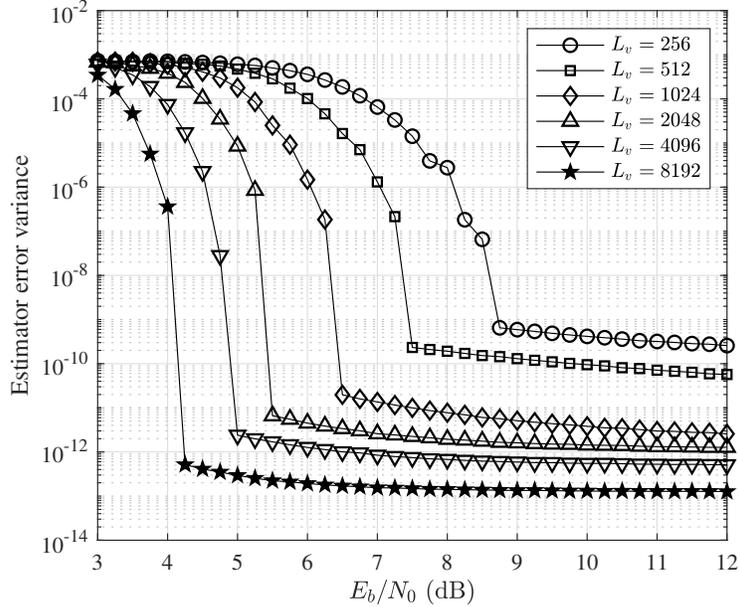


Figure 7: Estimator error variance vs. E_b/N_0 as a function of FFT length.

A FEEDFORWARD-INITIALIZED PLL

The two approaches described in the previous two sections may be combined to produce a “hybrid” approach. The blind FFT-based estimator is used to produce a frequency offset estimate that is used to initialize the PLL. With this initialization, PLL acquisition starts in frequency lock (or close to frequency lock) and only needs to acquire phase lock. Phase lock is relatively easy to achieve, even at low values of E_b/N_0 , as long as a low signal-to-noise ratio PED and the proportional-plus-integrator loop filter are used.

A block diagram summarizing this approach is outlined in Figure 8. The PLL elements are the same as those in Figure 3 and the FFT-based frequency estimator is identical to that in Figure 6. Note that the initialization method used here sets the initial condition of the integrator portion of the loop filter to the frequency offset estimate. When in lock, the phase ambiguity predicted by the S-curve in Figure 4, is still an issue and needs to be corrected. The phase ambiguity resolution block is identical to the one outlined in Figure 3.

The mean-squared error of the frequency estimate, for various values of closed loop bandwidth $B_n T_s$ and initialization length L_v , is summarized in Figure 9. The performance curves are similar to those of the FFT-based feedforward estimator in Figure 7: two distinct regions are observable, the first with an error variance approximately 10^{-3} at lower values of E_b/N_0 , and the second with a much lower error variance at higher values of E_b/N_0 . A transition region connects the two. The transition region is characterized by a steep decrease in the error variance with increasing E_b/N_0 until a “corner value” of E_b/N_0 is reached. As in Figure 7, the “corner value” of E_b/N_0 decreases with increasing L_v . Unlike Figure 7, the error variance floor is determined by $B_n T_s$, not by L_v .

The estimator error variance achieved by the PLL in Figure 9 is much higher than the estima-

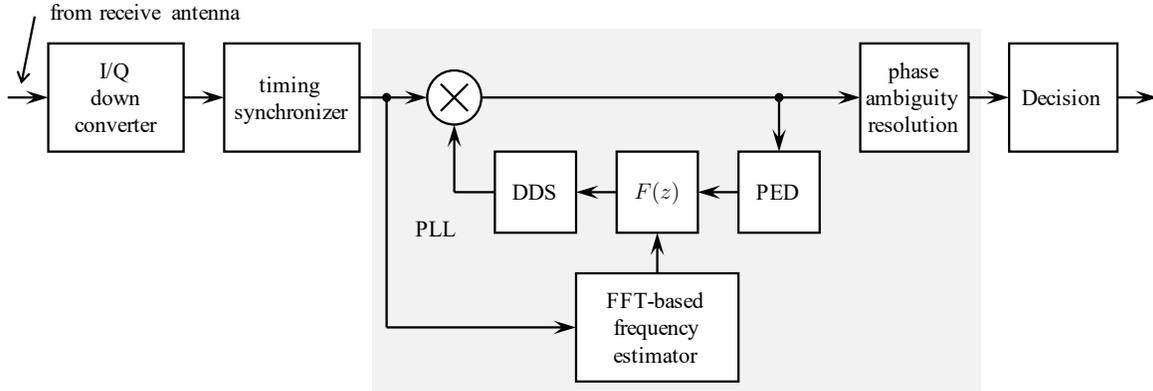


Figure 8: A block diagram summarizing the hybrid PLL+FFT-based approach.

tor error variance achieved by the feedforward estimator in Figure 7. The feedforward estimate must be very accurate because the system has no way of tracking phase error accumulation due to errors in the frequency offset estimate. In contrast, the PLL-based approach tracks errors in the instantaneous phase and can be more robust to errors in the initial frequency offset estimate. For this reason, comparing the frequency offset error variance does not produce a fair comparison. Bit error rate (BER) is the ultimate figure of merit; BER comparisons are performed in the next section.

Our experience is that the PLL sometimes has difficulty maintaining lock after the initialization. Simulation results tracking the lock status of the PLL are presented in Figure 10. Here, initializations formed from $L_v = 1024$ symbols and $L_v = 2048$ symbols are shown. For each value of L_v , the results for different values of $B_n T_s$ are more similar than they are different. This suggests that the closed-loop bandwidth is not the dominant factor in maintaining lock. The dominant factors are the quality of initial estimate and the signal-to-noise ratio. For $E_b/N_0 \geq 7$ dB, the PLLs maintain lock for both values of L_v . For $E_b/N_0 = 6$ dB, the results suggest $L_v \geq 2048$ is required.

COMPARISON

In the previous two sections, the frequency estimator error variance for the two synchronizers was computed. It was pointed out that the comparison is not entirely fair because the PLL, which tracks the instantaneous phase error, is able to track small frequency offsets. Consequently, PLL frequency estimate does not need to be as refined as the frequency estimate in a feed-forward system. Here, the bit error rate (BER) is used to compare the two approaches. The simulated BER is summarized by the plots in Figure 11. Observations:

- The BER performance of the FFT-based synchronizer outlined in Figure 6 is shown in the top left plot of Figure 11. For the values of E_b/N_0 used in the simulations, the FFT-based approach achieves ideal performance for $L_v \geq 2048$. For $L_v = 1024$, the FFT-based approach achieves ideal performance only for $E_b/N_0 \geq 6$ dB.

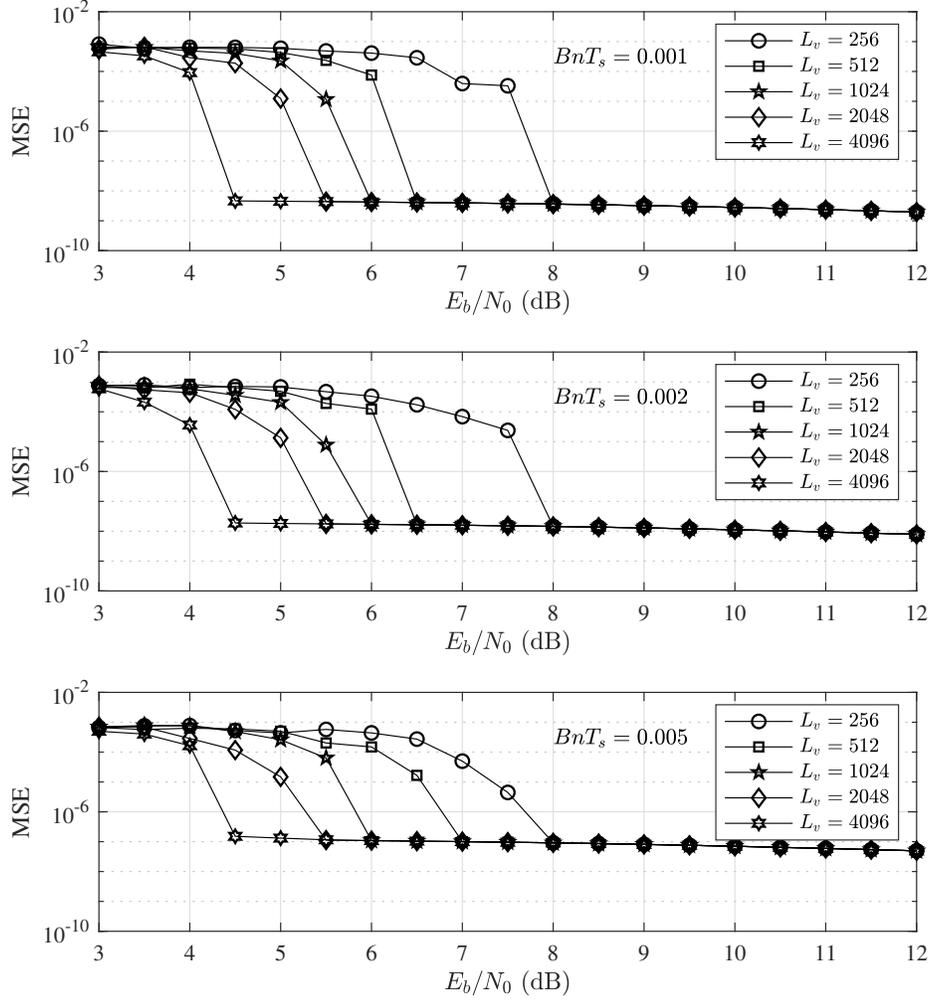


Figure 9: Estimation error variance for the frequency estimate of the feedforward-initialized PLL: (top) for $B_n T_s = 0.001$ cycles/symbol; (middle) for $B_n T_s = 0.002$ cycles/symbol; (bottom) for $B_n T_s = 0.005$ cycles/symbol;

- The BER performance of the FFT-initialized PLL approach outlined in Figure 8 is summarized by the other three plots in Figure 11, each for a different value for the closed-loop bandwidth. For $B_n T_s = 0.001$ and 0.002 cycles/symbol, the PLL initialized with an FFT-based estimate using $L_v = 2048$ samples achieves ideal performance for all values of E_b/N_0 used in the simulations. When the PLL is initialized with an estimate based on the FFT-based estimator using $L_v = 1024$, ideal performance is achieved only for $E_b/N_0 \geq 6$ dB. Increasing the closed-loop bandwidth to $B_n T_s = 0.005$ cycles/symbol does not improve performance.
- The values of E_b/N_0 on the x-axis correspond to the “over-the-air” signal-to-noise ratio. The equivalent uncoded E_b/N_0 can only be calculated once the code rate is known.

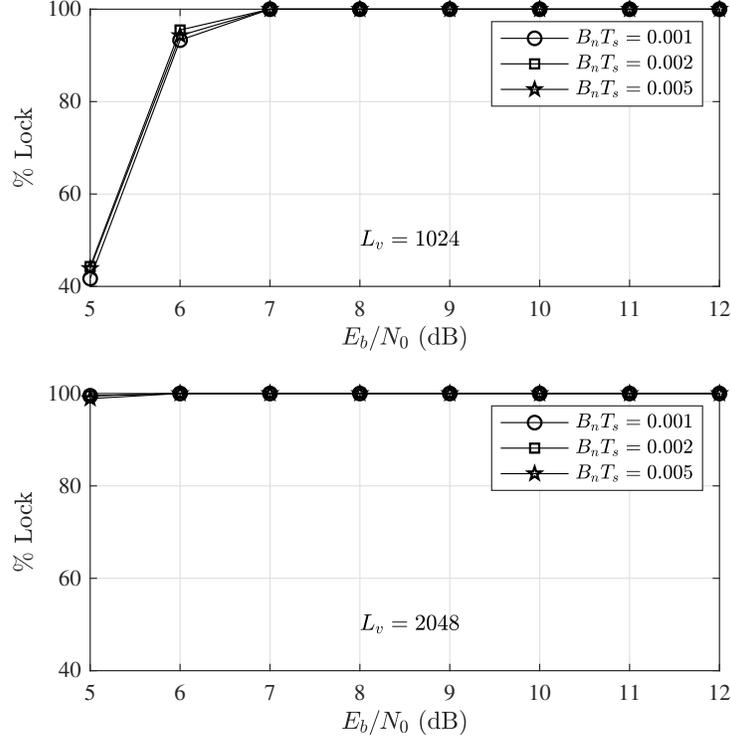


Figure 10: The percentage of time the PLL maintains lock after initialization: (top) for $L_v = 1024$ symbols; (bottom) for $L_v = 2048$ symbols.

CONCLUSIONS

In this paper, we have considered the problem of carrier phase and frequency estimation for coded 16-APSK in aeronautical mobile telemetry. Given the fact that coded systems tend to operate at lower signal-to-noise ratios than uncoded systems, the synchronizer must operate at these lower signal-to-noise ratios. For a 30 kHz frequency offset and a 10 Mbit/s 16-APSK signal, the conventional phase lock loop (PLL) system does not achieve consistent lock to be a useful alternative. Consequently, a blind feed-forward approach, based on the FFT, and an initialized feedback approach based on the PLL were examined.

The feed-forward estimator, based on the FFT, is summarized in Figure 6. This estimator is capable of achieving BER ideal performance for $E_b/N_0 \geq 6$ dB using 1024 symbols. (Increasing the number of symbols to 2048 extends the operating range to 5 dB.) The feedback estimator is based on a PLL initialized by a feed-forward estimate derived from the same FFT-based algorithm. This algorithm is capable of achieving ideal BER performance for $E_b/N_0 \geq 6$ dB using 1024 symbols. (Increasing the number of symbols to 2048 extends the operating range to 5 dB.) The performance of both approaches depends on the accuracy of the feed-forward estimate. An estimate based on 1024 or more symbols appears to be adequate.

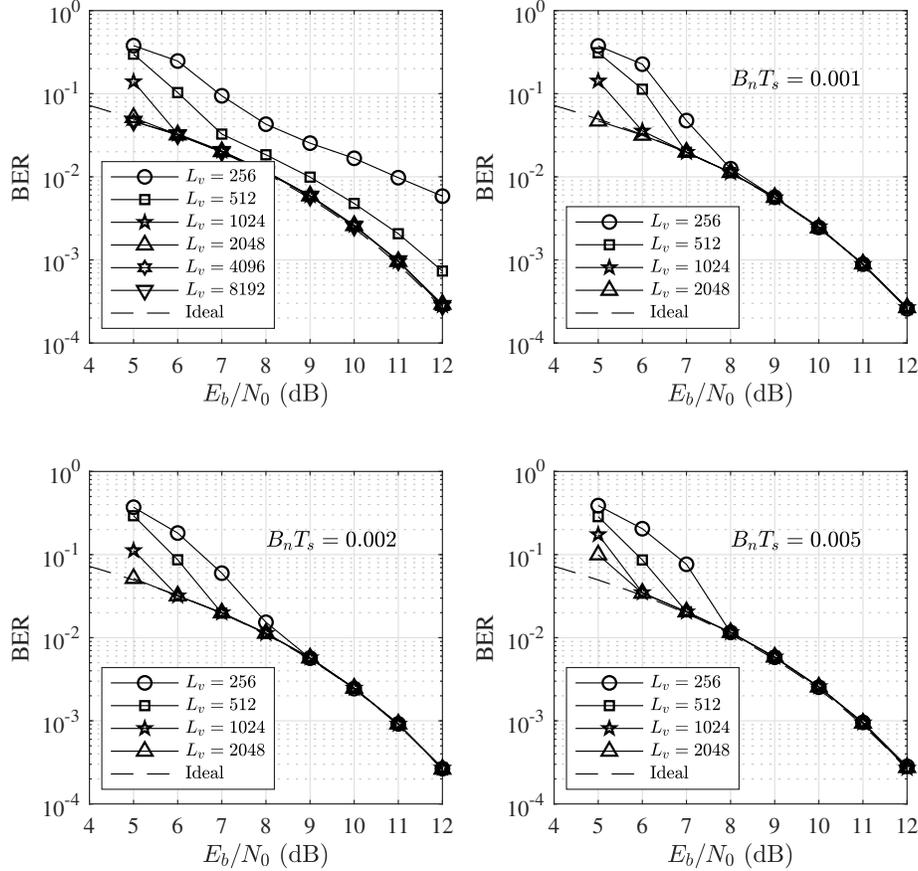


Figure 11: Simulated BER performance: (top left) the FFT-based approach; (top right) the FFT-initialized PLL approach with $B_n T_s = 0.001$ cycles/symbol; (bottom left) the FFT-initialized PLL approach with $B_n T_s = 0.002$ cycles/symbol; (bottom right) the FFT-initialized PLL approach with $B_n T_s = 0.005$ cycles/symbol.

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