Novel 8-inch wafer scale process for low-cost production of back side illuminated (BSI) imaging sensors

Joshi, Atul, Chiaverini, David, Kashyap, Sachin, Madhugiri, Vishwanath, Patti, Robert, et al.

Atul Joshi, David J. Chiaverini, Sachin Kashyap, Vishwanath Madhugiri, Robert Patti, Sangki Hong, Michael Lesser, "Novel 8-inch wafer scale process for low-cost production of back side illuminated (BSI) imaging sensors," Proc. SPIE 11723, Image Sensing Technologies: Materials, Devices, Systems, and Applications VIII, 1172308 (12 April 2021); doi: 10.1117/12.2588181

Event: SPIE Defense + Commercial Sensing, 2021, Online Only

Novel 8-inch wafer scale process for low-cost production of back side illuminated (BSI) imaging sensors

Atul Joshi[1a], David J. Chiaverini[a], Sachin Kashyap[a], Vishwanath Madhugiri[a], Robert Patti[b], Sangki Hong[b], Michael Lesser[c]

[a]SAAZ Micro Inc, 2545 W Hillcrest Dr, Thousand Oaks, CA 91320, USA; [b]NHanced Semiconductors, 1415 Bond Street Suite 155,Naperville, IL 60563, USA; [c]University of Arizona Steward Observatory, 325 S. Euclid Ave, Suite 117,Tucson, AZ 85721, USA

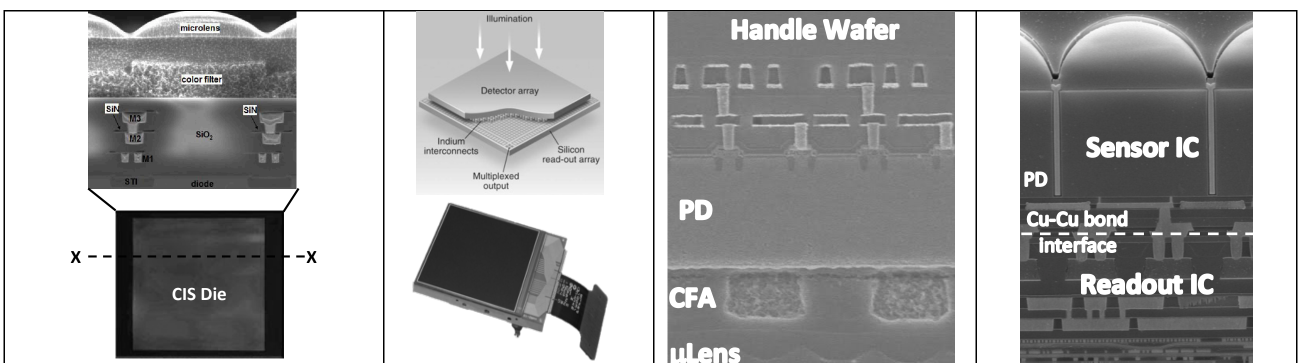
ABSTRACT

An 8-inch wafer scale process was developed that provides low-cost availability of back side illuminated (BSI) imaging sensors. The process has been optimized to convert standard CMOS and CCD 6-inch or 8-inch wafers from front side illuminated (FSI) sensors to BSI sensors. The process successfully demonstrates wafer planarization, bow correction, bonding to carrier wafers, wafer thinning, re-planarization, anti-reflection coating, through silicon vias (TSVs) and back side metallization. Good wafer thinning control was obtained for a wide range of epi thicknesses varying from less than 4 microns to 15 microns. The thinner epi is optimized for UV and visible sensing while the thicker epi material is optimized for near-infrared (NIR) sensing. The processed wafers demonstrate backside passivation and anti-reflection (AR) coatings that optimize the QE performance in a variety of bands such as 200nm-300nm, 300nm-400nm and 400nm-900nm.

Keywords: back side illumination (BSI), CMOS image sensor (CIS), CCD image sensor, UV, NIR, silicon wafer process, wafer bonding, Planarization, wafer thinning, Front side illumination (FSI)

INTRODUCTION

CMOS and CCD sensors were traditionally fabricated as front side illuminated (FSI) sensors as the FSI fabrication process were readily available in silicon foundries but BSI involved several additional complex steps. Over two decades from 1990s to 2000s these sensors dramatically improved in performance such as in array size, pixel densities, readout rate and noise performance[1]. Because the light path in such sensors had to encounter several interfaces such as a tall metal layer stack in the case of CIS and polysilicon gates in the case of CCDs (figure 1-a), these sensors could not achieve the theoretic limits of silicon photodiode quantum efficiency (QE) and optical crosstalk.



(a) FSI imager	(b) Die level BSI	(c) Wafer scale BSI	(d) 3D stacked BSI

Figure 1. Progression from FSI to BSI imaging

[1] Communication: atul@saaztechnology.com

Image Sensing Technologies: Materials, Devices, Systems, and Applications VIII, edited by Nibir K. Dhar, Achyut K. Dutta, Sachidananda R. Babu, Proc. of SPIE Vol. 11723, 1172308

As price was not a barrier for scientific imagers, die level BSI processes were developed[2] to improve their optical performance (figure 1-b). There were two process variants, namely the front side of the detector die bonded to the front side of a readout IC (ROIC), known as a hybrid, or the front side of the sensor die (CMOS or CCD) bonded to a fan out substrate. In the case of hybrid BSI, the detector wafer was optimized for imaging performance independent of the constraints imposed by the silicon process used for the readout IC. As the detection layer in this approach is decoupled form readout this approach allows heterogenous material integration, thus the approach is routinely used for manufacturing infrared sensors by bonding II-VI or III-V detection materials to silicon readout chips. In the hybrid approach indium bumps are deposited on each pixel of the wafers and then the detector wafer as well as the readout wafer are diced to hybridize individual die. Similar processes are used if the die is bonded to a fan out substrate instead of a ROIC as is routinely done for scientific CCDs. Once bonded the backside substrate is removed from the detector and then the back side is passivated as well as anti-reflection coated. The substrate or the ROIC that the detector is bonded to have a larger dimension than the detector die dimension so that the ROIC or the substrate footprint outside the detector area can be used for wire bonding. Even though this die level process is expensive, it has been employed for high performance silicon imagers as well as for infrared imagers.

In the last decade lower cost wafer scale BSI processes have been developed by some of the CMOS and CCD foundries[3]. These processes involve bonding the detector wafer to a handle wafer (figure 1-c), then removing the back side substrate to passivate, AR coat, and optionally deposit color filters as well as micro-lenses. To access the wire bond pads the silicon epi layer as well as inter layer dielectric are etched to expose the wire bond pads from the back side. Another variant of the wafer scale processes has been recently developed to bond the detector wafer to a ROIC instead of a passive substrate[4] (figure 1-d). Separating the readout from the detector allows to independently optimize the imaging performance of the detector layer as well as the digitization and processing performance of the ROIC layer.

It is surprising that even with continued global advancement of wafer scale BSI technology these processes are not readily available for scientific and defense sensor use. As mobile phones provide the largest volume to manufacturers these processes are specially geared towards developing sensors optimized for consumer mobile use. Semiconductor fabs' key focus area is shrinking the pixel size. Technological advances such as deep trench isolation (DTI) and capacitive deep trench isolation (CDTI) have made it possible for pixels to be shrunk to less than a micron with visible QE as well as NIR QE approaching that of scientific sensors. Such advanced hybrid stacked BSI processes are only offered in the newest CIS process nodes. These nodes are not suitable for scientific sensor use as they 1) have very high mask costs which is a deterrent for low volume applications, 2) limit the pixel size to less than 3-5 micron due to lateral charge transfer or micro-lens limitations, 3) do not have custom micro-lenses or custom AR coating available, 4) do not allow back side bias, 5) do not allow very thick or very thin epi, and 6) do not allow tweaking process parameters. For CCDs the situation is even worse as it is even hard to find a reliable foundry partner and any BSI options are held by captive fabs that compete in the end product market.

As legacy FSI sensor processes are readily available for scientific use with no real flexible scientific BSI options at those commercial foundries, the scientific community has worked on creating some solutions. The most notable efforts have been by the University of Arizona Imaging Technology Laboratory's (ITL) developing the chemisorption process[5] and JP developing the delta doping method[6]. Other entities have also developed some commercial implant and anneal techniques. However, such processes have not been optimized for a variety of bands using a variety of substrates with varying epi thicknesses and wafer sizes, such as 6", 8" and 12" wafers. The objective of this research is to develop a single window capability for providing foundry services for a variety of scientific sensor needs. The following wide variety of capabilities are in development:

- A variety of spectral bands such as UV-A, UV-B, blue enhanced visible, visible, NIR and broadband response
    - Specialized epi thicknesses suitable for each band
    - Specialize passivation
    - Specialized AR coating suitable for the bands
- Handling all commercial starting wafer sizes including 6", 8" and 12"
- Allowing detector wafer bonding to handle wafer or stacking with a ROIC wafer to create a 3D hybrid
- Providing other options such as back optical side shield, MTF enhancement grids and backside contacts

The process involves starting with easily available frontside illuminated imaging devices (FSI CMOS or FSI CCD), and enabling the processes to turn the devices into backside illuminated devices (BSI CMOS or BSI CCD). It is highly desirable to provide batch processing to lower cost and reduce process time. To enable this technology, it is required to employ 3D wafer bonding, precise epi thinning for improved UV performance, specialized anti reflection coatings, and reduction of surface states which is critical for near UV performance.

UV-A and UV-B require special backside processing to counteract backside surface charge. All spectral bands require antireflection coatings (ARC) to optimize the required pass band QE, light masking, and a means of contacting the frontside bond pads from the backside. Note that some backside illuminated imagers use the frontside pads from the frontside, but access from the backside enables easier packaging. For cost reasons, wafer lot level processing is highly desired. Each requirement is addressed by this project.

The back-illuminated sensors must be relatively thin for photogenerated electrons to diffuse to the frontside pixel wells and be collected under the sites where they were created. Most sensors are built on epitaxial silicon, with layers which are 5um–20μm thick. The substrate must be backside etched down to this thickness range, so that the photogenerated electrons are created in this high-quality epitaxial layer. In the case of UV bands, the thickness needs to be of the order of only 2-um to 4-um to optimize the response.

Starting wafers for this project were processed at a commercial foundry, employing a front side illumination. This project started with eight-inch wafers cored to 6 inches while the full backside 8-inch processing capability was developed in parallel. Due to this project, eight-inch wafer backside illuminated image sensor processing is now fully enabled and twelve-inch wafers can also be cored to run through the process. In future complete twelve-inch processing can be available.

1. Backside processing methodology

The backside process comprises: 1) incoming wafer inspection, 2) surface preparation, 3) carrier wafer bonding, 4) wafer backside thinning, 5) backside surface passivation and anti-reflection coating, and 6) Backside metallization and pad opening. The following sections detail these process steps.

2. Wafer Preparation

Typical cross-section of the starting martial is depicted by figure 2.

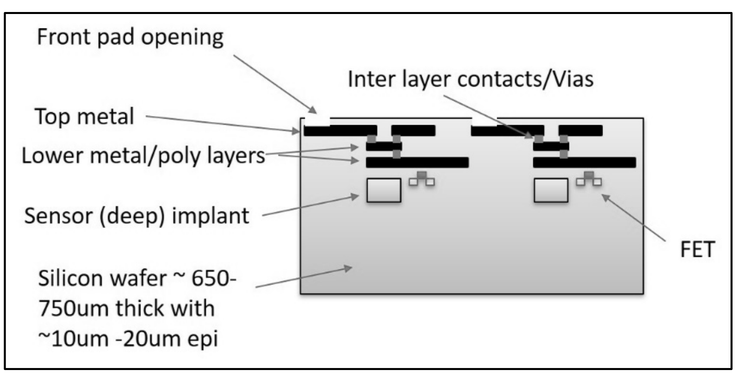


Figure 2. Typical starting front side illuminated wafer. Wafers may employ either buried channel CCD or pinned photodiode.

Front side imager wafers are received and inspected for bowing and bond surface topology. Specifications for bowing are 30um upward bow (u shaped) and 10um downward bow, measured relative to appropriate side (note that when bonding wafers, the same wafer could be plus or minus bow, depending on bonding surface, since bonding surface is circuit side, that is the relevant surface for this project, and in this case the bow must be less than 30um for eight-inch wafers, but is more relaxed for six-inch wafers). After bowing correction, if any, the wafers are inspected for surface smoothness. Surface smoothness specification is <5nm variation over any 200um scan, and <0.5um over any 10mm-by-10mm area. Incoming wafer surface roughness as high as 4um was successfully handled. A custom process was devised to attain the specified topology for wafers with high roughness. The developed process is quite robust as it can handle non-planar wafers.

wafer ID (Lot-B-1)		6-inch wf Bow (µm)		Topology (µm)
		0°	90°	
Run-3	**14**	10.5	22.4	3.92
Run-3	**16**	19.8	25.2	4.17
Run-3	**17**	23.5	17.3	4.01
Run-3	**18**	9.9	15.3	4.06
Run-4	**17**	35.3	14.9	4.81
Run-5	**19**	3.9	13.3	4.07

Figure 3. A sample of incoming wafer bow and surface topology is shown.

Bow is measured in two directions (Figure 3), both through the center of the wafer and perpendicular to each other. The surface topology of legacy processes can be quite poor (figure 4) as they are not designed for wafer bonding. A process was developed for extensive surface topology correction. Bow correction was not needed for the six-inch wafers. If Run-4 wafer 17 was an eight-inch wafer it would have required bow correction.

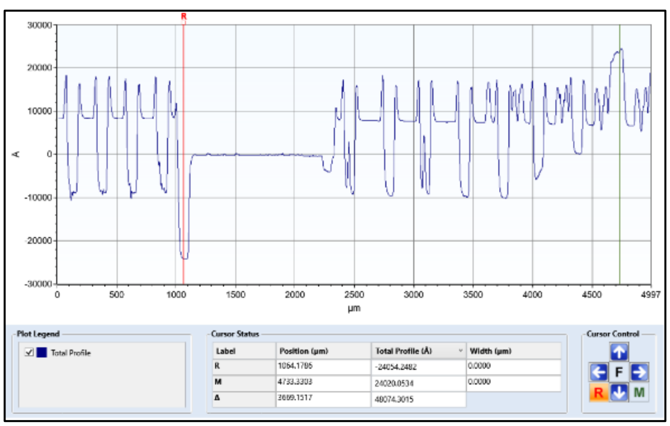


Figure 4. Incoming wafer shown has 4.81um peak to peak surface topology over a distance of 5mm

Once the surface is smoothened, only 30nm topology is observed over a 5mm distance *(Figure 5)*. The surface topology is negligible over short distances.

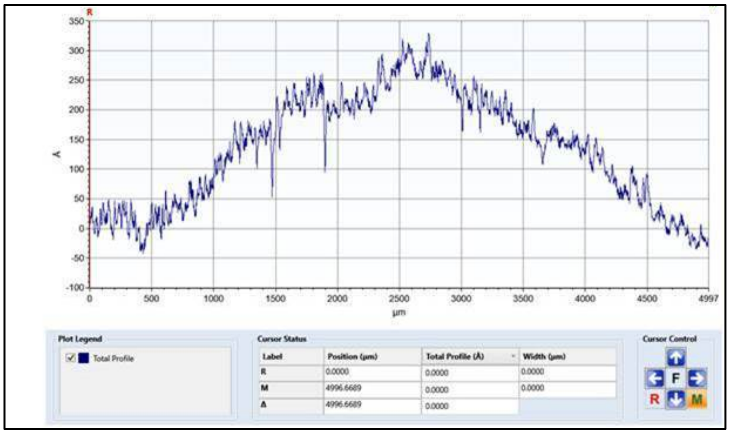


Figure 5. Surface topology after smoothening (vertical scale in angstroms)

3. Wafer Bonding

After coring, bow correction, and front surface topology correction the imager circuit wafers were DBI® bonded to handle-wafers and thinned. Figure 6. depicts wafer pair after bonding. Wafer surface preparation, including bow correction and planarization are key to achieving success with the Direct Bond Interface (DBI®) method

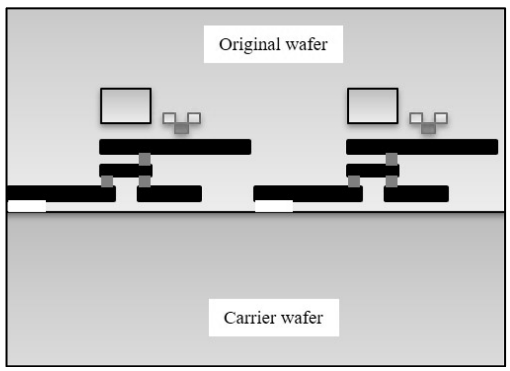


Figure 6. Wafer Pair After Bonding.

Figure 7 shows the cored wafer side by side with the eight-inch wafer. The center of the cored wafer is maintained to allow easy identification of the die. Though the cored wafer appears quite smooth, a close examination of the wafer reveals a rather jagged edge. This results in some bonding and polishing problems but does not significantly impact the goal of this project.

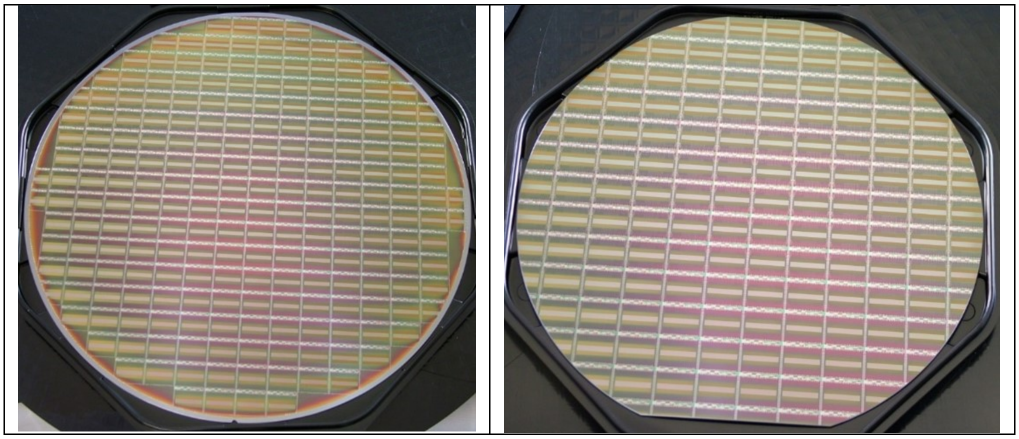


Figure 7. Before and after coring of 8in wafer. Center of wafer not changed by coring.

Figure 8 shows the bonded wafers, before thinning. The white areas revealed by C-SAM imaging indicate bond defects. These are mostly due to wafer edge defects due to coring, and do not impact a significant portion of the die. Edge problems are much less prevalent in non-cored wafers. Additionally, various edge grinding, and polishing steps are available if cored wafers are required (e.g. due to handling and test restrictions).
If significant bonding issues are present (e.g., large bond defect away from edges), the wafers may be separated and reworked before final annealing but are permanently bonded thereafter.

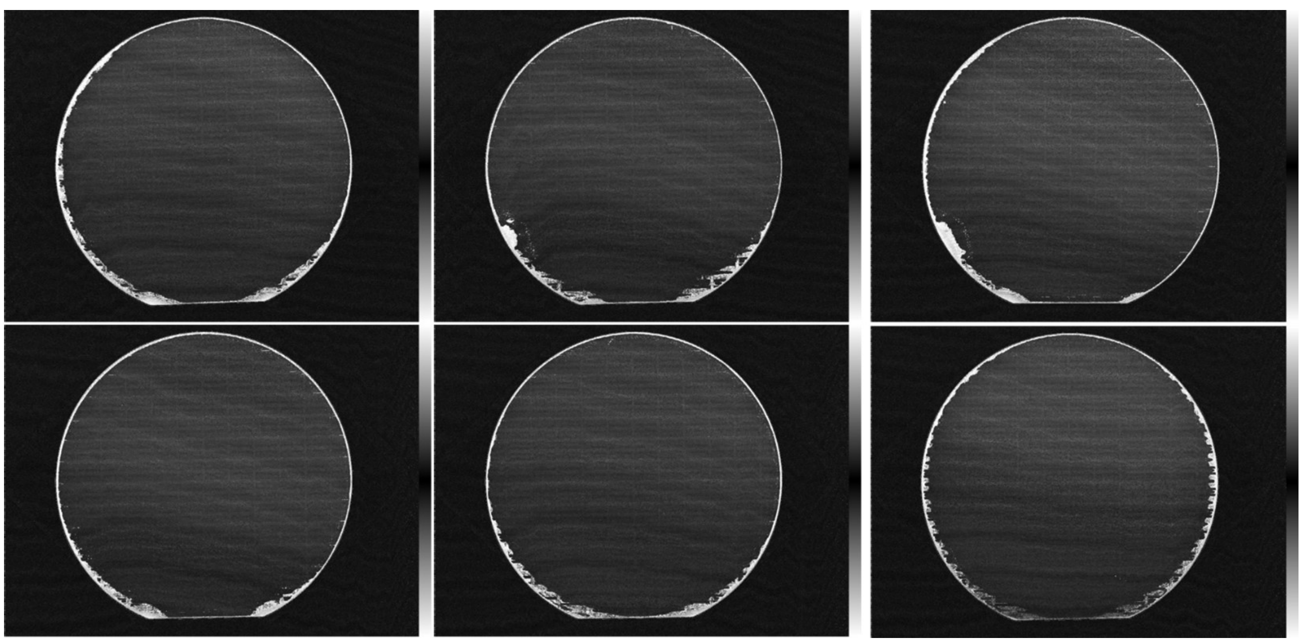


Figure 8. Permanently bonded sensor wafer to carrier wafers, before thinning. The white areas indicate bonding defects. These are mostly due to coring and do not affect a significant portion of the die.

4. Backside Thinning

Thinning of wafers to about 250um is performed by wafer lapping. Thinning the wafer to ~20um epi uses wafer grinding. Near final epi thickness is obtained by CMP to the epi layer using the epi gradient as a selective etch stop. The final epi thickness is obtained by iterative CMP and measurement. Initial epi for this project was 14.5 um to 16.5um. UV-A and

UV-B epi thickness after thinning is targeted for 4um. NIR epi thickness after CMP is targeted for 14um. Figure 9 shows how the bonded thin wafer appears.

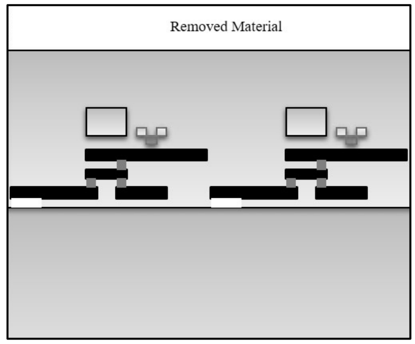


Figure 9. Bonded thinned wafer

The thinned wafers are shown in figure 10, looking from the backside of the sensor. The mirror polished surface has surface roughness ≤ 4 Å. Wafer bow after thinning was quite high (~130um) convex (positive). Changes in bow are expected due to thinning the wafer, which changes the stress. Though the bow values seem quite high, they did not interfere with backside mask exposure and etch. The difference in appearance between the 14um epi and 4um epi is evident. Slight variations in the 4um epi result in areas where the epi is transparent, especially near the edges, where it was reported that the polishing rate was somewhat higher than towards the middle. Again, some of this is due to the cored wafer. Future runs of eight-inch wafers will be less susceptible to this issue. As expected, the 14um epi is opaque to visible light.

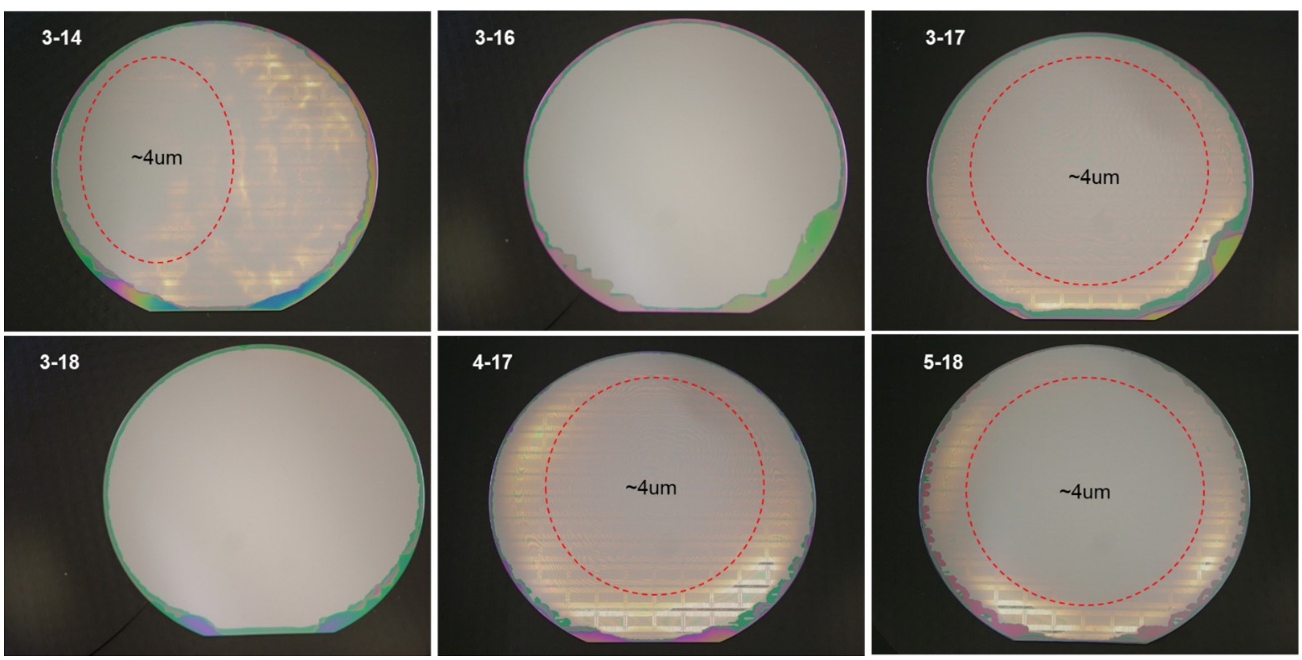


Figure 10. Polished thinned wafers seen from the backside of the image sensor wafer. The circled areas show the estimate of the 4um region. The remaining two wafers, 3-16 and 3-18, are thinned to 14um epi.

5. Backside Surface Preparation and Anti-Reflection Coating

A backside charging process is critical to achieve low dark current and high QE, especially for UV devices. ITL's chemisorption process has resulted in improved absolute quantum efficiency (QE), good QE stability with temperature and environmental contamination, and enhanced near-IR response on CCD and CMOS imagers[5]. This process was applied to sensors on a wafer scale for this project, including the new enhancement for oxidation of eight-inch CMOS wafers.

Figure 11 shows the low temperature thermal oxide followed by chemabsorb process (dashed line). This is followed by anti-reflection coating (darker color layer above the dashed line).

This process requires a high-quality oxide to be grown on the silicon backside. Because low temperature, high quality thin oxide growth process is not commercially available, this project developed the capability to grow oxides on 8-inch wafers. Previously only stitched die could be processed. The development started with processing full 6-inch wafers that was later scaled to full 8-inch wafers. Thin film ARC was custom designed for each band are applied after the oxide growth.

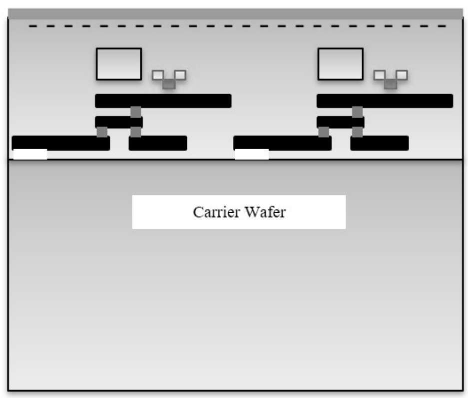


Figure 11. Wafer after Low Temperature Thermal Oxide, Chemabsorb and Anti Reflection Coating

One of the most significant quantum efficiency losses of back illuminated image sensors is reflection off their back surface. The thinning process creates a mirror-like finish with an extremely high specular reflectivity. This reflection loss approaches 60% in the UV. The application of a thin film antireflection (AR) coating directly onto the image sensor back surface can therefore significantly increase QE. Figure shows the result of the UVA (300A to 400A) anti reflecting coating for a witness sample accompanying the wafer. Reflectance averages less than 15% across the band (Figure 12). The UVB and NIR bands show similar improvements relative to non-coated wafers. Final QE assessment, determined by optical characterization, is planned to be presented in a subsequent publication.

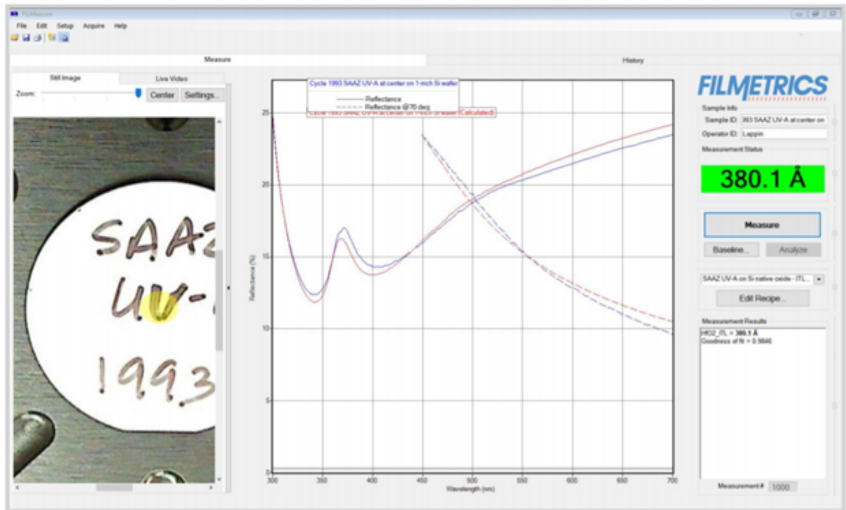


Figure 12. UV-A Band: 300nm to 400nm. The data is measured for a one-inch diameter silicon sample disk placed near the wafers being coated. The red is calculated, and blue is measured on the sample wafer. The dashed lines refer to 70-degree angle calculation and measurement.

6. Backside Metal and Pad Opening

After thin film ARC wafers get backside aluminum metallization and patterning. Finally, front side pads are accessed from back side. This final backside process consists of depositing an aluminum light barrier, then exposing and etching away the active pixel area and frontside pad areas. After metal etch, the pads are opened by etching ARC over the pad openings, followed by a silicon etch, and then a final oxide etch up to the frontside aluminum pads (metal 1 for these die). Wafer with backside metallized and patterned, and finally front side pads accessed from back side oxide etch is depicted in figure 13. The initial backside metal coating consisted of a very thin layer of titanium (for superior adhesion), follow by a half um of aluminum. If an ARC is used that is not compatible with titanium etch an alternate process can be used. This process consisted of a thinner aluminum layer (0.2 microns) which has been proven to provide a quality light barrier with good adhesion to the backside surface.

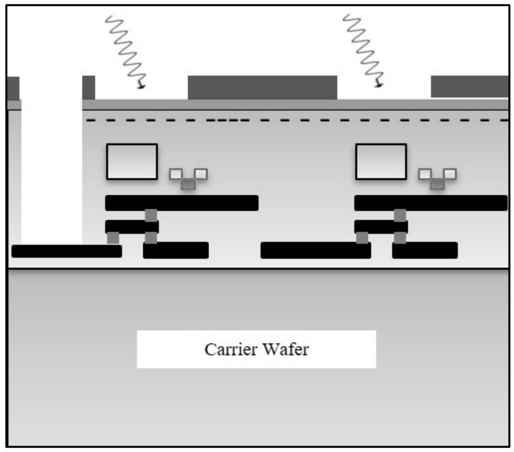


Figure 13. Wafer after back metal, optical area opening, and frontside pad opening

Care must be taken to provide sufficient metal 1 overlap of the pad opening due to some expansion of the drawn dimensions during etch. Measurements showing low metal pad resistance and non-degradation of diode protection, were made by micro probing the frontside pads from the backside. Detailed image sensor functionality characterizations of the backside devices compared to frontside results are in progress and will be reported on in a subsequent paper.

Figure 14. Backside aluminum, Exposed ARC, and Pad Opening

In figure 14 the deposited aluminum is light brown while dark brown regions are exposed ARC. Front side double bond pads are shown, with one of each pad pair numbered from the front side with polysilicon. (The topology on the front side allows the numbers to be visible, when looking at the original wafers.)

7. Conclusion

A process has been development for wafer scale BSI processing of commercially supplied FSI wafers. The process successfully demonstrates wafer planarization, bow correction, bonding to carrier wafers, wafer thinning, re-planarization, anti-reflection coating, through silicon vias (TSVs) and back side metallization. This project shows that FSI devices can be converted to superior performing backside illuminated devices using a wafer lot process suitable for production. Lot size of three wafers can be proceed thru each major step, including surface preparation, wafer bonding, backside thinning, backside surface state compensation, antireflection coating, and backside light shield deposition and pad opening. Starting with die level capability the critical steps of low temperature thermal oxidation and chem absorb process were upgraded to handle six-inch wafers and subsequently eight-inch wafers. Additionally, very thin epi thickness was demonstrated, empowering the development of high-performance UV devices. Thicker epi was processed for NIR enhanced imaging. Detailed electrical and optical performance measurements are planned to be reported in a subsequent publication.

8. References

[1] A. Joshi, D. Chiaverini, K. Jung, V. Douence, G. Wijeratne, G. Williams and M. Loose, "Scalable Architecture for Video-Rate CMOS Imaging System on a Chip", Proceedings from IEEE International Workshop on CCD and AIS, June 9-11 2005, Nagano, Japan.

[2] Yibin Bai, Jagmohan Bajaj, James W. Beletic, Mark C. Farris, Atul Joshi, Stefan Lauxtermann, Anders Petersen, George Williams, "silicon CMOS imaging technologies for x-ray, UV, visible, and near infrared", Proceedings Volume 7021, High Energy, Optical, and Infrared Detectors for Astronomy III; 702102 (2008) https://doi.org/10.1117/12.792316, SPIE Astronomical Telescopes + Instrumentation, 2008, Marseille, France

[3] Chipworks report, "8MP Omnivision BSI sensor"

[4] System Plus Consulting Report, "Apple IpAD Pro LiDAR Module structure, process & cost report"

[5] Michael P. Lesser, Venkatraman Iyer "'Enhancing back-illuminated performance of astronomical CCDs", Proceedings Volume 3355, Optical Astronomical Instrumentation; (1998) https://doi.org/10.1117/12.316776
Event: Astronomical Telescopes and Instrumentation, 1998, Kona, HI, United States

[6] M.E. Hoenk, P.J. Grunthaner, F.J. Grunthaner, M. Fattahi, H.-F. Tseng and R.W. Terhune, "Growth of a Delta Doped Silicon Layer By Molecular-Beam Epitaxy On a Charge-Coupled Device For Reflection-Limited Ultraviolet Quantum Efficiency," Appl. Phys. Lett., 61: 1084 (1992).