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Maria Ruiz-Gonzalez, Robert G. Richards, Kimberly J. Doty, Phillip H. Kuo, Matthew A. Kupinski, Lars R. Furenlid, Michael A. King, "A read-out strategy for high-resolution large-area SiPM-based modular gamma-ray cameras," Proc. SPIE 12031, Medical Imaging 2022: Physics of Medical Imaging, 120314K (4 April 2022); doi: 10.1117/12.2610069

SPIE.

Event: SPIE Medical Imaging, 2022, San Diego, California, United States

A read-out strategy for high-resolution large-area SiPM-based modular gamma-ray cameras

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ABSTRACT

Ongoing developments in the field of molecular imaging have increased the need for gamma-ray detectors with better spatial resolution, while maintaining a large detection area. One approach to improve spatial resolution is to utilize smaller light sensors for finer sampling of scintillation light distribution. However, the number of required sensors per camera must increase significantly, which in turn increases the complexity of the imaging system. Examples of challenges that arise are the analog-to-digital conversion of large numbers of channels, and a bottleneck effect that results from transferring large amounts of raw list-mode data to an acquisition computer. Here we present the design of a read-out electronics system that addresses these challenges. The read-out system, which is designed for a 10" × 10" SiPM-based scintillation gamma-ray camera, can process up to 162 light-sensor signals per event. This is achieved by implementing 1-bit and non-uniform 2-bit sigma-delta modulation analog-to-digital conversion, and an on-board processing system with a large number of input/output user pins and relatively high processing power. The processor is a system-on-a-module that also has SDRAM, which allows us to buffer raw list-mode data on board. The bottleneck effect is avoided by buffering event data on the camera module, and only transferring it when the main acquisition computer requests it. This design can be adapted for other crystal/sensor configurations, and can be scaled for a different number of channels.

Keywords: Gamma-ray imaging, SPECT, read-out electronics, scintillation camera, SiPM.

1. INTRODUCTION

The purpose of this paper is to present the design of the read-out electronics system for a large-area, high-resolution gamma-ray imaging camera. An increased number of light-sensor channels presents challenges such as increased electronics complexity and need for higher processing power. For instance, the output of a conventional high-speed analog-to-digital converter (ADC) is N lines in parallel, where N is the resolution of the converter. For M channels, the total number of data lines is $M \times N$. As example, 162 channels (the number of channels that our read-out system can handle) digitized at a resolution of 12 bits results in 1944 data lines, which is four times the amount of input/output (I/O) pins in conventional high-end field-programmable gate arrays (FPGAs). In order to reduce the number of lines, serial output converters or multiplexing schemes could be used. However, for the same clock frequency, the data transfer would be many times slower. The techniques we present here offer the benefits of a serial converter, without the reduction in conversion speed. We also present methods to process the large amount of data in an efficient way.

AdaptiSPECT-C (ASC) is a stationary human brain single-photon emission computed tomography (SPECT) system.[1] ASC consists of 24 7" x 7" hybrid PMT/SiPM modular scintillation cameras arranged in a hemisphere geometry, and one 10" x 10" SiPM vertex camera. The vertex camera is intended to enhance the detection of radiation from subregions of the brain related to the delivery and clearance of candidate therapeutics. Here we present the design of the read-out electronics for the 10" vertex camera, which is based on combining two read-out boards for the 7" cameras. The read-out electronics for the 7" cameras receive 81 voltage signals from

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Medical Imaging 2022: Physics of Medical Imaging, edited by Wei Zhao, Lifeng Yu, Proc. of SPIE
Vol. 12031, 120314K · © 2022 SPIE · 1605-7422 · doi: 10.1117/12.2610069

the camera photosensors.[2] The analog-to-digital conversion (ADC) is performed by sigma-delta modulation (SDM).[3] The digital side of the ADC is implemented on a field-programmable gate-array (FPGA). Energy and timing information are transferred from the FPGA to an on-board processor and buffered to on-board memory. The data is then transferred from buffer to the main computer by TCP/IP protocol. The 10" camera utilizes two read-out boards, for a total of 162 available channels. Since each event is captured by two different processors, trigger signals must be shared between the processors. For synchronization, we must keep track of variations in the clock oscillators. Individual signals on the SiPM arrays can be combined in any configuration to obtain anywhere from 1 output to 64 outputs per array. The SiPM arrays are subdivided to enhance resolution in desired areas, while maintaining a suitable number of channels for the read-out system.

2. METHODS

We digitize silicon photomultiplier (SiPM) signals with the sigma-delta modulation (SDM) technique. The output of a SDM is a 1-bit data stream, where the density of 1's is proportional to the amplitude of the input signal. In a conventional SDM-based ADC, to recover the input waveform the output is low-pass filtered. However, the sum of elements on the 1-bit data stream is proportional to the integrated input signal in a support time,[3,4] thus to estimate pulse amplitude we don't need to filter the 1-bit stream. Instead, we calculate the running sum at every clock cycle, and when an event occurs we capture the value of the running sum for every channel. One important benefit of running sums is that they utilize very few resources on the FPGA, allowing us to implement a large number of channels per device. Another advantage of the SDM technique is that for every channel we only need two FPGA pins; one for the output and one for the modulator feedback loop. Since we compute the integration of the input signal at every clock cycle, the computation speed is equivalent to a parallel ADC, with the benefit of the 1-bit output as in a serial device. The implementation of two 1-bit SDM channels is shown in Figure 1. To recover waveform information for triggering and timing purposes, we have developed a non-uniform 2-bit SDM,[5] where the digital steps can be optimized for the shape of the input signal. This results in an equivalent resolution higher than 2 bits.[6] The non-uniform 2-bit modulator consists of three comparators with programmable threshold, and three feedback paths, with feedback currents proportional to the comparator thresholds. These SDM techniques make the read-out and on-camera processing for hundreds of channels feasible.

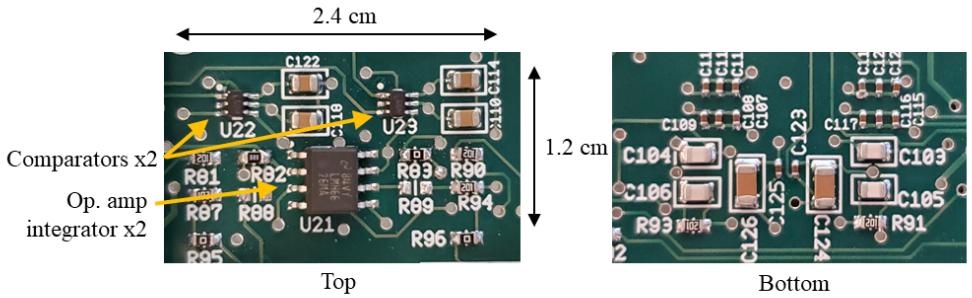

Figure 1. Two 1-bit SDMs occupy an area of approximately 3 cm^2. One channel consists of an integrator and a comparator. Two integrators are implemented utilizing a dual op-amp and feedback capacitors. Each modulator has its own comparator IC. The output of the comparator goes to the FPGA. The modulator feedback current is implemented with an FPGA output pin and a resistor. The bottom side of the board shows feedback and decoupling capacitors.

For on-board processing, we use the Ultrazed system-on-a-module (SoM) from Avnet.[7] It has a Zynq UltraScale+ chip, which contains an ARM-based processor and a Xilinx FPGA on the same integrated circuit. The SoM has 26 user I/O pins on the processor side, and 180 FPGA I/O pins. The SoM is shown in Figure 2. On the FPGA side, each SoM can handle 81 1-bit SDM channels, one 2-bit SDM, and the remaining pins are used for programming and configuration. For the 10" camera, we utilize two read-out boards, which support 162 channels.

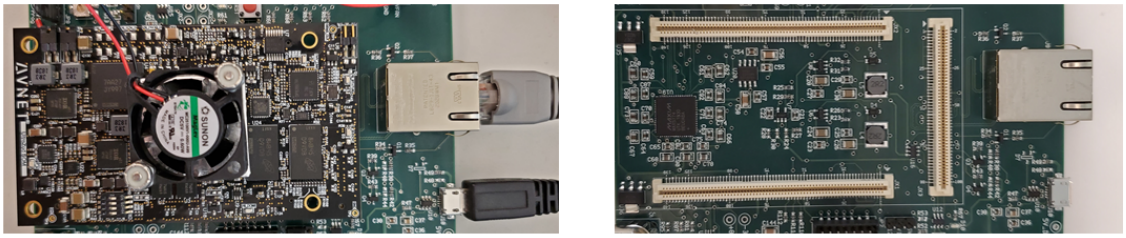

Figure 2. Ultrazed system-on-a-module, which contains an ARM-based processor, a Xilinx FPGA, and non-volatile memory. The SoM has 26 user I/O pins on the processor side, and 180 FPGA user I/O pins, which can be accessed by the headers shown on the right.

Since a single event is processed by two devices, we reconstruct the list-mode event in the main computer, as illustrated in Figure 3. Each board has its own 2 GB DDR4 SDRAM buffer, and the data is transferred from buffer to the main computer via ethernet and the TCP/IP protocol. A lightweight TCP/IP stack is implemented on each processor, thus each read-out board is a node on the network. We must keep track of any variations in FPGA clock frequency. This is done by distributing a single low-frequency clock to all boards, and counting the number of fast clock cycles in one slow clock period.

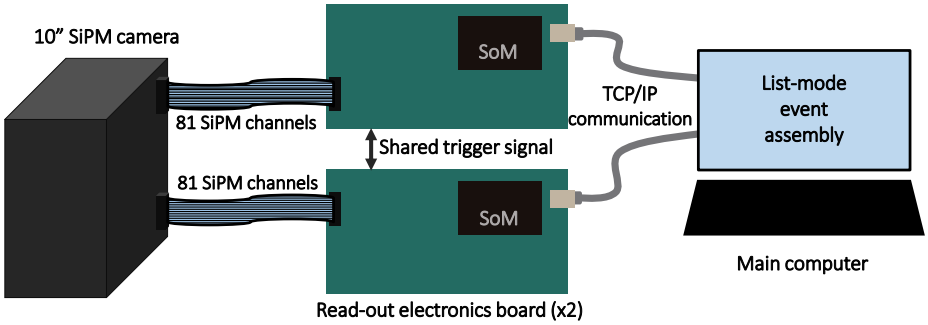

Figure 3. Since a single event is processed by two different boards, the processors share trigger signals, and the list-mode event is assembled in the main computer.

We perform the 2-bit SDM on the sum of selected channels that ensures a trigger for events at any position on the camera face. Figure 4(a) shows the signal distribution. Alternate rows are read by each board. Within the rows, alternate channels are combined to be processed by the 2-bit modulator for triggering. Figure 4(d) is a plot of the average number of photons detected by each 1” $\times$ 1” SiPM array when an interaction occurs at the center of an SiPM array. It can be seen that the light is spread significantly only to contiguous sensors. This result is used to demonstrate that the configuration from Figure 4(a) is efficient and sufficient. Each SiPM array consist of 8 $\times$ 8 SiPMs, whose outputs can be combined in any configuration. Figure 4(a) is the result of a single output per SiPM array, however the arrays can be subdivided to obtain a higher spatial resolution in desired areas of the camera. Figures 4(b) and 4(c) are examples of subdivisions than increase resolution at the edges and at the center. To find the configuration that gives the best overall spatial resolution, photon transport Monte Carlo simulations can be performed.[8] The only limitation set by the read-out electronics is that the number of channels must be 162 or less.

3. RESULTS AND CONCLUSIONS

We have designed a read-out system that can process up to 162 light-sensor signals in a single gamma camera. This is achieved by implementing 1-bit and non-uniform 2-bit SDMs, using a SoM with a large number of I/O user pins and relatively high processing power. The read-out system is for a 10” $\times$ 10” high-resolution modular

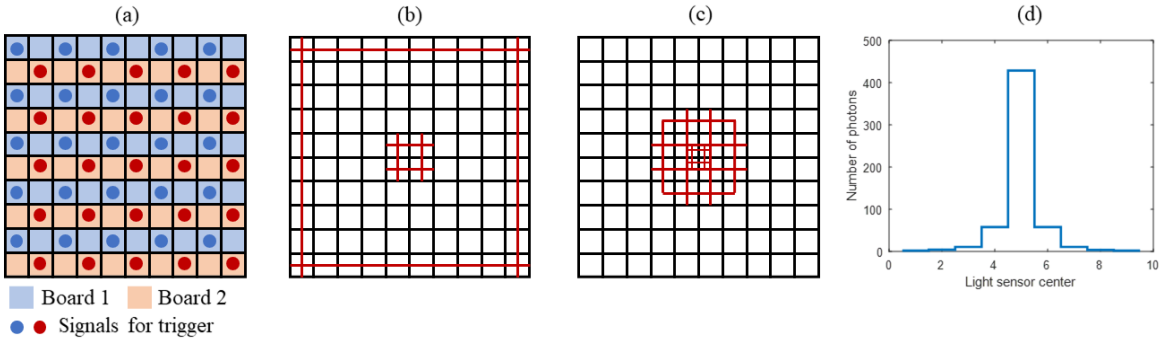

Figure 4. (a) Signal distribution for the two read-out boards. Alternate rows are read by each board. Within the rows, alternate channels are combined to be processed by the 2-bit modulator for triggering. (b) and (c) are examples of SiPM array subdivisions utilized to enhance resolution at the edges/center of the camera. (d) Average number of photons detected by each 1" × 1" SiPM array when an interaction occurs at the center of an SiPM array.

SiPM-based scintillation gamma-ray camera. This read-out electronics design benefits the next generation of gamma cameras, which are trending towards higher light-sensor density in larger detection areas.

ACKNOWLEDGMENTS

This work was partially supported by NIH/NIBIB grant 1R01EB022521. The authors disclose that Dr. Phillip H. Kuo has a financial interest in and partial employment in Invicro, a Konica Minolta Company. He is also a consultant and/or speaker for Amgen, Eisai, General Electric Healthcare, Novartis, Invicro, Bayer, Chimerix, Fusion Pharma, and UroToday. He is a recipient of research grants from Blue Earth Diagnostics and General Electric Healthcare.

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